APPLICATION NOTE

ABSTRACT
Despite the relatively simple interconnections in the DAA, extraordinary attention should be given to the layout of the DAA since it directly connects to the network. Both Part 15 and Part 68 of FCC regulations should be considered by the engineer during the layout process.

AN810
DAA printed circuit board layout

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INTRODUCTION

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EMI SUPPRESSION (Part 15b)

Most significant sources of EMI are:

– Clock traces
– Fast clock
– Two or more clocks in the same system
– High impedance ground return wires (long traces)
– Inadequate or improper power supply de-coupling
– I/O connectors where cables exist or enter the system

In order to achieve low EMI emission it is advisable to keep all clock traces as short as possible and as far from all other traces as possible, especially analog modem traces. In a system where there is more than one clock, try to keep them in separate areas of the circuit, using separate grounds to prevent them “beating together” to give rise to higher frequencies than either clock’s fundamental.

As a preventive measure, add a RC circuit (see Figure 1) as close to the clock source as possible to try to slow down the clock edge if necessary. The value for the resistor and capacitor varies depend on the clock source and the slowness for the clock edge. If the RC circuit is not needed, the resistor can be shorted with a zero ohm resistor or jumper wire and the capacitor can be omitted.

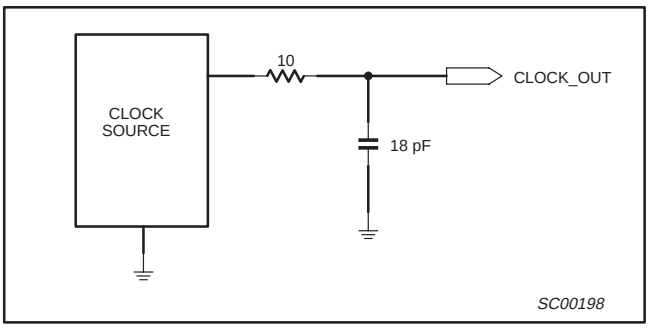

Figure 1. RC circuit

Don’t use a clock source with more drive capability (i.e., fast rise/fall time of the clock edge) than necessary. In this respect it is better to use a crystal as a clock source rather than an oscillator, since oscillators usually provide maximum drive and fastest slew rate, significantly increasing the device’s EMI emission.

All ICs should be bypassed with capacitors close to the power supply pins. Additional caps should be placed along the supply traces to ground to prevent long loop current. The supplies to the sensitive analog components such as the analog front end, operational amplifiers in the line interface hybrid must be keep separate from any digital power supplies. These supplies should be bypassed with a high quality tantalum capacitor with a value about 22 μF or larger, and a low inductance ceramic capacitor of value of 0.1 μF. The 22 μF cap is used to decouple the low frequency while the 0.1 μF is used to decouple the high frequency. One of the most common mistakes of placing bypass capacitors for a surface mount device IC on a multiple layers board, is to have the bypassing capacitors close to the power supply pads without actually having short traces from the pads to the capacitors (see Figures 2 and 3).

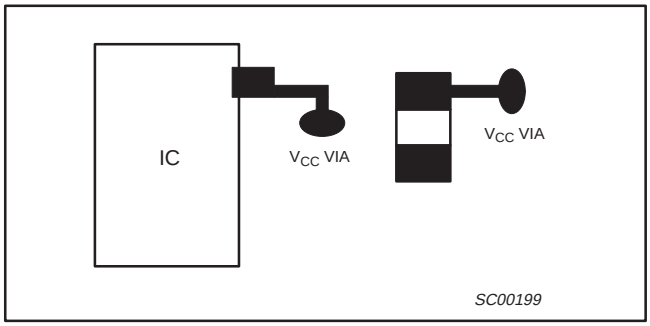

Figure 2. Incorrect way of placing bypass capacitor

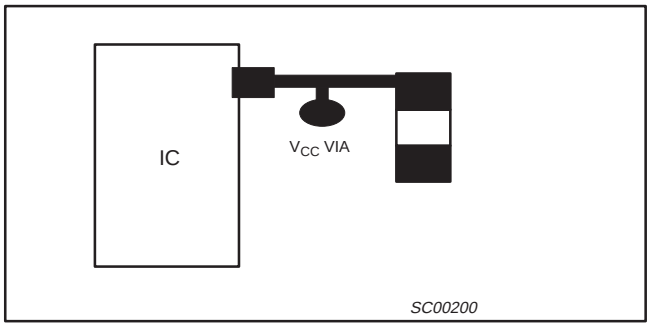

Figure 3. Correct way of placing bypass capacitor

The speaker ground and amplifier’s power connections are quite capable of influencing the performance of the modem; since they involve amplification of the input signal by as much as 20 to 30 dB, and dumping that current into the system ground at the speaker. The effect is very noticeable if the speaker is on during the modem handshake stage, causing the modem to connect at lower speed or occasion retrain if the speaker is also on after the modem has made a connection to the remote modem.

Keep the speaker circuit away from the DAA and the modem transmit and receive circuits. Use a separate power supply for the speaker amplifier and route the speaker’s ground back to the system digital ground instead of the system analog ground.

Most often failure of FCC Part 15 can be traced back to the cables that connect the system to the outside world — phone lines, speaker cable and microphone cable. High frequency signals can be blocked before they get out onto the cables by placing inductors in series with the cables at the exit points. One type of such inductor commonly used are ferrite–beads. Depending on the type, the impedance at the frequency of interest varies from 100 Ω to greater than a 1000 Ω. Use beads with impedance of about 400–500 Ω over the frequency of interest (1 MHz – 500 MHz). You can use beads with higher impedance but they will cost a lot more.

Capacitors are also used to bypass high frequency signals to earth. They are often connected to the tip and ring of the RJ-11 jack and to earth ground The most typical values in modem applications you often see are 470 pF – 1000 pF, however, the capacitors are in the DAA side of the system, they must have a rating of at least 1500 V, although 2000 V rating are often used.

TELEPHONE NETWORK INTERFACE (Part 68): Hazardous Voltage and DAA Layout

A high voltage, 1500 V, is placed between the tip and ring of the RJ-11 jack and the system ground to simulate a lightning strike. If a low impedance path exists between the DAA and the rest of the system, some traces may be burned, or some components may catch fire. To protect against this test, there must be a barrier between the DAA and the rest of the system.

The network side contains the line and phone jacks, current limiting resistors, ferrite beads, the ring detector circuit, surge protector, etc. The transformer, the ring detector optoisolator, and the hook-relay are crossed between the network side and the system side. Therefore these components must be chosen to withstand high voltages, up to 1500 VAC. A surge protector (MOV) or a spark gap is also used for extra protection, and they must be placed close to the RJ-11 with heavy traces. These devices should not conduct below the ringing voltage, and sometimes in rare cases the ringing voltage can be as much as 310 VAC. To limit the energy dissipated in this device, two current limiting resistors are added in series with tip and ring, and a total of about 20 Ω is typical.

There should be no traces that cross the barrier, either entering it or passing through it to go somewhere else (see Figure 4). Remove all ground planes and V_{CC} planes within the Network Side. Use heavy traces of at least 12 mil for all traces in the Network Side. Try to put as much space between these traces as possible. Avoid a zig-zag pattern, or 90 degree angle routing.

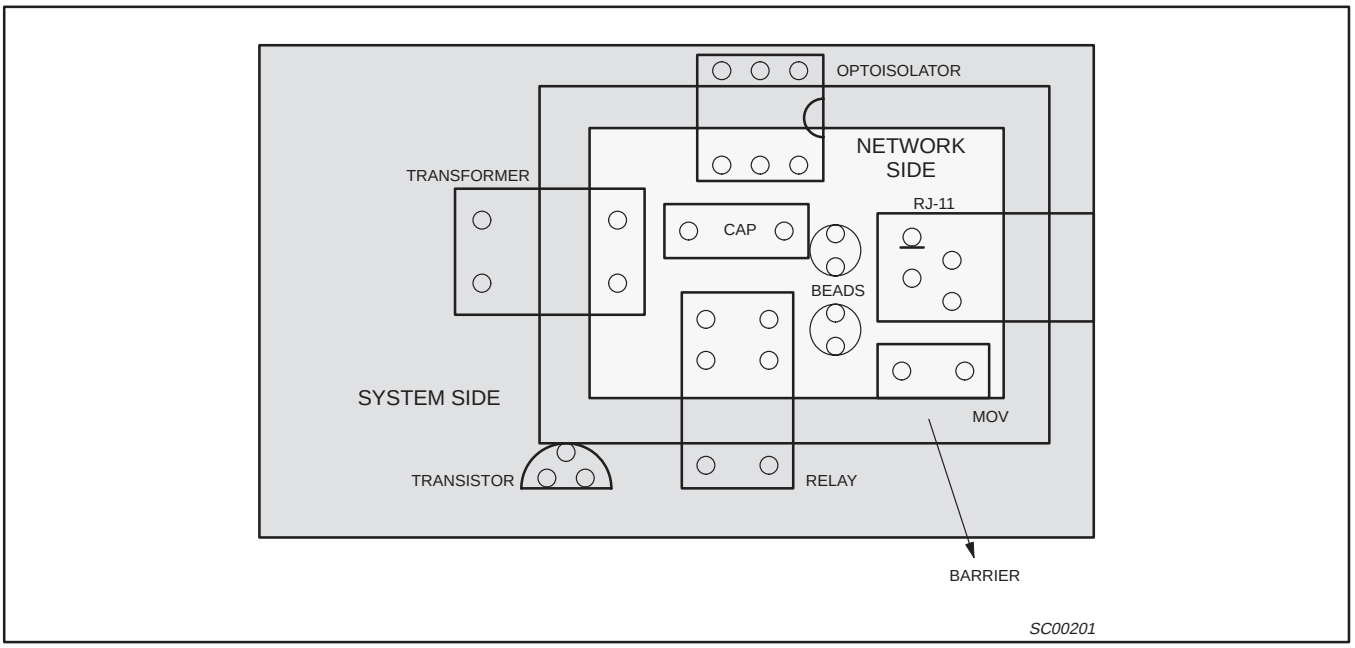

Figure 4. DAA board layout

POWER SUPPLY AND GROUNDING FOR UCB1200/1300

When using a single power supply, as suggested in the reference schematic shown in Figure 5, V_{CCA1} and V_{CCA2} should be derived from the cleanest power supplies available.

The UCB1200/1300 and its analog circuitries should be placed close together, and should have its own ground plane. The UCB1200/1300 analog and digital ground pins should be connected to this ground plane which in turn should be connected to the rest of the system ground by a ferrite bead.

Although not shown in the figures, traces bringing power to the UCB1200/1300 (V_{CCA1}, V_{CCA2}, V_{DD1}, V_{DD2}) should be as wide as possible, at least 50 mil, to keep the impedance low. Likewise for power and ground vias, they should be as large as possible.

Here is a list of guidelines for optimum printed circuit board layout.

1. Group the analog components together in one area and the digital components in a separate area.
2. Split the ground plane into separate digital and analog ground planes with digital components placed above the digital ground plane, and analog components above the analog ground plane as shown on Figure 6. The digital pins and analog pins should be connected to their own plane with very low impedance vias.
3. The ground plane split should be underneath the digital section of the chip.
4. The digital and analog ground planes should be connected together at one point and that point should be near the power supply.
5. Analog trace should be routed over the analog plane and the digital traces should be routed over the digital plane.
6. Keep digital traces and clock away from the analog area.
7. Decoupling capacitors should be placed as close to the IC as possible. (Refer to Figure 7.)
8. Use additional bypass capacitors along all power and ground traces to provide short, low impedance loops for ground currents pulses generated by high-frequency switching.
9. Power supply terminals should be shunted by quality tantalum capacitors in the order of 10 μF.
10. To reduce EMI emission from digital signal and clock, do not route the traces with 90 degree bend, use two 45 degree turn instead.
11. Use very short traces for clocks.
12. Keep the audio amplifier and speaker ground away from the rest of the modem portion due to:
    a. the magnitude of the audio current pumped into the ground (a few hundred mW peak).
    b. audio signals are amplified during the initial handshake.
    c. audio spectrum falls over the receive signal.

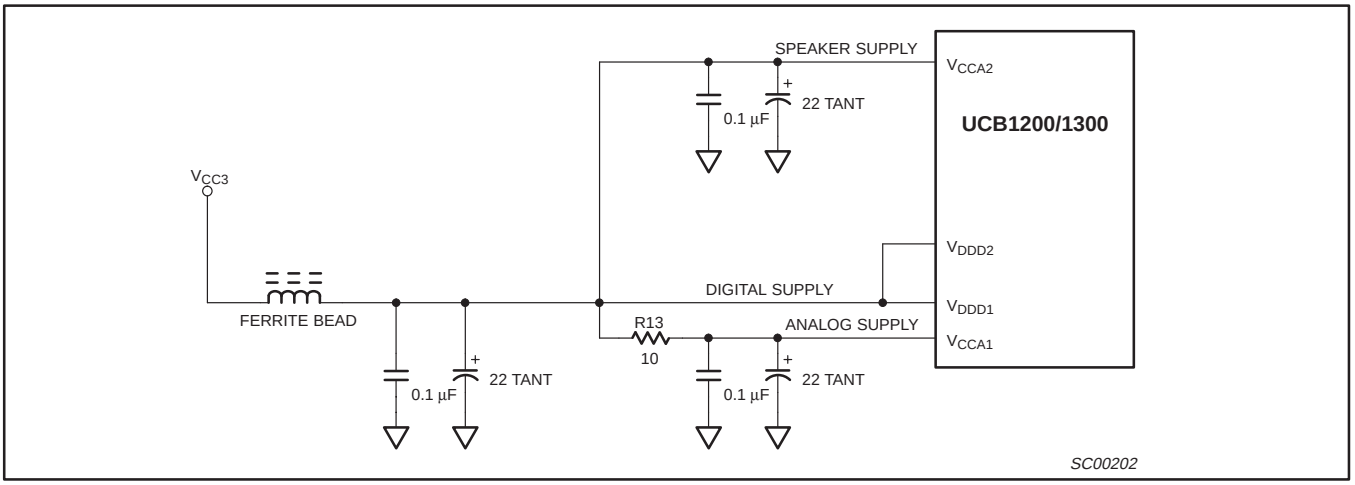

Figure 5. Power supply and grounding circuit

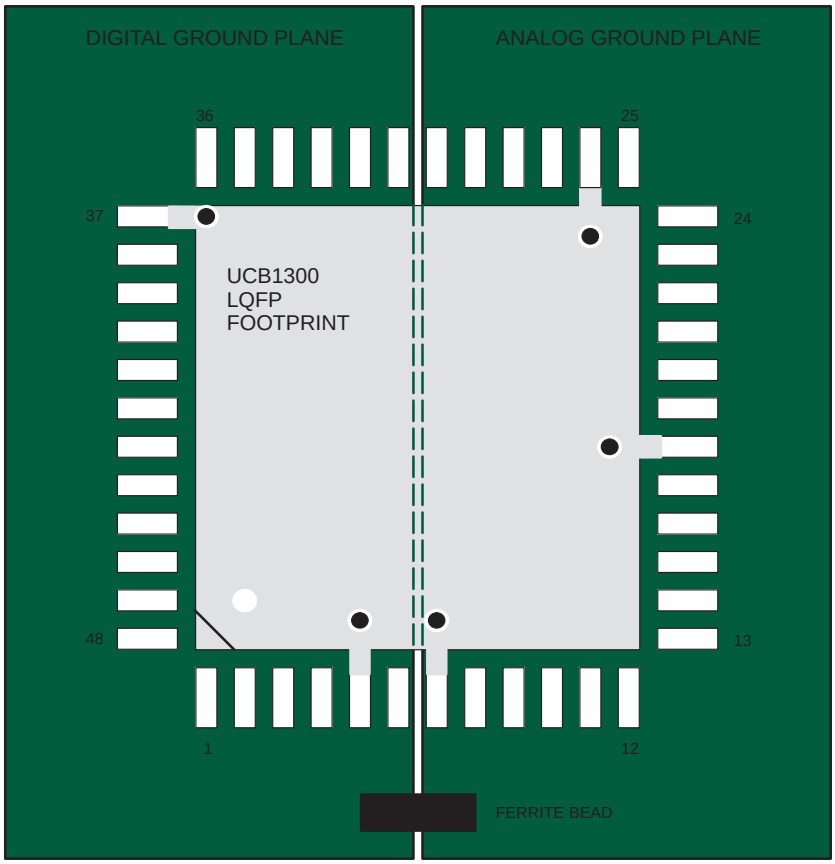

Figure 6. UCB1300 recommended ground plane

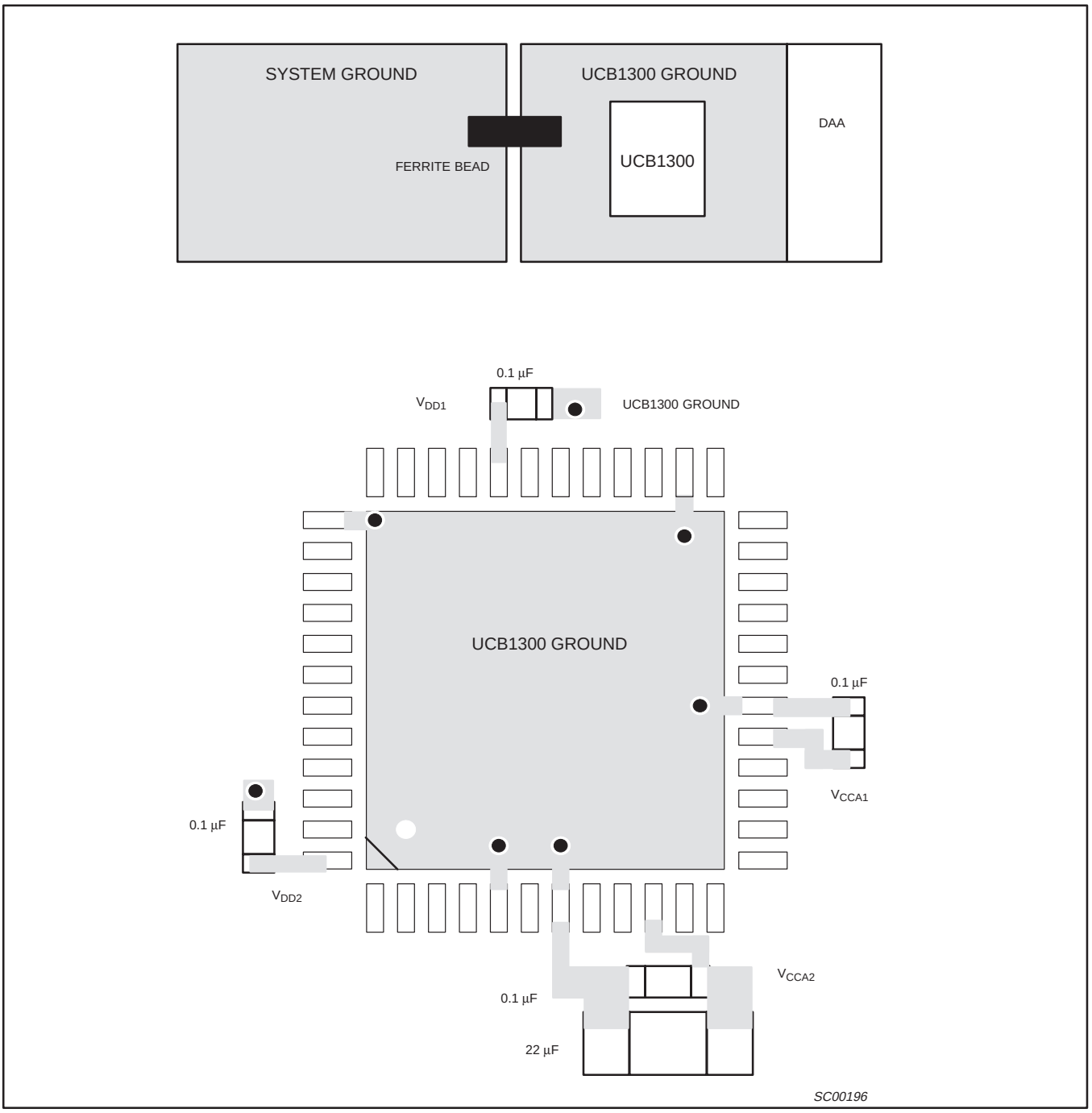

Figure 7. Printed circuit board layout for UCB1300

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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