Electrostatic discharge protection for the NE83Q92 or NE83C92 Ethernet transceiver

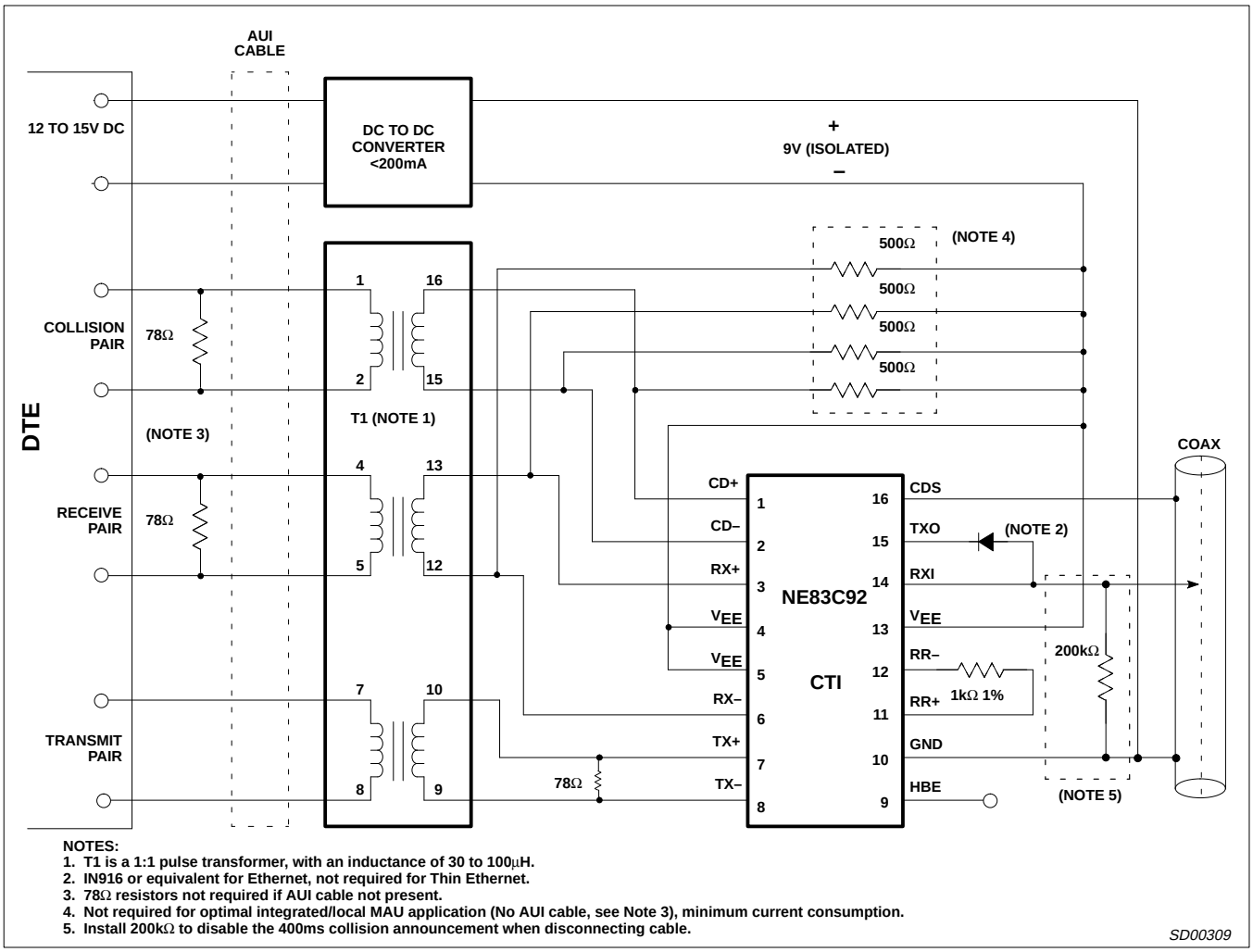
AN4004

Author: L. J. Hadley

INTRODUCTION

This application brief describes techniques which may be used to prevent damage to the NE83Q92A under certain electrical overstress (EOS) test and environmental conditions. In particular reference is made to the test conditions specified by the International Electrotechnical Commission under the IEC 801-2 guideline. Two different types of external protection devices are discussed as alternate solutions to the potential problem of internal device damage as it applies to the use of the Philips NE83Q92A in an Ethernet environment. A third alternative, robust PC board design using electrostatic principles, is mentioned briefly.

The circuit in Figure 1 shows a typical Ethernet transceiver configuration using the NE83Q92. The NE83Q92 is an industry standard type device transceiver used to interface the Ethernet coaxial LAN to the DTE or PC.



NOTES:
1. **T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.**
2. **IN916 or equivalent for Ethernet, not required for Thin Ethernet.**
3. **78Ω resistors not required if AUI cable not present.**
4. **Not required for optimal integrated/local MAU application (No AUI cable, see Note 3), minimum current consumption.**
5. **Install 200kΩ to disable the 400ms collision announcement when disconnecting cable.**

Figure 1. Typical Ethernet Transceiver

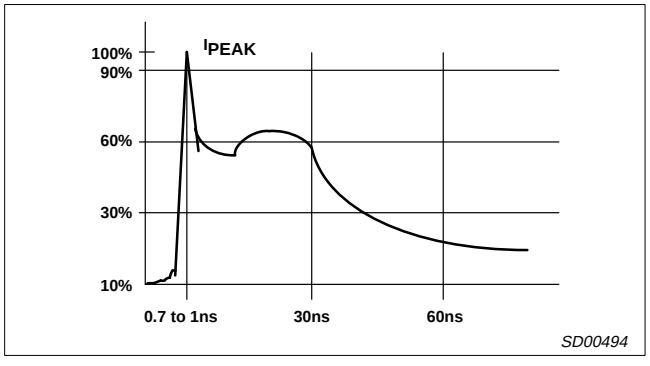


Figure 2. IEC 801-2 ESD Impulse

IEC 801-2

The specification called for by IEC 801-2 pertains to the high voltage ESD immunity standards which are required for this category of European electronics equipment. The test procedure requires that all equipment be able to withstand ten pulses of voltage magnitude 8kV through direct contact discharge or the same number of 15kV pulses by indirect air discharge. The high voltage impulses are generated by a prescribed simulated human body model electrostatic source using a 150pF capacitance discharged through a 330Ω resistance. Figure 2 shows the typical current waveform as specified by IEC 801-2.

Test Method

The test results in this report were attained using the direct contact discharge of ten 8kV impulses to the shield of the Ethernet bus coaxial shield for each device sample of the NE83Q92.

High Voltage Transient Produces E.M. Wave

In analyzing the effect of such a high voltage impulse on an Ethernet transceiver, note that the coaxial shield is connected to the - 9V common ground and the Carrier Detect Sense (CDS) line, and these connections are sometimes made by conductive traces of fairly narrow width.

As the high voltage generator probe contacts the shield of the Ethernet coaxial connector and the discharge occurs, an electromagnetic wave front is caused to propagate across transceiver board interface and to enter the circuit board. There it travels along the metal traces which connect the shield to the PC board common ground plane. As shown in Figure 1, the transceiver coaxial interface does not connect to the DTE terminal but is isolated from it by transformer coupling. Thus, any transient impulse entering the board is discharged into the transceiver circuit's distributed capacitance which may be of limited magnitude. The energy is then dissipated through leakage paths back to the reference plane or earth ground. (The actual path resistance to the ground return is in the hundreds of kΩ..) It must be noted that a current impulse flowing into the circuit board environment through narrow traces encounters an impedance to ground that is dependent upon the trace inductance. A 15nH trace inductance will exhibit nearly 30Ω of series impedance at 300MHz, which is the range of the impulse frequency spectrum. This means that a discharge pulse as specified above will force a fifty ampere transient through the trace impedance and result in an approximate 1.5kV peak at the CDS pin. Narrower traces in critical ground returns will allow even higher voltages to develop. If the voltage overstress is high enough, dielectric breakdown of the integrated circuit may occur. In addition, the current pulse will result in additional electric and magnetic field transients which are coupled to the surrounding components on the board.

note that in the case of the CDS input function, frequency response does not limit the operational effectiveness of the receiver since RXI is primarily sensitive to the average differential voltage between the CDS and RXI nodes.

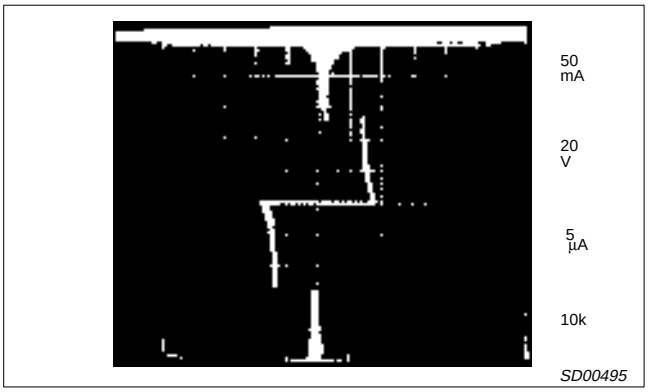


Figure 3. Bidirectional Diode (SIDACTor) Voltage Breakdown Characteristics

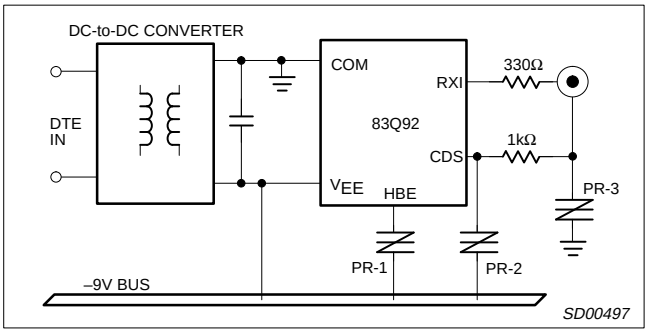


Figure 4. Transient Surge Protection Circuit

AN EXTERNAL PROTECTIVE DEVICE STOPS BREAKDOWN

The High Speed Bi-directional Clamping Diode

Two different types of external transient suppression devices are discussed. The first is a bi-directional surge protection diode SIDACtor®. This device acts as a high impedance to AC transients having a peak-to-peak voltage which is below the SIDACtor break-over voltage, $V_{BO.}$ (The particular device used in this example has a controlled breakdown voltage of 30V. The diode's breakdown characteristic is shown in Figure 3.) As long as the peak-to-peak voltage remains below breakdown a maximum leakage current of 5µA flows through the diode. Once activated the protection device exhibits a clamping resistance of 60 to 80mΩ with a voltage drop of two to three volts. A parallel precaution, in addition to the active breakdown device, involves the use of a resistance in series with the CDS pin. This acts to limit the inrush current further protecting the internal base structure. A second damping resistor may also be added in series with the RXI pin as shown by the circuit diagram in Figure 4. The impulse time delay at the CDS pin is directly related to the magnitude of the series resistance multiplied by the parallel capacitance of the surge protection diode. Using the SIDACtor as reference with a typical shunt capacitance of less than 100pF, the resulting delay is approximately 100ns. It is important to

The Multilayer Varistor

The second type of transient over-voltage protection device used in this evaluation is called a multilayer-varistor (MLV). Philips tested MLV devices manufactured by AVX under the trade name TransGuard®. The characteristics of the MLV are different than the SIDACtor in principle but effectively achieved the same results. The MLV device relies on the semiconductor breakdown action of a Multi-layer ceramic-zinc oxide junction to clamp high speed voltage transients within nanoseconds. The MLV device voltage breakdown characteristics are shown in Figure 5 below.

While its shunt capacitance is higher than the SIDACtor diode by an order of magnitude, this should not interfere with the CDS circuit operation, as explained above.

Both types of ESD protection devices were tested and proved effective in preventing internal breakdown of the NE83Q92 under the IEC 801-2 test procedure. An 8kV conducted impulse was applied to the RXI BNC connector shell in each analysis. Air discharge testing, as is also defined by IEC 801-2, was not included since conducted direct connect discharge was considered the most severe.

(TransGuard® is a registered trade mark of AVX Corp.)
(SIDACtor® is a registered trade mark of TECOR Electronics, Inc.)

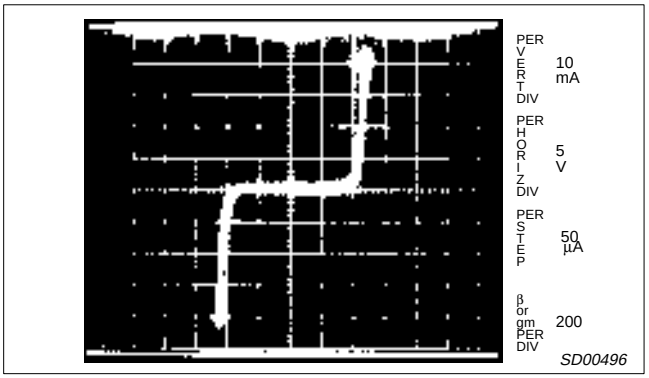


Figure 5. MLV Voltage Breakdown Characteristics

The Physical Layout

The circuit board configuration used to evaluate the TransGuard MLV devices is shown in Figure 6. Note that a 1 resistance is added in series with the Collision Detect Sense (CDS) pin of the NE83Q92 to further prevent internal stress on the device by providing current limiting at the base of the input transistor for the collision sense circuit. The protection devices are placed at three points around the NE83Q92 as follows: (1)- BNC shield to common ground plane; (2) CDS pin to $-V_{EE}$ bus; (3) and HBE pin to $-V_{EE}$ (if the HBE function is not used as an active input, the protection device between Pin 12 and $-V_{EE}$ may be eliminated. In this case connect Pin 12 directly to $-V_{EE}$.) (4) A 330Ω resistor is added in series with the RXI input to further limit current spikes from being induced into the input pin as discussed above. **There is no apparent degradation of Ethernet performance or specification compliance with the addition of the CDS and RXI resistors of these values.**

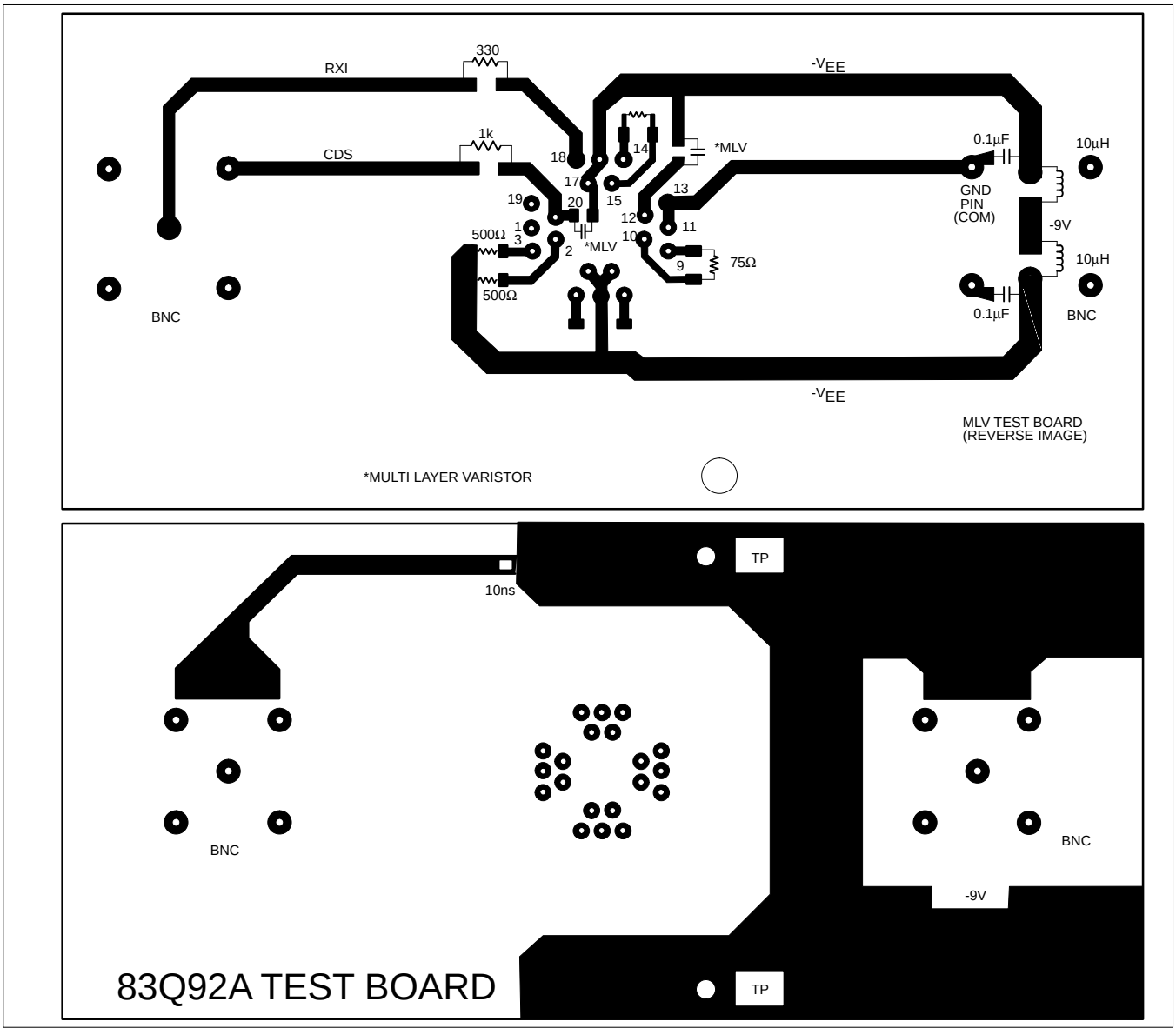


Figure 6. MLV Test Board

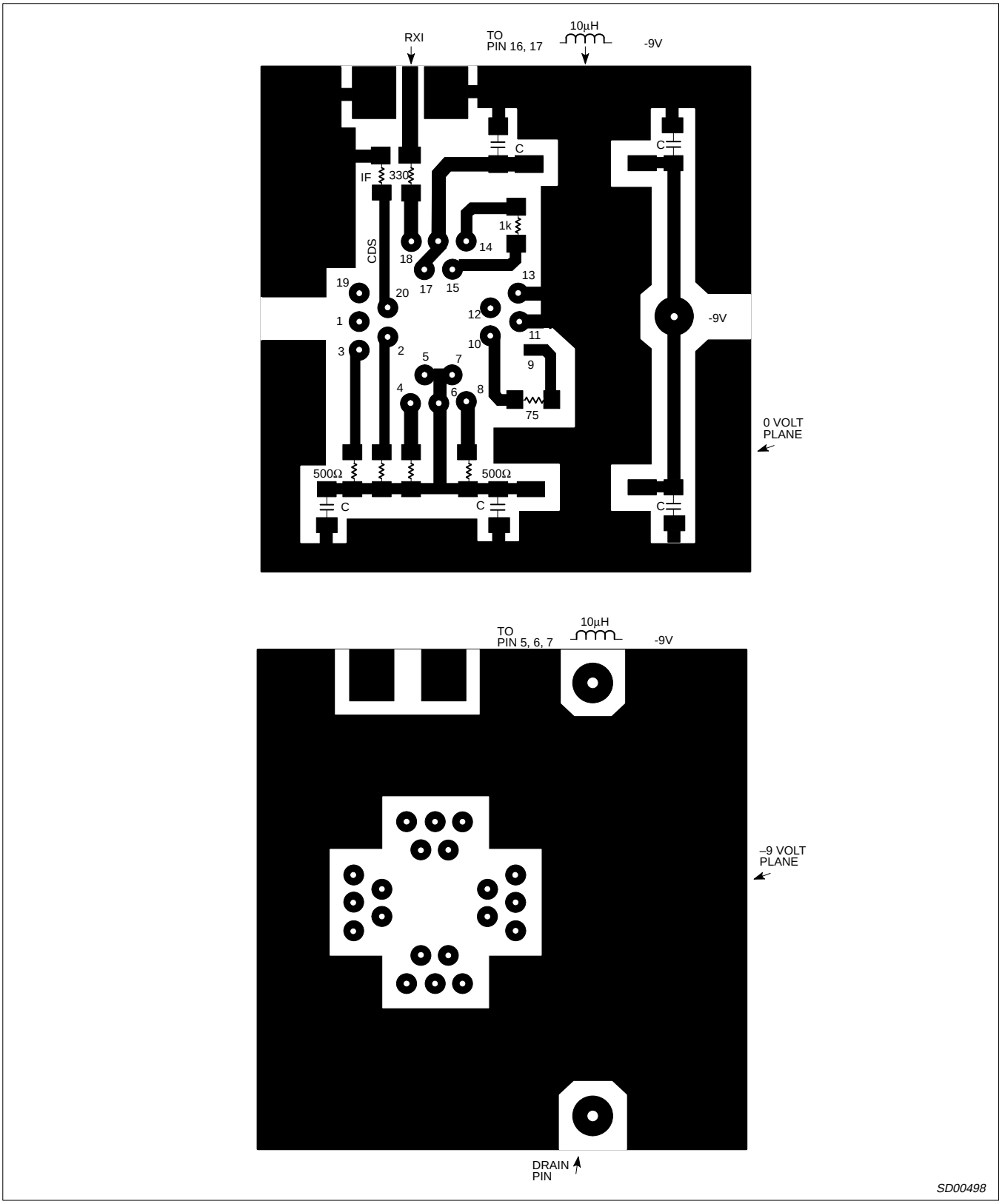


Figure 7. Electrostatically Robust PC Board

Electrostatically Robust Board Prevents Breakdown

The circuit board in Figure 7 shows one example of ESD protection which successfully protected the NE82Q92 for voltages up to 9.9kV without the use of external protection devices. This circuit board is designed to prevent high voltage impulses at the coaxial shield from overstressing any of the NE83Q92 pins by a combination of two conductive circuit planes and low inductance returns.

By careful layout, distributed shunt capacitance across the device supply leads is used to absorb transient pulse energy. Keep in mind that voltage across any distributed capacitance is directly proportional to instantaneous charge, so even a small capacitance will limit peak voltage build-up under transient conditions. The goal is to force the input conductor shield (0V plane) and $-V_{EE}$ plane to respond to a voltage transient on the coax as if it were single capacitance with a low impedance charging path on the supply side, but a high impedance return to the external system ground reference. This allows the protected circuit to ride out the surge like a cork responding to a wave crest in water.

Separate 0V and $-V_{EE}$ circuit planes act as low impedance surge paths, in addition to adding parallel shunt capacitance which absorbs charge and reduces high voltage gradients in proximity to signal conductors. In the actual test circuit, RF chokes and shunt bypass capacitors were used to simulate the supply decoupling and to isolate the external bench supply from the high voltage impulse.

The Test Set-up

IEC 801-2 testing is carried out using a ground plane with symmetrically attached 470kΩ isolation resistors connected between the Ethernet transceiver and the ground plane (see Figure 8). The 8kV IEC 801-2 pulse voltage is applied between the copper ground plane and the shield of the Ethernet coax as illustrated.

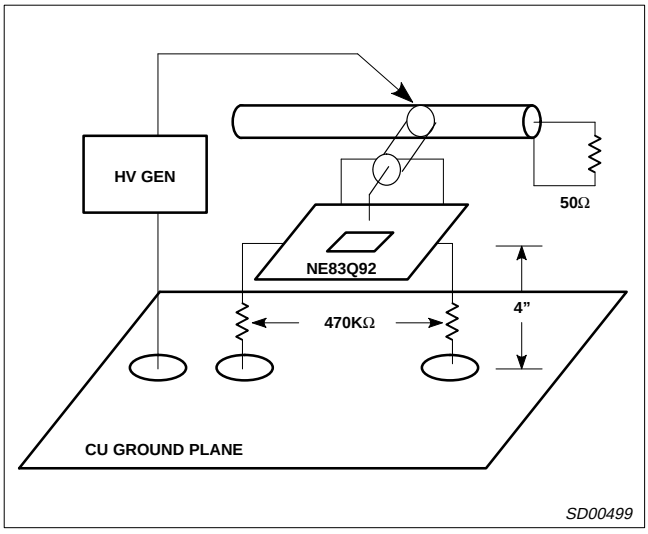


Figure 8. IEC 801-2 Test Setup

CONCLUSION

It is possible to provide high voltage transient protection to sensitive on-board circuit devices by using electrostatic and electromagnetic principles as a guide to ESD-robust PC board design. This option may present a formidable problem to the designer faced with limited board space and insufficient copper ground plane to effectively do the job. In this case, external protective devices are the most logical choice. The external transient limiting device approach lends itself both to new board design and to the retrofitting of existing Ethernet boards.

Device Specifications

SIDACtor - PO300-3EA70
- Rating:
  - Clamping Voltage V_{BO} = 27 - 36 Volts
  - On State Voltage = 2 - 3 Volts
  - $I_{max\ surge}$ = 30 Amps
- Package TO-92

TransGuard VC080512A250
- Rating:
  - V_{BO} = 25 Volts
  - Working Voltage = 12 V_{DC}
  - Peak Energy = 0.1 Joule
  - Peak Current (8/20µs) = 40 Amps
- Package- 805 SMD

Test Equipment: Schaffner Model NSG 432
- Static Discharge Simulator
- -9 Volt regulated bench supply
- Tektronix Semiconductor Curve Tracer Model 576