APPLICATION NOTE

ABSTRACT

Galvanic node isolation is an important consideration in the design of IEEE 1394 bus systems. Connecting a non-isolated node to a properly functioning bus can stop all bus activity, or worse yet, cause the communication on the bus to become unreliable. This application note describes the node hardware design process in a step-by-step manner so that not only the design step is discussed, but the reasoning behind the step is made clear to the designer. Node power supplies and bus power are also discussed.

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IEEE 1394 bus node galvanic isolation and power supply design

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OVERVIEW

Galvanic node isolation is an important factor in the design of IEEE 1394 bus systems. Connecting a non-isolated node to a properly functioning bus can stop all bus activity, or worse yet, cause the communication on the bus to become unreliable. This application note describes the node hardware design process in a step-by-step manner so that not only the design step is discussed, but the reasoning behind the step is made clear to the designer. Node power supplies and bus power are also discussed.

SUMMARY

This application note is divided into four sections:

1. The need for and principles of Galvanic Isolation in the design of a 1394 bus node;
2. Practical Galvanic Isolation techniques related to Philips Semiconductor chips;
3. Supplying power to a Galvanically Isolated 1394 bus node;
4. A quick reference to inter-pin coupling of Philips Link and PHY chips.

The first section discusses what Galvanic Isolation is and why it may be required in the design of certain bus nodes. Typically, the need for isolation is brought about by the interconnection of different earth ground domains by means of the 1394 bus. Earth ground domains may get connected to bus nodes in insidious ways; this section of the Application Note is meant to sensitize the reader to this fact.

Practical (low cost, manufacturable) methods of implementing Galvanic Isolation are presented in section two. The use of Philips' single capacitor isolation system is discussed, with simple, low cost suggestions for dealing with the need to get low frequency signals across the isolation barrier. Attention is paid to specific answers to problems presented on a pin-by-pin basis.

Many questions in the minds of node designers center on powering the isolated node. Section three delves into several ways to supply power to the PHY circuitry and the bus in both isolated and non-isolated node designs.

The suggestions for designs in this Application Note are not meant to be exhaustive of all possible techniques. Many of the suggestions have been implemented and are in production at the time of writing of this document. Great care has been taken to present solutions that have been proven in the laboratory and in production where possible. We solicit comments and alternative solutions from the reader for future versions of this Application Note. Please send your comments and alternate solutions to 1394@philips.com.

SECTION 1: GALVANIC ISOLATION EXPLAINED

The Need for Galvanic Isolation

Galvanic isolation refers to a design technique which will separate signal currents from AC power distribution introduced stray noise currents. Basically this process will provide two separate paths for signal and noise currents which will not allow them to mix or to mix only over short distances, thereby minimizing the effects of noise currents on the signals.

Where do the noise currents come from? In North America and other parts of the World the power distribution systems introduce a safety factor into the system by referencing local power (that is found in the home or office) to a local earth grounding point. Each building typically has its own local earth grounding point (usually a rod or pipe driven into or routed through the earth near the building). One wire from the power distribution system is connected to the local earth grounding point. The potential difference between the human body and the earth ground is zero. Other wires in the power distribution system are now referenced to earth ground by means of the local ground … in a North American home the maximum available potential difference between any AC power wire and ground is about 120 volts rms. This is true even though the power introduced to the building has a total potential of 240 volts … the transformer from which the power is derived has a center tapped winding connected to earth ground. This system is known as a split phase center tapped earth referenced distribution system. Please note that EACH building has its own earth reference point; large buildings may have several earth reference points (at the convenience of the electrical distribution system). Because the Earth does not present zero electrical resistance between local earth ground points, differences of potential build up between these ground points. Also, any time there is any difference of potential, we have a current flowing. Imagine an earth ground point every 50 feet or so, the magnitudes, directions and frequencies of the earth borne currents are mind-boggling! Add to this potpourri of currents an occasional dish antenna ground, or ground wave from a radio transmitter and you have an extremely complex jumble of currents at frequencies from DC to microwave.

Your house is built with electrical wiring running to each power outlet. In North America, we use two wires to conduct the AC currents and we include a third "safety ground" wire to allow connection to the local earth ground. You plug in your computer and monitor to a single outlet. Since both your computer and monitor have switching power supplies, they are required to have filters installed which remove some of the noise currents which would travel on the power lines. These currents typically are summed and sometimes their algebraic sum is zero, most of the time it is not. The summing point for these noise currents is the "safety" ground line. The noise currents on the safety ground line are seeking to return through the power line to the power distribution transformer near your home. You have now introduced some noise at a jumble of frequencies to your home's safety ground. Now ground is no longer quiet, at least to sensitive electronic equipment. A few hundred millivolts difference of potential now is added to the safety ground line.

For each outlet and piece of "grounded" equipment connected to the outlet, the amount of noise current introduced to the safety earth ground increases. In your neighborhood, each home contributes its share of electrical noise to the earth ground. Each individual local ground imparts more noise to the earth. The greater the distance between the two earth grounds, the more difference of potential will be measured.

In a suburban environment, dramatically different ground "domain" potentials rarely get connected together. The earth ground for the home electrical system is usually not far from the earth ground used for the CATV (cable TV) distribution system. Broadcast TV antennas and satellite antennas are usually located close to the house and therefore their associated ground potentials are about the same as the home electrical system ground potential.

In a city environment, there are usually more electrical noise problems with earth grounds. In a high-rise building, the earth ground resides at the bottom of the structure. As we measure ground potentials at different levels in the building with respect to the earth ground, we find increases in electrical noise as we ascend. CATV coaxial cables enter the building in the basement. The roof of the building may have one or more broadcast/satellite antennas on it. The grounds for these signal sources can carry electrical potentials very different from those found in the building electrical system.

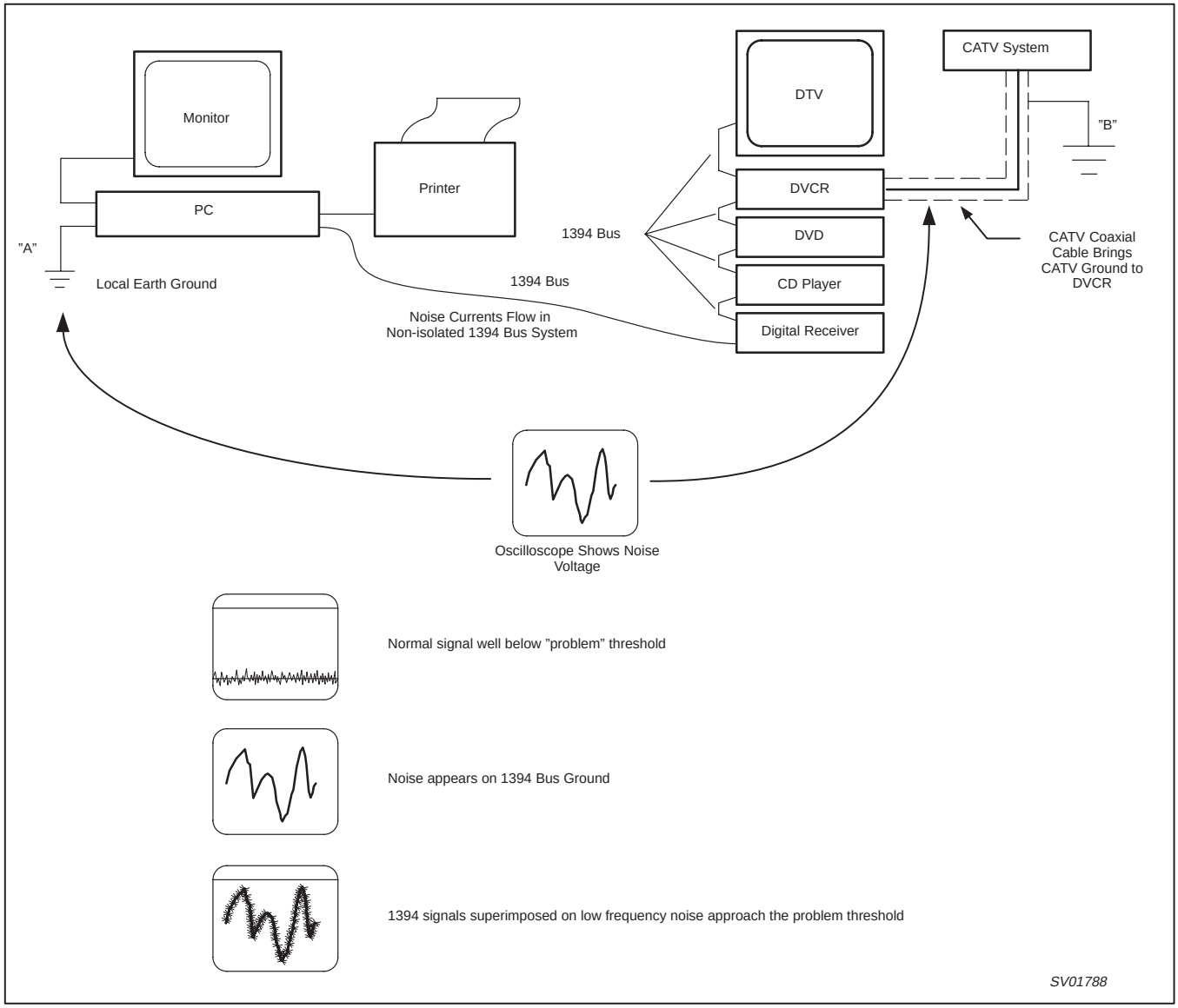

Figure 1.

Now connect the PC side of Figure 1 with the consumer equipment side by means of an IEEE 1394 bus cable. In most cases, the difference in ground noise potential will produce only a small amount of bus ground noise current. However, in some cases these currents can be in the order of magnitude of amps! The ground domain marked “B” may have a distinctly different potential with respect to ground domain “A”. This difference of potential results in current flow on the IEEE 1394 bus ground wire which connects the two domains.

If either of the nodes (PC or Digital Receiver) were to incorporate galvanic isolation, little or no bus ground current would flow and the two systems would be isolated from each other. It’s important to know which nodes on a bus employ isolation; use of an isolated node to interconnect a PC system to a CE system can prevent bus malfunctions.

IEEE 1394 signals are digital in nature, but are transmitted at low levels in order to reduce electromagnetic interference. Common mode voltage and current signaling (requiring a ground return path) on the order of a few hundred millivolts and a few milliamps is used routinely on the bus. A few hundred millivolts/milliamps of accompanying noise can disrupt the operation of a 1394 bus.

PRINCIPLES OF GALVANIC ISOLATION

The solution to the noise problem above is to not allow the noise current to flow in the ground return path. If we can provide a means of electrically separating the grounds of the two device “domains” we will eliminate noise current flow which could disrupt our common mode signals.

We must alter our thinking slightly to include thinking of ground “domains” or islands. The equipment connections above tie two different ground domains (“A” and “B” as shown in Figure 1) together by means of the bus ground return wire... this results in noise current flow in the ground return wire which causes problems. This concept will become important when we realize that signals on the 1394 bus

are relatively low level (hundreds of millivolts) as opposed to logic signal levels from 3.3 volt digital parts.

To readers familiar with the 1394 bus, it may seem that the use of a 4 wire bus cable would “solve” the ground noise problem. In fact, the 4 wire bus cable (while not having a shielded ground wire provided for the sole purpose of interconnecting node grounds) uses the cable shield itself to interconnect node grounds! So we have the same or even greater potential for a problem with the use of the 4 wire bus cable. The problem can be greater than that seen with the 6 wire bus cable because the interconnection resistances involved with the use of the cable shield “ground” are higher than those of the 6 wire cable, leading to greater differences of potential across the 4 wire cable. Furthermore, with the shield now carrying common mode signals, it becomes a source of electromagnetic interference.

While isolating nodes on a 1394 bus is not quite as simple as installing a transformer, the above illustration serves to show the general principles of galvanic isolation. Now we will look at specific solutions related to the 1394 bus.

To begin, instead of thinking of a piece of equipment as being in a single ground domain, we should separate the application domain from the physical layer domain in each bus node. For simplicity we will concentrate on the design of a single bus node.

Each node consists of several “layers” of interest. The Physical (PHY) layer translates bus level signals into logic level signals and vice-versa. The Link layer (link chip) gathers and groups the bus data into packets and quadlets for presentation to the application (also formats for bus transmission). The application layer (application) uses the information transmitted on the 1394 bus for some end purpose (like displaying it on a monitor, recording it on tape, etc.). Typically, the application layer and the link chip share a common ground and power domain; that is, their grounds and power supplies are tied together by direct connection. In non-isolated nodes, the PHY is also directly connected to the link chip and the application ground and power domains.

Using Figure 1 above, and bearing in mind that the PHY communicates at voltage levels between 100 and 200 millivolts on the 1394 bus, we become aware that noise voltages of several hundred millivolts could disrupt bus communications. However, the same amount of noise impressed on a 3.3 volt digital signal will usually not cause any problem at all. In the remainder of this application note we will strive to keep noise currents away from the PHY domains of the nodes by using galvanic isolation.

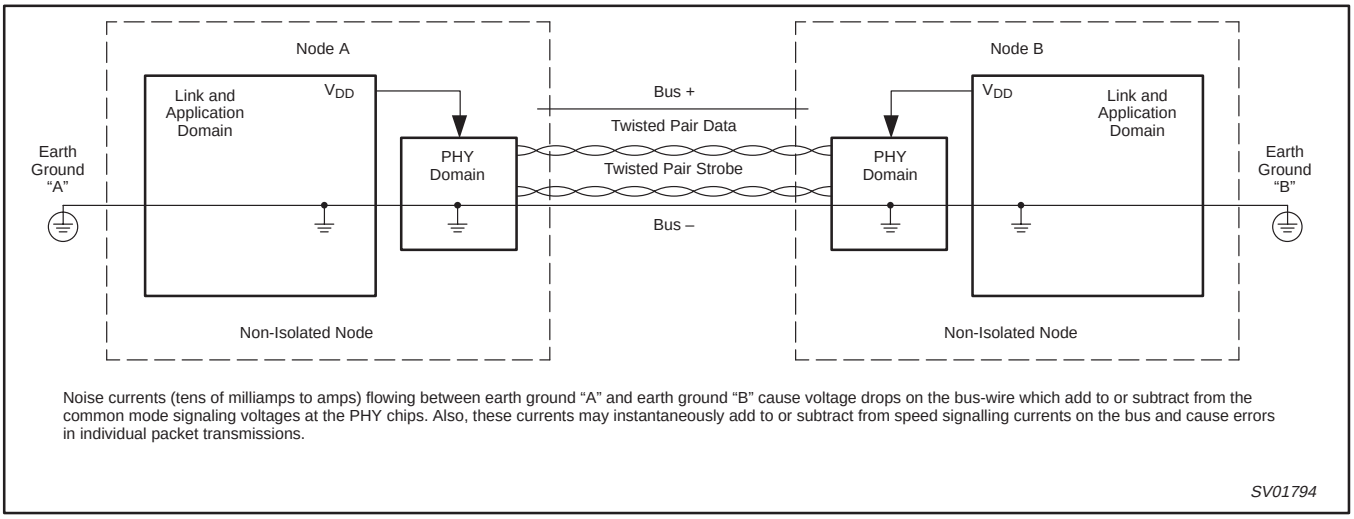

Figure 2.

In Figure 2, we see an example of two non-isolated nodes on a bus. The bus cable interconnects the two nodes with 6 wires: a twisted pair for transporting the data signals, a twisted pair for transporting the strobe signals, a wire for carrying bus power from node to node, and the bus ground wire (bus –). The twisted pair wires carry signals with amplitudes of 100 to 300 millivolts (with respect to the opposite wire in the pair... this is differential mode signaling). Impressed on the twisted pair is a voltage with respect to the bus ground wire; that is, each of the twisted pair wires has a “DC” level on it which is at the same level with respect to the bus ground wire. This “DC” voltage is typically between 1.3 and 2.5 volts and occasionally makes short duration excursions below and above those levels for signaling purposes. Differences of potential developed in the bus ground wire circuit add to or subtract from the common mode “DC” voltage level. If these voltages approach several hundred millivolts, bus signaling is affected.

If earth grounds “A” and “B” are far apart and have large differences of potential between them, currents of several hundreds of milliamps to amps may flow on the bus ground wire. Note that there is a direct connection between earth ground “A” and earth ground “B” in Figure 2. In Figure 3, note that there is a block called “isolation” between the link and PHY domains of Node A. This isolation may take the form of transformers or small value capacitors as will be discussed later. In either case, the large bus ground wire currents are prevented from flowing directly between the two earth grounds by the presence of these high impedance components in the isolation block.

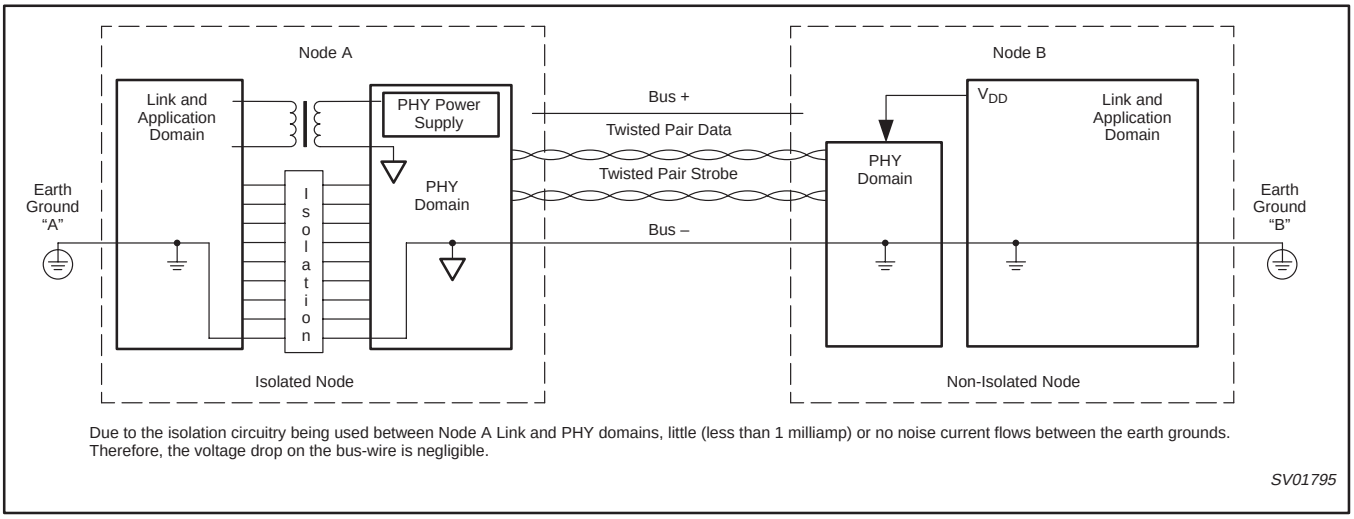

Figure 3.

To those readers familiar with IEEE 1394 node design, placing transformers (several) between the link chip and PHY chip will result in complete isolation between these domains … no current will flow between the transformer primary and secondary circuits except for the intended link-PHY interface signal currents. Performing isolation through the use of transformers works in an obvious way.

IEEE 1394, ANNEX J TRANSFORMER ISOLATION

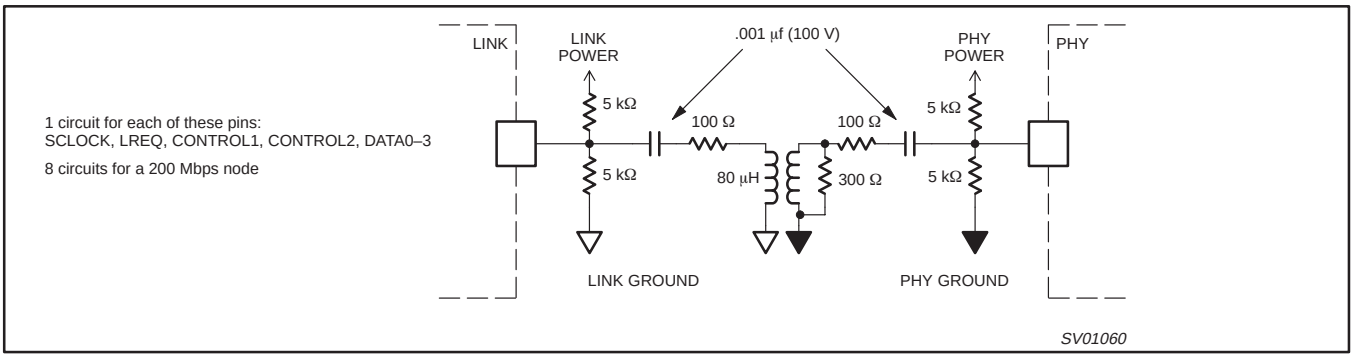

Figure 4. Transformer isolation (provides galvanic isolation up to 500 V)

IEEE 1394, Annex J transformer isolation is shown in Figure 4. While this form of galvanic isolation provides the highest level of protection, it is expensive and requires a large quantity of PC board space. Philips link and PHY chips may be used with this type of isolation in environments requiring nodes to tolerate large potential differences between grounds. Normally, voltage potentials are no more than a few volts between nodes. Some industrial applications could require transformer isolation, however. Consult the Philips 1394 Applications Group if you encounter an isolation problem where ground voltages differ by more than 20 volts (peak or DC). For clarity purposes only one of 8 signal lines (for a 200 Mbps node) has been shown in Figure 3. 56 resistors, 16 capacitors, and 8 transformers will be required for full implementation of transformer isolation in a 200 Mbps node.

Performing isolation through the use of capacitors is not so obvious until we look into the frequencies of the signal and noise currents involved in this interface.

Signal frequencies between the link and PHY chips are typically based on a 50 MHz clock (SCLOCK). The signals are digital in nature and swing through the full supply voltage (3.3 volts in most cases). The rise times of the signals are typically very fast, 2 nanoseconds, and the lowest frequency components will not go much below 50 MHz, with the highest frequency components of the signal approaching 500 MHz.

The ground noise frequencies are typically much lower in frequency. Since high frequencies don't travel great distances without significant attenuation, the VHF and UHF components of the ground noise spectrum are at very low levels (if they can be measured at all). More common frequency components result from the use of switching power supplies; still more common are the fundamental and harmonic frequencies of the power line frequency (50 or 60 Hz). In reality, measured ground noise currents seldom have frequency components over 1 MHz. The fact that these two operating frequency "spectra" are so far displaced from one-another is in our favor.

If small value capacitors (1 nF) are used as "isolation" components, we see that the high frequencies of the link-PHY interface will be able to be "passed through" the isolation component while low frequency earth ground noise will be attenuated by these components. In fact, the most injurious frequencies, those near the power line fundamental frequency, will be very greatly attenuated; just a look at the ratio 60 Hz/50 MHz and one will become aware of the amount of attenuation (118 dB).

Another important factor in Figure 3 is the presence of the power supply transformer between the link/application domain and the PHY domain. Isolation of the PHY power supply is required in order to separate the PHY ground system from the link/application ground system. The isolation of the PHY power supply can be accomplished by means of a transformer (or separate transformer winding off the main power supply) or by means of an isolating DC to DC converter. In any case, the ground of the link/application domain MUST be isolated from the PHY ground domain. The fact that isolation exists is also shown by the use of different ground symbols for each domain.

With the isolation in place as shown in Figure 3, the Node A PHY circuitry remains directly connected to earth ground B by way of the bus-wire in the bus cable. Because a high impedance at ground noise frequencies has been introduced in the “isolation” box within Node A, little or no current flows from the Node A PHY domain ground to the Node A link/application domain ground. The voltage level on the Node A PHY domain ground is the same as that of earth ground B due to isolation having been employed. Now there is no large earth ground related noise current flowing in the bus ground wire, and hence, no large voltage drop on the bus ground to interfere with common mode bus signaling.

If the bus cable between Nodes A and B in Figure 3 were to be disconnected, Node B’s PHY domain will remain at earth ground B potential and Node A’s PHY domain ground will adjust to the same potential as earth ground “A”. This happens due to the influence of a large resistor (1 Meg Ohm) which is connected between the Node A link/application ground and PHY ground. This resistor is required by the 1394 standard when isolation is employed (it’s usually placed in parallel with the ground coupling capacitor).

IEEE 1394, ANNEX J CAPACITIVE ISOLATION

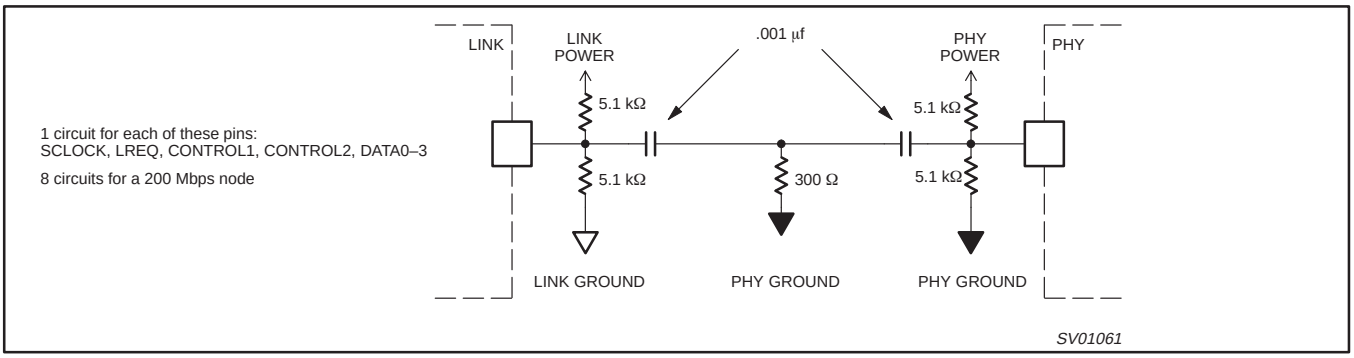

Figure 5. Capacitive isolation (provides galvanic isolation up to ≈ 60 V)

Figure 5 shows the IEEE 1394, Annex J capacitive isolation solution. This type of isolation is useful up to about 60 volts DC (or peak) ground potential difference levels. Note that several resistors are required to provide the proper biasing of the link chip and PHY chip pins. Also, if employed, close attention should be paid to the ground connections in this circuit. Like the transformer isolation technique cited in Figure 4, one of each of these circuits is applied to each signal line between the link and PHY chips. That means in a 200 Mbps node there will be 8 of these circuits required ... that’s 56 resistors and 16 capacitors! This circuitry requires almost as much PC board area as the transformer isolation solution shown in Figure 3.

Philips has simplified the capacitive isolation circuitry shown in Figure 4 by internally biasing the link-PHY interface signal pins and also reducing the required number of coupling capacitors to one per signal line. This is known as the Single Capacitor Isolation System.

SECTION 2: PRACTICAL GALVANIC ISOLATION TECHNIQUES

Ground and power isolation: (minimum component count method).

The Link layer and Physical (PHY) layer ground and power planes should be thought of as islands. Referring to Figure 6, it can be seen that there are typically four islands (domains) of importance in an isolated design:

1. The Link layer power and ground domain
2. The PHY layer power and ground domain
3. The port connector shield ground domain
4. The application ground (chassis frame) or earth ground domain

Each of these domains consists of the local ground and power plane in a multilayer printed circuit board layout. For illustrative purposes, each of these ground and power planes are considered of equal size for a given domain.

The Link domain typically consists of ground and power planes that feed the Link and application microcontroller, codec, interface circuitry, analog I/O in the case of a VCR or DVD player, etc. Due to the fact that there can be many different clocks and sub-divisions of clock frequencies, the Link ground domain is typically a very noisy electrical environment. Placing the link chip near the edge of such an environment is usually a good practice. Referring to Figure 6, the link chip is shown near the eastern edge of the Link domain. It is assumed that the power supply to this domain is fed to the link chip from the west or northwest part of the domain, therefore the power supply currents do not flow between the link chip and the eastern edge of the domain. This minimizes the amount of high frequency noise current between the link chip and its eastern domain boundary. The link chip should be oriented in the domain so that pins that interface the PHY are facing the PHY domain. The use of a straight-line flow approach to signal currents should be considered for three reasons (1) usually minimizes the area of PC board consumed, (2) paths of signal and noise currents are easily determined, (3) minimizes line capacitances to preserve signal integrity.

The PHY domain is typically smaller than the Link domain because it only involves the PHY chip, the isolated portion of the PHY power supply and the outboard discrete components used to bias the 1394 bus and couple the PHY to the Link. It would be a good design practice to place the PHY power source to the northeast or southeast of the PHY chip, this will act to reduce the high frequency power supply noise currents that appear between the PHY chip and the western border of the PHY domain. It is desirable to allow only Link-PHY related currents in the ground plane of the western side of the PHY domain; in parallel with this, the same is true of the eastern side of the Link domain. Minimizing the distance between the western edge of the PHY and the western edge of the PHY domain is also a good practice. However, the ground plane should not be cut back so much that it does not extend under the traces involved with the Link-PHY interface bus and associated circuits. The PHY ground plays a big role in controlling spurious (radiated) noise from these traces. The PHY chip itself should be oriented in this domain so that the pins that interface with the link chip face the link chip. This orientation will then place the port related pins facing the port connectors; again, a straight-line approach to signal flow.

As shown in Figure 6, the Link-PHY coupling capacitors are placed over the gap between the Link and PHY domains. The gap may be as small as 1 mm, but should not be made larger than about 5 mm for shielding purposes. (The gap is exaggerated in the drawing). The capacitors are shown as C1, C2, C3, etc. with CR and RR shown near the middle of the grouping. CR and RR are ground return paths for AC and DC currents traveling on the Link-PHY interface. If possible, it is good design practice to place the ground return parts (CR and RR) on the centerlines of the Link and PHY chips straddling the domains gap. In this way, the currents that flow between the Link and PHY will have a short path back to their source through the Link and PHY ground pins; this will minimize the amount of noise impressed on the ground currents along the way.

The coupling capacitors, C1 through C8, should be placed symmetrically around the ground return parts (CR and RR). The recommended signal line for each capacitor is indicated in the chart below:

C1	LREQ
C2	SCLK/SYSCLOCK
C3	PHYCTL0
C4	PHYCTL1
C5	D0
C6	D1
C7	D2
C8	D3

These placements are recommended for the L21 link chip interfacing with a P11A PHY; other link/phy combinations will have slightly different placements.

Connecting the lines as indicated in Figure 6 results in short traces which minimize line capacitance and radiated noise.

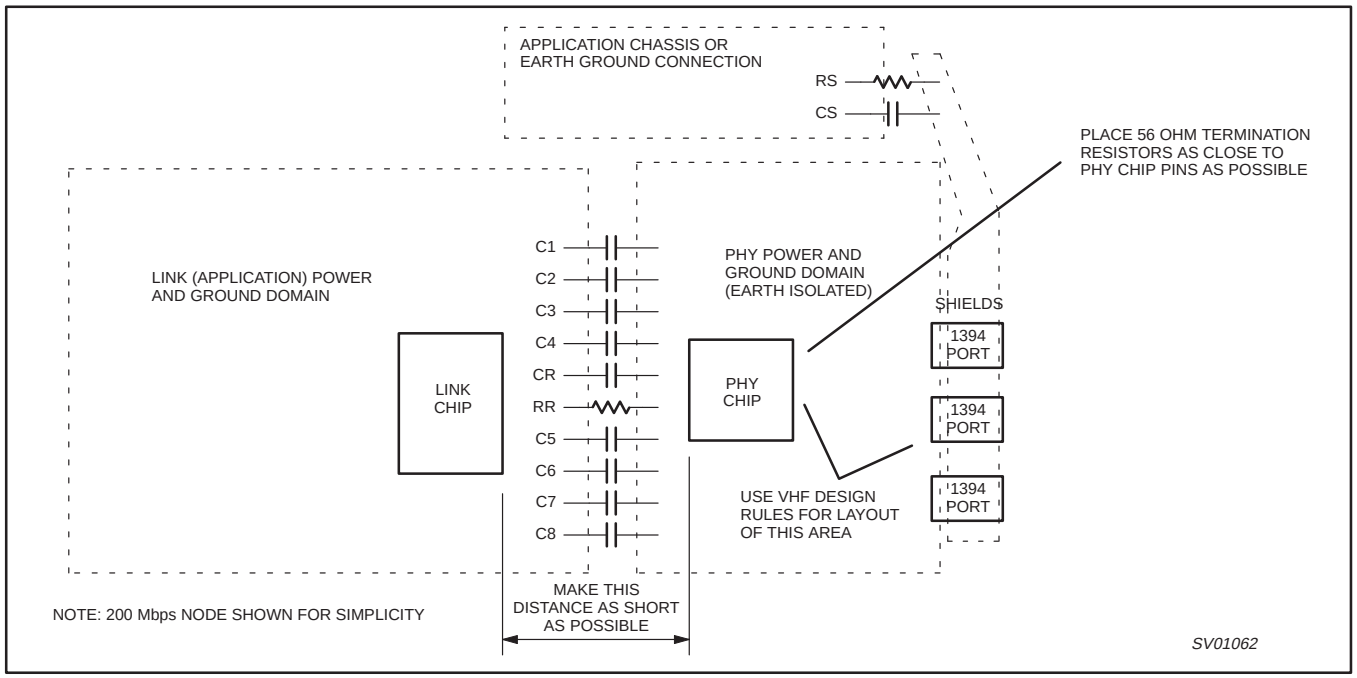

Figure 6.

NOTICE to users of L11-P11/P11A, L21-P11/P11A chip set combinations: It has been determined that the galvanic isolation coupling capacitor charge initialization provided by these parts, in some cases, does not allow the signal line coupling capacitors to fully initialize their dc charge states. This can result in one or more coupling capacitors becoming charged after power up. Coupling capacitors that are charged are capable of effectively coupling only part of the signal amplitude across the galvanic isolation boundary. We recommend that each signal line in the above chip combinations be equipped with a 39K resistor pull-down (connected to link ground for link side pull-downs; connected to PHY digital ground for PHY side pull-downs) in order to properly bias the capacitors after power up. Signal lines affected are SCLK, LREQ, CTL0..1, PHYDATA0..3. Uni-directional signals (SCLK and LREQ) require the pull-down resistor be applied ONLY to the input side of the coupling (i.e., for SCLK, on the link side of the system; for LREQ, on the PHY side). For the remaining bidirectional signals a pull down resistor must be placed on each side of the coupling capacitor.

The 1394 cable shields must be treated independent of the Link and PHY ground domains. Typically the shields of the bus cables are exposed to noise currents from several sources. Any high frequency noise voltage differences between nodes result in high frequency noise currents on the shield of the cable connecting the two nodes. Also, some noise from the transitions of data and strobe lines inside the cable appears on the cable shield due to capacitive and inductive coupling. According to IEEE 1394, it is good practice to avoid connecting the shield pins of the port connectors to the local PHY ground. Such a connection might introduce earth referenced noise currents into the PHY domain … the only path from the PHY domain to an earth ground return would then be through the CR/RR path which is used as the signal current return path between the Link and PHY. The added noise currents can disrupt Link-PHY communications. The recommended method of cable shield termination is sown in Figure 6. Notice that the shields connect to either the application frame/chassis ground (in the case of a earth isolated frame) or directly to earth ground at the point where the application ground is connected to earth ground (typically near the mains supply cord attachment point). Using Figure 6 as a guide, it can be seen that noise currents impressed on the cable shield are shunted away from the PHY ground domain (in favor of the earth or application chassis ground), thus leaving the PHY domain appreciably quieter from the standpoint of electrical noise. Electrostatic charges (ESD) present on the bus cable shield prior to connection will also be safely routed away from the PHY chip by means of this connection.

The application ground domain connection to earth ground varies greatly with the specific application. Some appliances are provided with a 3-wire mains cord which carries earth ground to the chassis of the appliance by direct connection. This is obviously the simplest way to rid the appliance of earth-referenced noise and electrostatic discharge currents. However, most consumer electronics such as VCRs, DVDs, TVs, audio components, etc., are fitted with 2-wire mains connections and thus lack a direct earth ground. Each manufacturer has their own way of coping with electrostatic discharge and noise currents. Appliances connected to antennas typically are equipped with safety agency approved networks that vector electrostatic discharges to the power line via a safe pathway. These appliances have an established “pseudo ground” for this purpose. Consideration should be given to connecting the IEEE 1394 cable shield domain (through the RC isolating network) to such a pseudo ground if allowed by the relevant safety agencies. This connection will vary from application to application; it is left to the equipment designer to make this connection in a safe manner and in strict accordance with the safety agencies.

Special attention should be paid to the voltage ratings of capacitors and resistors used in this circuit. It is suggested that consideration be given to using a 100 nF, 630 volt rated polyester (self healing design). It is also suggested that the resistor be a leaded part of 1/4 to 1/2 watt rating in order to obtain suitable voltage stand-off. Other methods of handling ESD while making the required signal coupling are shown in the section called “Powering the Node”.

We recommend that the PHY and the link chips be reset simultaneously when capacitive Galvanic isolation is used. For L11, L21 and P11/P11A parts, the reset must be held at least 100 uS to allow the signal line coupling capacitors time to equalize their charges so that these capacitors are able to pass full amplitude signals. Power up reset of these parts needs to last at least 3 milliseconds in order to allow the PHY clock to start and stabilize. The L4x, P2x part combinations require less reset time for a hot reset because they have enhanced coupling capacitor charge initialization circuitry. Hot reset time for the L4x, P2x part combinations should be 30 uS minimum. The reset state at power up should last the recommended 3 milliseconds to allow the PHY clock to stabilize regardless of which part combination is used.

NODE DESIGN DECISIONS

Once the decision has been made to apply galvanic isolation to an IEEE 1394 node design, several other decisions need to be made. The isolation issues that have been discussed to this point have been involved with coupling the high frequency signals (50 MHz) across the galvanic isolation barrier. We now turn to the other signals involved in the link-PHY interface and to the galvanic separation for link and PHY power domains.

Accomplishing galvanic isolation by means of the use of small coupling capacitors works well when the signal frequencies are at least two orders of magnitude above the unwanted noise frequencies. The signals about to be discussed have frequency components well below 50 MHz, some approach 0 Hz (dc).

The designer at this point will need to make the following decisions:

1. Will I reset the link and PHY chips from a common signal source? (Highly recommended)
2. Do I need to use the power-down feature of the PHY?
3. Do I need to supply an LPS signal to the PHY? (L11 and L21 nodes only)
4. How do I interconnect the L4x and P2x “C/LINKON” signals?

Attendant with the above decisions are issues involving the PHY power supply:

5. How will I provide isolated power to the PHY in my design?
6. Do I need to supply power to the 1394 bus?
7. How do I use bus power to supply my PHY?

Each of these seven issues is discussed below.

Decisions regarding low frequency control signals

1. Will I reset the link and PHY chips from a common signal source?

When galvanic isolation is employed, this is a very desirable course of action. Resetting the link and PHY chips from the same signal source is the only way to guarantee that the isolation coupling capacitors will be discharged and able to pass the entire signal amplitude when required. If the link and PHY are reset from different sources, the coupling capacitors may be subjected to different dc levels across the capacitors. This leads to capacitor charging, which results in the capacitor’s inability to couple the full amplitude of the signal from one side of the isolation barrier to the other.

The reset signal is a very low frequency signal... in fact it is a dc level for most of the time that the node is powered. A capacitor cannot be used to couple this signal across the isolation barrier. Optical isolation devices (optocouplers) are used to provide the coupling. Optocouplers do not operate well at high (50 MHz) frequencies (those that may are quite expensive!); hence, they are not used to couple the link-PHY interface signals. However, for the reset signal coupling the circuit of Figure 7 (or its equivalent) is suggested. The optocoupler and ancillary components are inexpensive and consume a small amount of board real estate. The reset signal source may be the same as that used for the microcontroller unit or it may be a pin of the microcontroller itself. The timing associated with the reset signal is critical. We recommend a 3 millisecond reset time period when power is first applied to the PHY (this also means the link will be in the reset state for 3 milliseconds). The 3 milliseconds allows the PHY clock to start and stabilize; the 3 milliseconds link reset time will not effect the link operation. If it is desired to reset the link and PHY during operation (any time after the initial 3 milliseconds after power-on), a 30-50 microsecond reset period should be used for L4x/P2x part combinations. For L11/P11A and L21/P11A part combinations a 100-150 microsecond reset time period should be used.

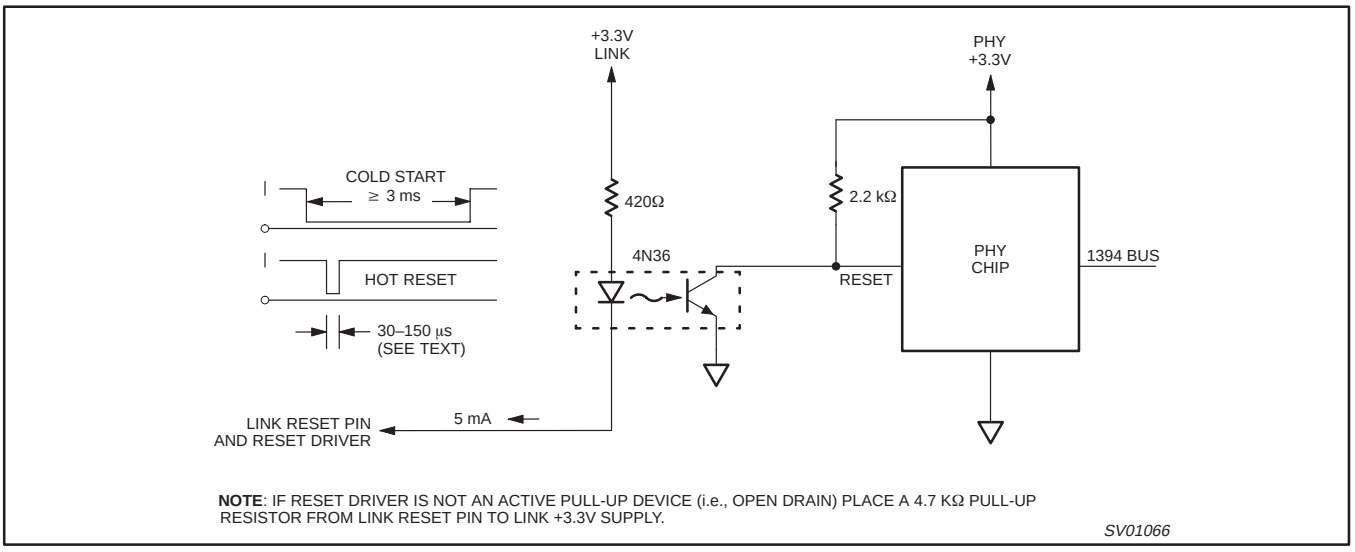

Figure 7. Resetting a galvanically isolated PHY

Example: Resetting a Galvanically Isolated PHY

If it is desired to perform reset functions on a Galvanically isolated PHY the circuit shown in Figure 7 may be used. Please note that the PHY is subject to two reset conditions: (1) power-up and (2) hot restart. The power-up reset condition is initiated by the initial application of PHY power. When the PHY is just coming to life its clock will take some time to start and become stable (typically 1–3 milliseconds). The reset state (low) must be held on the PHY reset pin during this time for proper initialization of the part. After the PHY has operated for more than 3 milliseconds, it is considered in the "Hot" condition. A reset while in the Hot condition can be initiated by a short low condition on the PHY reset pin.

Using the circuit in Figure 7, the 4N36 opto-isolator has specified rise and fall times of about 5 microseconds (μs); actually, measured rise times with this circuit have been 4–5 μs, fall times have been 8–10 μs. Using the measured parameters, we need 30 μs minimum driving pulse width on the Link side to guarantee that both Link and PHY chips reset during a Hot reset condition. The power-on reset of the node, being of much longer duration, does not present a timing problem.

It should be noted that the LED drive to the opto-isolator requires about 5 milliamps of current; to obtain this amount of current may require a special reset driver.

2. Do I need to use the power-down feature of the PHY?

Use of the PHY power-down feature may be desirable in order to conserve power when no active bus cables are connected to the node. The CNA line from the PHY may be optically coupled to the application and the application MCU can assert the PHY PD pin via another optically coupled circuit to accomplish PHY power-down. Even if PHY power-down is not implemented, it may be useful for the application to determine that there are no active bus cables connected to the node so that the link and its associated circuitry may be powered-down. The PHY PD and CNA optical coupling circuits are shown in Figures 8 and 9.

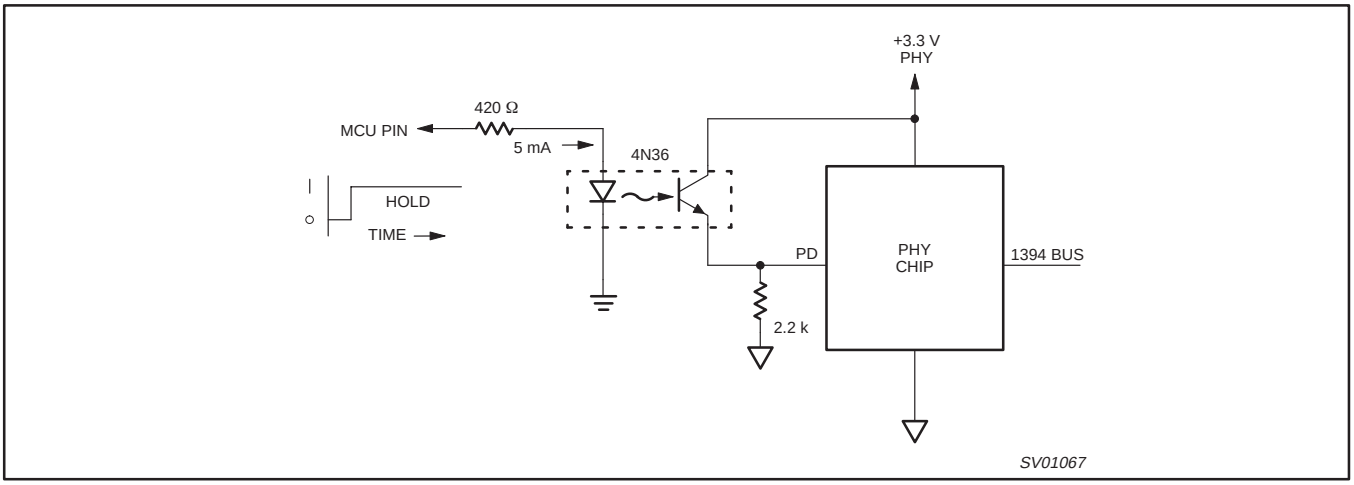

Figure 8. Isolated node implementing PHY power-down

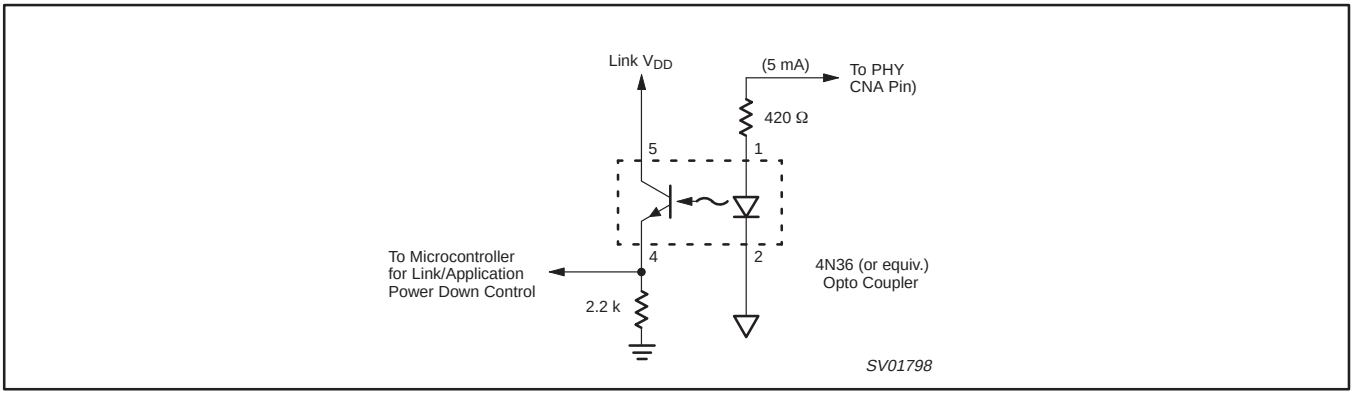

Figure 9. Isolated node connecting PHY CNA signal to node control MCU

Example: Galvanically Isolated Node Implementing PHY Power-Down

The Philips PHY is equipped with a power-down pin which allows the PHY to consume less power during node idle periods. If it is desired to power-down the PHY of a galvanically isolated node, use the circuit shown in Figure 8.

Because the PHY power-down may be of unknown duration, but usually more than seconds of time, we recommend the use of an opto-isolator circuit. The 4N36 (or equivalent) part is inexpensive and readily available. Use of the recommended resistors will provide fast rise and fall times on the PHY side of the circuit and allow for smooth operation. The 420 Ohm current source resistor on the application side of the node will require 5 milliamps of current from the logic source which is controlling the PHY, this may require the use of a special component. The size of the resistor on the PHY side (2.2 k) will require about 1.5 milliamps from the PHY supply when operating.

When the PHY enters power-down its clock is stopped and all node activity ceases. When the power-down signal is removed, the PHY requires about 3 milliseconds to re-start its clock and recover from the reset state. This time lag should be taken into account by the software which is driving the node (link chip).

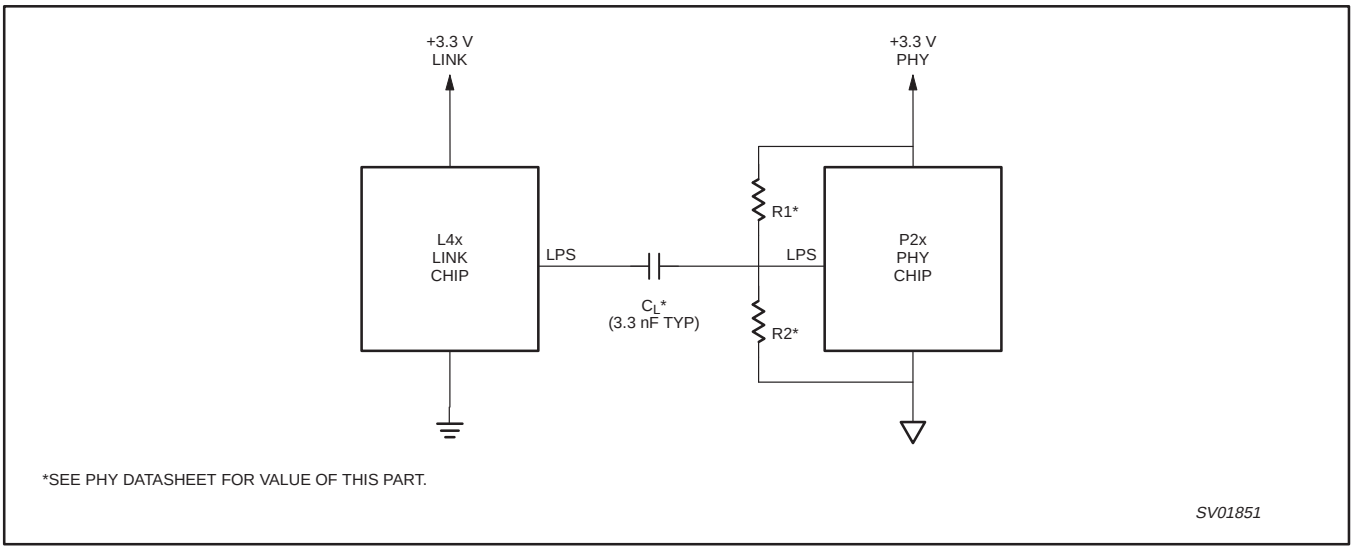

Figure 10. Single capacitor LPS coupling for use with L4x links and 400 Mbps PHY chips

3. Do I need to supply an LPS signal to the PHY?

For L4x/P2x equipped nodes, the LPS signal is coupled between domains by means of a coupling capacitor (see Figure 10). However, L11 and L21 link chips are not equipped with LPS pins. If it is desirable to inform the PHY of the state of power (powered-up or powered-down) of the link layer, the optically coupled circuit shown in Figure 11 may be employed.

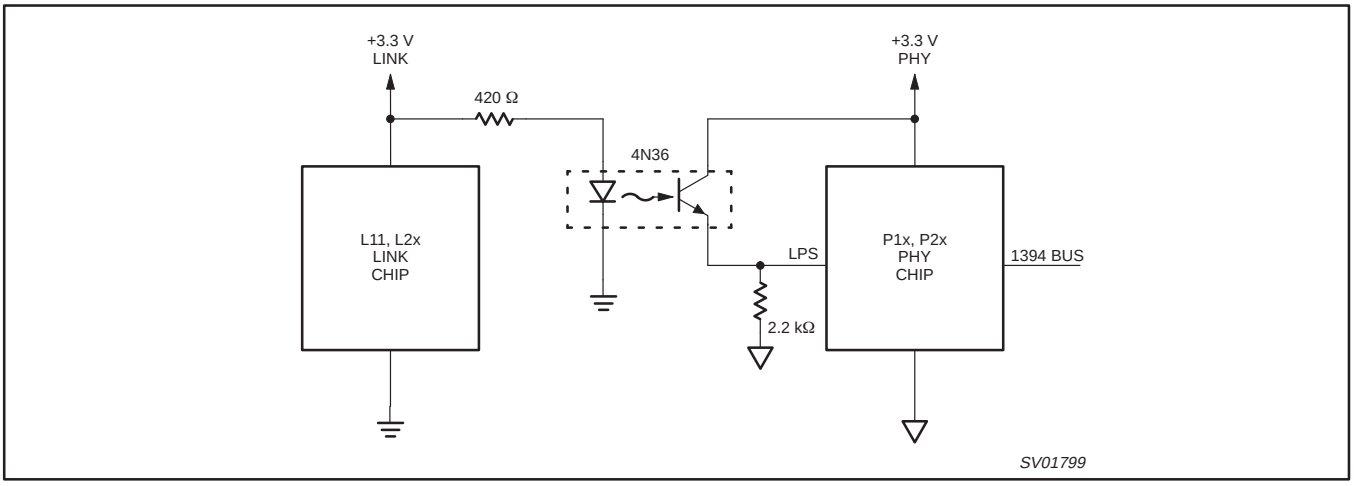

Figure 11. Using the link power to supply LPS to the PHY

Example: Two Ways to Configure the PHY LPS Pin of a Galvanically Isolated Node

The LPS pin allows the PHY to determine if the connected link chip is powered. A high level on this PHY pin holds a counter within the part in a continuous reset state and thus indicates to the PHY that its Link partner is powered. The LPS pin does not care whether the LPS signal is a continuous high DC level or an intermittent high level (as from a pulse train or square waveform).

Figure 11 shows the LPS pin being isolated by means of an opto-isolator circuit. The 4N36 opto-isolator provides up to 2500 V_{DC} isolation between the PHY and Link domains. The Link power supply contributes about 5 milliamps of DC current to the LED of the opto-isolator. The PHY side of the circuit supplies about 1.5 milliamps to the 2.2 k Ohm resistor, thus pulling the LPS pin high to indicate that the Link power is present. Please note that this circuit indicates only that Link power is present, not that the link chip is actually operating. The PHY ISO– pin should be tied to PHY V_{DD} unless IEEE 1394 Annex J isolation is being used on the signal pins (data, control, and LREQ).

4. How do I interconnect the L4x and P2x “C/LINKON” signals?
This way!

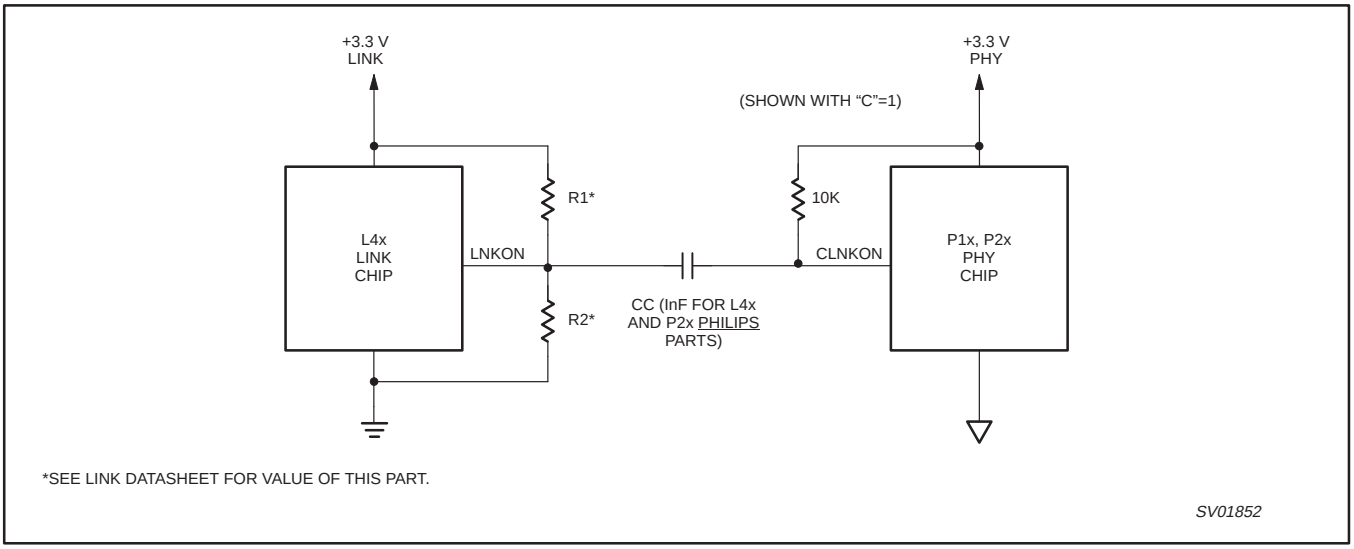

Figure 12. Single capacitor LINKON coupling for use with L4x links and 400 Mbps PHY chips

SECTION 3: DECISIONS RELATED TO SUPPLYING POWER TO THE PHY CIRCUITRY AND THE BUS

5. How will I provide isolated power to the PHY in my design?
There are many ways to accomplish power supply isolation (isolating the PHY power supply from earth ground referenced circuits). Figures 13, 14, 15, 16, and 17 show some of the ways. Note that the simplest and most cost effective ways are outgrowths of careful power supply planning and design. For high volume applications, it is usually more cost effective to add a small winding to an existing power transformer (whether it be line frequency or switching) than to add an additional power transformer. None of these schematics are intended to show how the PHY power supply may be used to provide bus power. Notice that the PHYs shown in Figures 14, 15, and 16 are also powered from bus power (if the local node power is shut off).

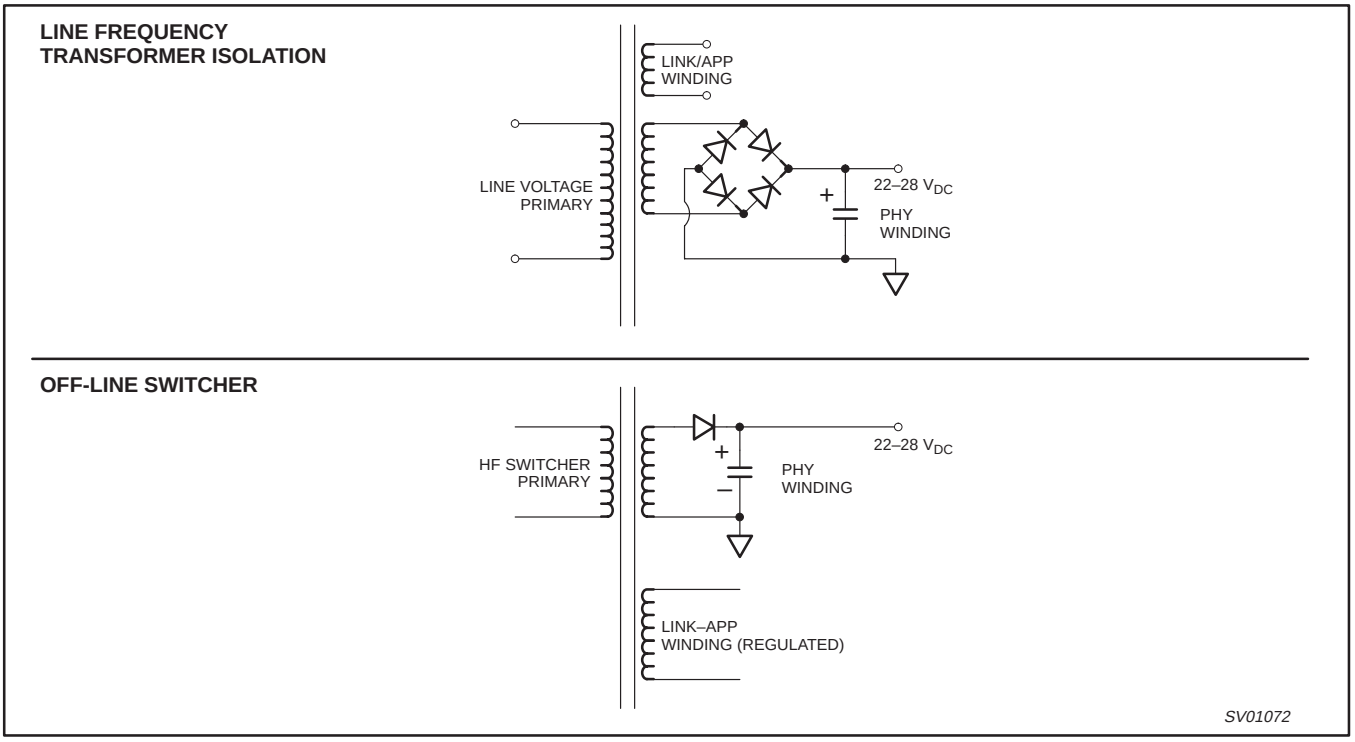

Figure 13. Two ways of developing isolated PHY power

Figure 13 depicts two ways of obtaining separate DC power systems from the AC line for nodes requiring galvanically isolated PHY circuits. The link and application layers of the node are powered from separate transformer secondary windings (in both examples). Typically, the link/application power winding in the switcher example is the one which is regulated. The PHY voltage is allowed to vary because there is a post-regulator supplied by that winding.

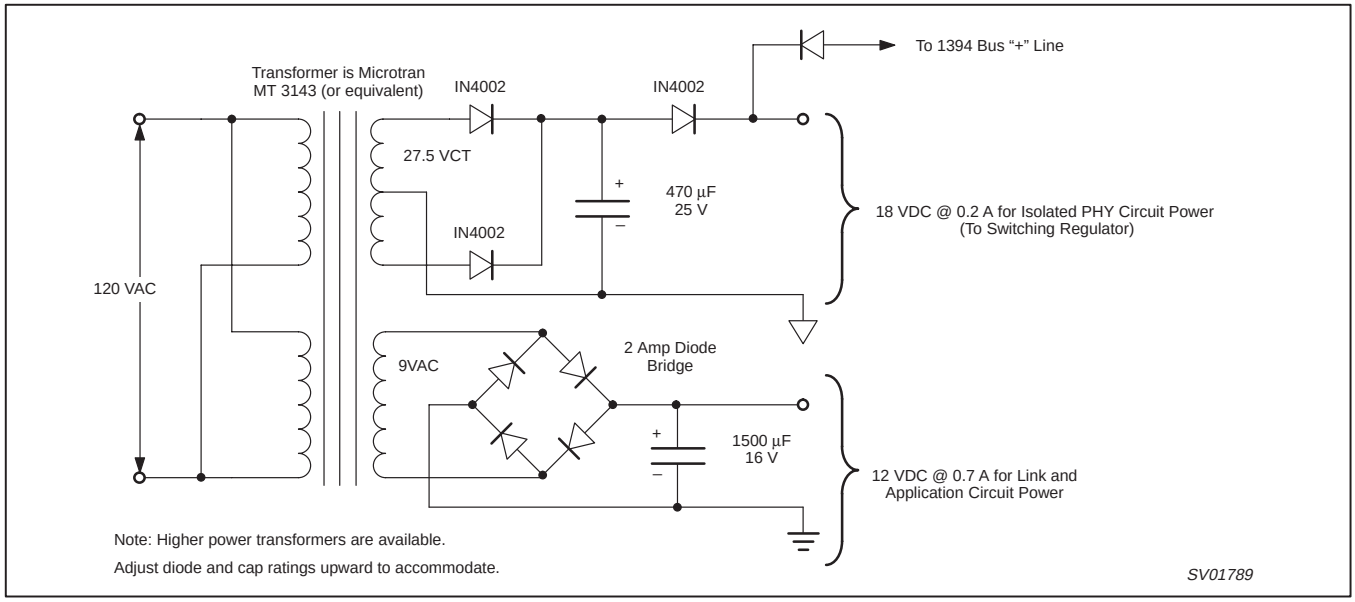

Figure 14. A practical method of supplying isolated PHY power and link/application power

Figure 14 shows a method of getting link/application power (about 12 VDC) from one secondary of a transformer, while obtaining about 18 VDC for PHY circuit power. This particular transformer is available from a variety of manufacturers and has the unique feature of providing two different secondary voltages. The PHY circuitry may also be powered from the bus through an isolating diode so that even if the transformer is powered off, the PHY will remain operational on bus provided power.

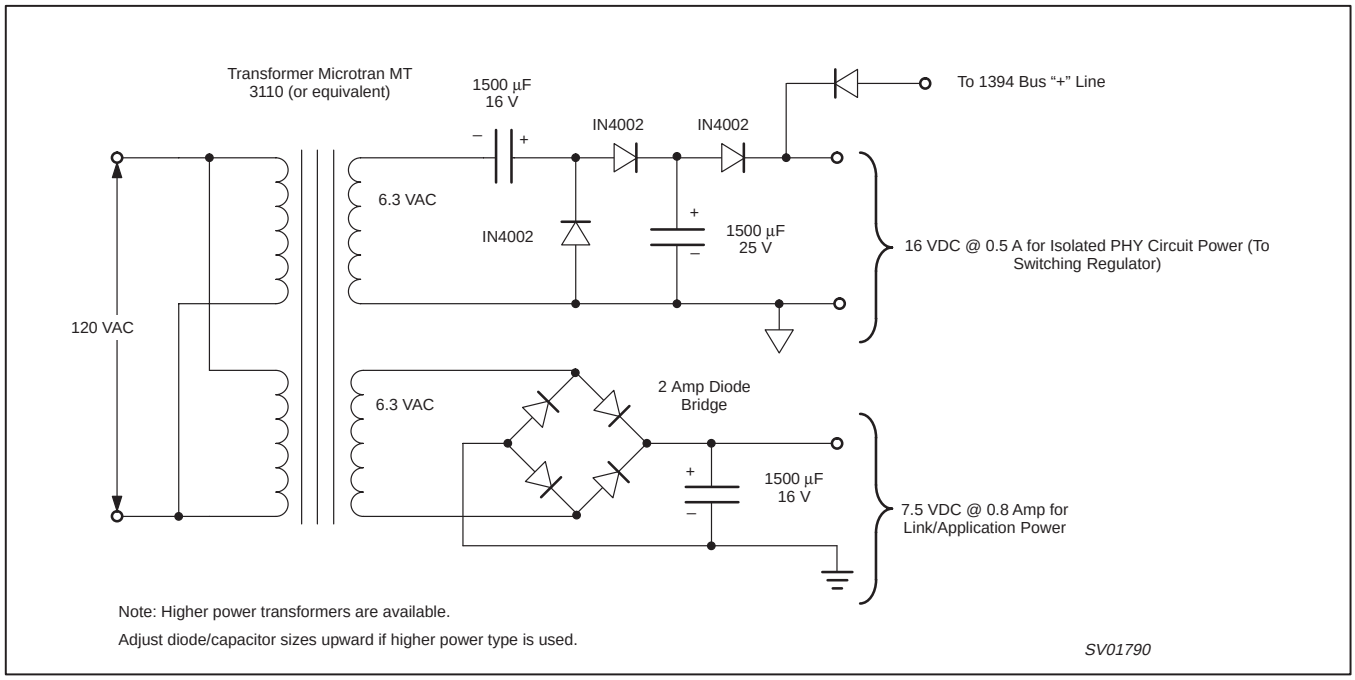

Figure 15. Low cost voltage doubler method of supplying isolated PHY power and link application power

Figure 15 shows how a low cost dual secondary transformer can be used to obtain link/application domain power while also supplying isolated PHY power.

The 6.3 VAC of the upper transformer secondary transformer is shown to be full-wave-doubled up to an output DC voltage of about 16 V. The 16 V at about 1/2 A is suitable for introduction to the input of a switching regulator to supply the 3.3 VDC PHY circuitry power. Note also that with the addition of a diode, bus power can also be used to power the PHY in case the application is powered down. The lower secondary of the transformer provides about 8 VDC to the link/applications domain for devices which require only 3 to 5 V for operation.

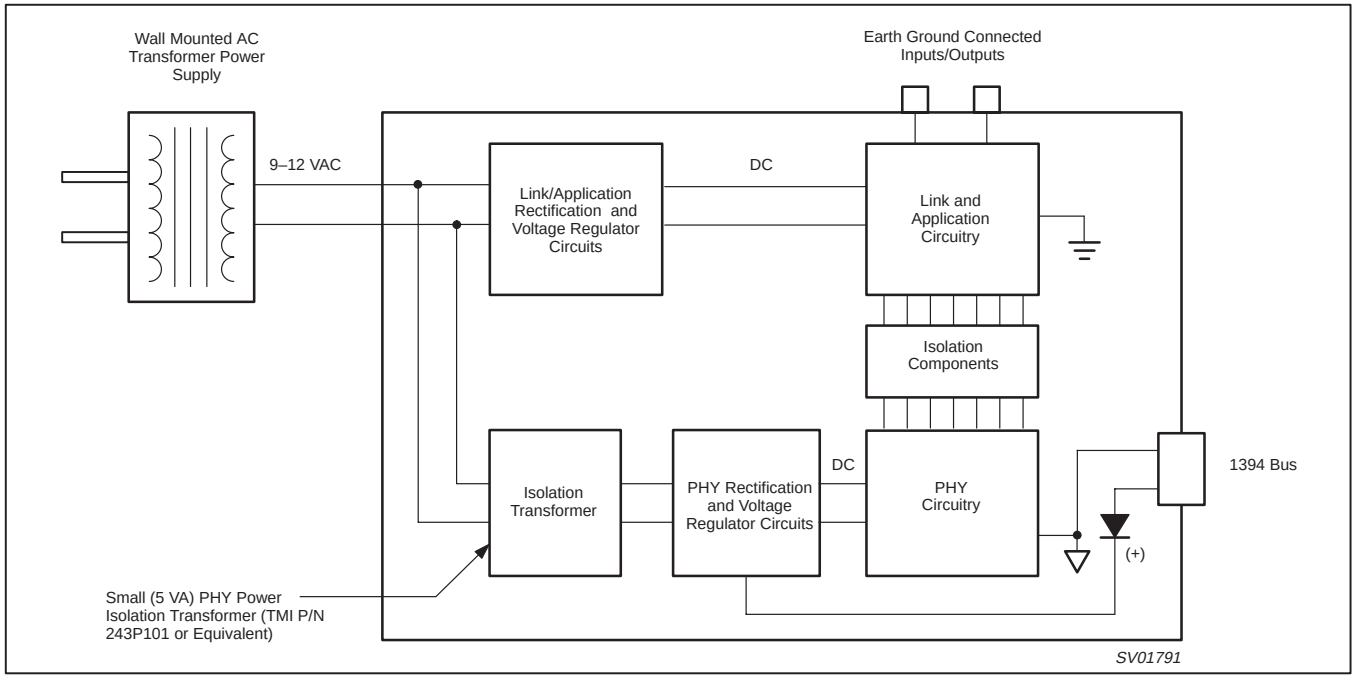

Figure 16. Method for obtaining PHY circuit power when an AC wall-mounted transformer supply is used for application power

Figure 16 demonstrates a method of coping with the need for isolated PHY power in an application powered by a wall-mounted single output AC power supply.

The 9 to 12 VAC from the wall transformer is introduced to the link/application domain circuitry for rectification and regulation to the DC voltages required in the domain. Also, in parallel, the AC voltage is directed to a small (low cost*) isolation transformer. The transformer takes the 9 to 12 VAC on its primary and outputs 15 to 20 on its secondary windings. This secondary voltage is rectified and regulated to provide the 3.3 VDC required by the PHY circuitry. The voltage regulator used may be either a linear type or switching type. If a switching type is used, bus power may be connected to the input of the switcher in order to power the PHY circuitry during application power downs (thus providing bus repeater functionality).

*TMI (Transformer Manufacturers, Inc., Chicago, IL) quoted $4 to $5 range in quantity as of the date of this Application Note. For further information, please contact TMI at: www.tmitransformers.com.

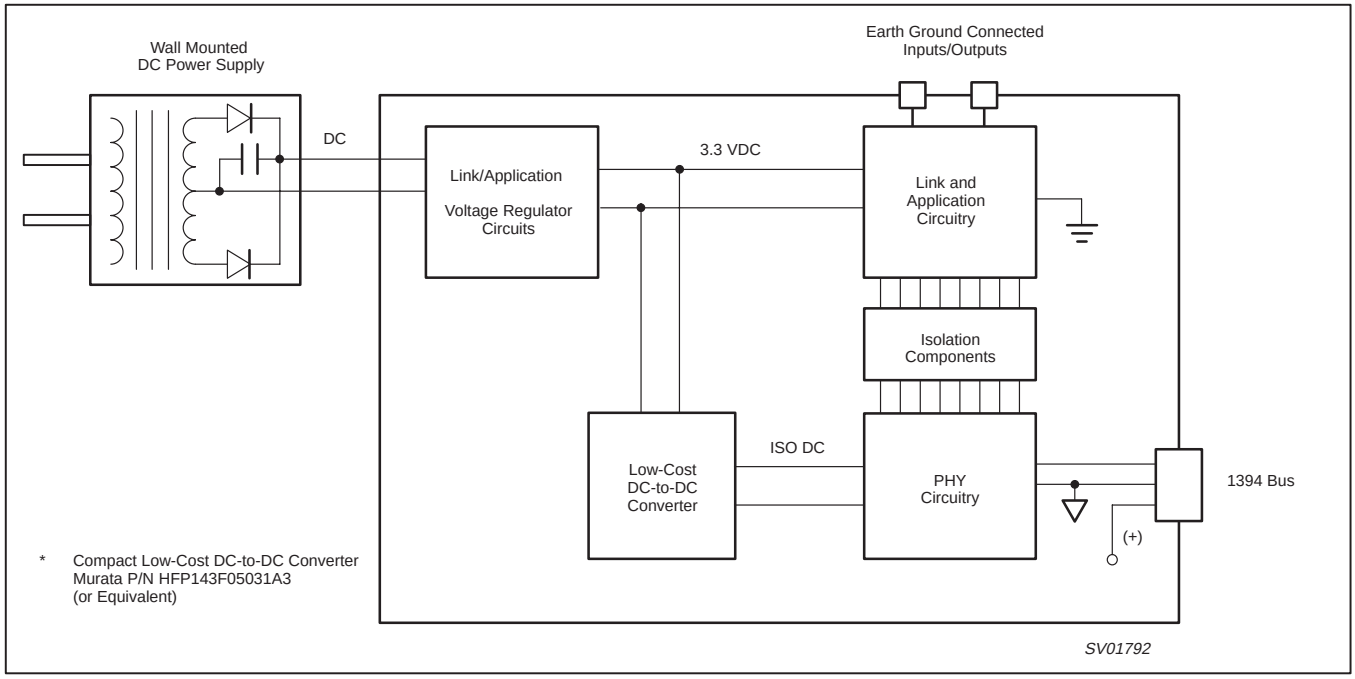

Figure 17. Method for obtaining isolated PHY circuit power when a DC wall-mounted supply is used

Figure 17 shows a method of coping with the need for isolated PHY power in an application powered by a wall-mounted, single output DC power supply.

The unregulated DC power supply sends current to an on-board switching regulator supply which, in-turn, reduces and regulates the voltage to the voltages required by the application and the link chip circuitry. The 3.3 V for the link chip can also be used to drive the input of a low cost* DC-to-DC converter such as the one shown in Figure 18. This particular converter has an isolated 3.3 VDC output which is capable of powering the PHY circuitry. Note that no bus power is either supplied or consumed in this design.

*Murata quoted $3.87 in quantity for this SIP packaged converter as of the date of this Application Note. For further information, please contact Murata Electronics at www.murata.com.

Table 1 shows various Link-PHY chip combinations and what sort of coupling should be used for each pin type in an isolated node design. The Pin Names are in the column at the left side of the chart. Across the top of the table are interfaces using the common names for the Philips parts. For example: L11 means the general part group PDI1394L11Bx, P11A means the general part group PDI1394P11Bx including P11 and P11A, etc. Select the interface used in your design and use the coupling method corresponding to each active pin type used in your design.

6. Do I need to supply power to the 1394 bus?

While it is not mandatory to supply power to the 1394 bus, it is often very desirable to do so. Supplying power to the bus is a way of assuring continued bus operation when a member node is shut off. It's also a good idea to allow the PHY to be powered from the node power supply or alternatively from the bus. If a node supplies bus power, it is expected to have the power available to the bus even if the node's link layer/application is powered down. Power may be supplied at levels of 15 watts, 30 watts or 45 watts, according to the standard. Typical power supply voltage levels are between 24 and 30 volts to account for bus cable line voltage drops. See the standard for details on when and how to supply bus power.
Figure 19 shows a block diagram of a way to supply isolated power to the 1394 bus. Supplying earth ground isolated power allows the PHY of this isolated node to use the power and also allows the node to supply other nodes on the bus. When supplying bus power be sure to set the power class bits of the PHY to the proper states to indicate how much power is being supplied to the bus. Also, please note the various cable shield to earth/chassis ground connections shown in Figure 19.

SUPPLYING ISOLATED POWER TO THE 1394 BUS

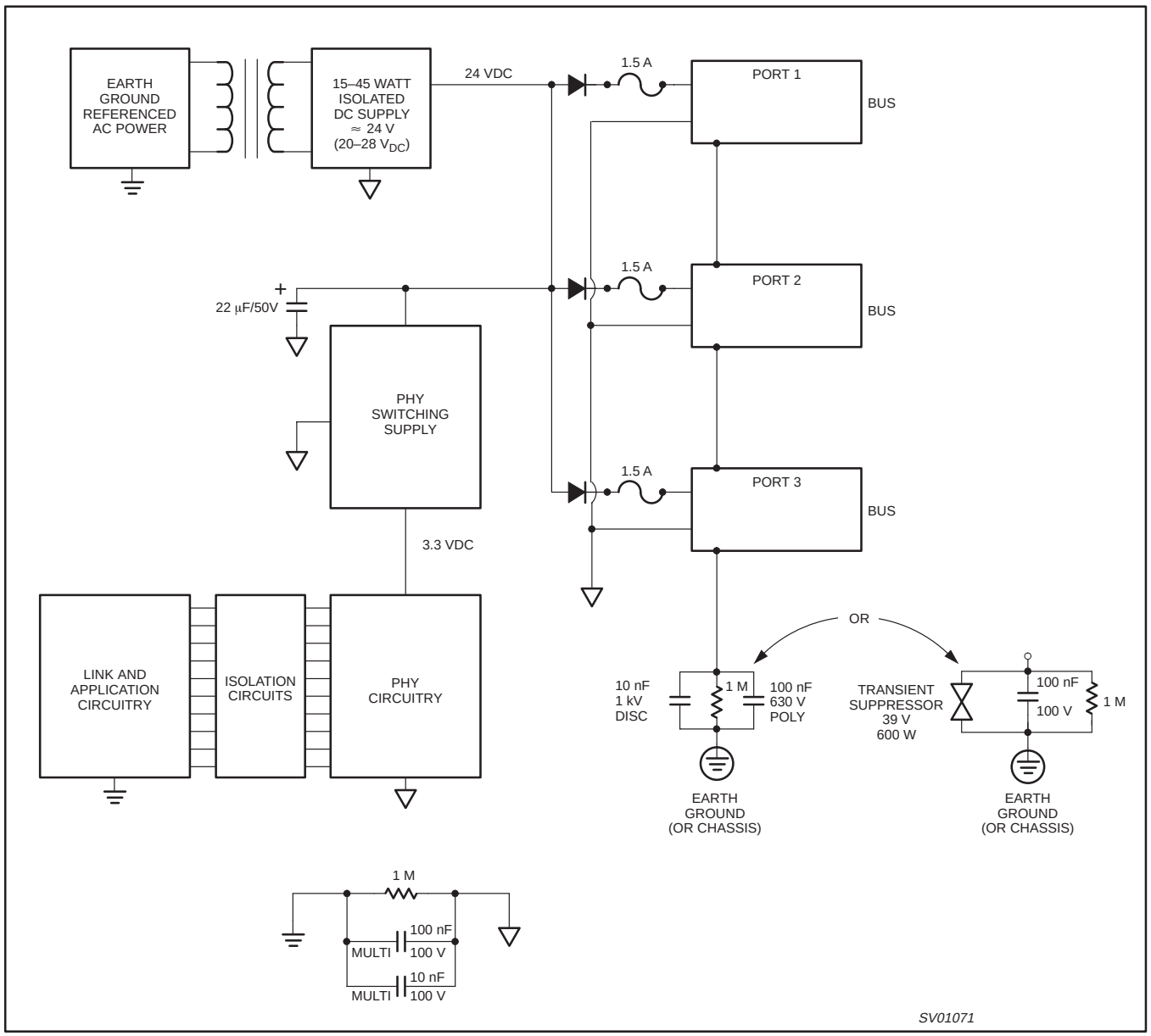

Figure 19. Supplying isolated bus power

Figure 19 shows a node which supplies isolated bus power. The 15 to 45 watt isolated DC is typically supplied by circuitry similar to that shown in Figure 13. Please note that the 24 V directed to the bus connectors is also supplied to the PHY regulator circuitry of the node in order to derive the 3.3 V DC PHY power. Two types of 1394 bus port shield terminations are shown. Due to the fact that the bus cable shield may be electrostatically charged, the use of robust capacitors (or transient suppression) is recommended. Capacitors used for link – PHY ground circuit coupling may be common 50 V types in most applications.

7. How do I use bus power to supply my PHY?

Most PHY chips consume 40 to 150 milliamps at 3.3 volts dc. This means that the typical PHY circuitry requires less than 500 milliwatts from a power supply. The fact that the PHY requires a 3.3 volt supply can sometimes be problematical. It would be easy to derive the 3.3 volts from a 500 mA linear regulator, but considering the power losses at high bus voltages (up to 4 watts at 30 v), it is usually wiser to employ a low cost switching regulator and avoid a design that requires heat sinking. Figure 20 shows a typical switching regulator system powering a PHY circuit. Through the use of the steering diodes D1 and D2, the node power supply or bus power (depending upon which has the greater voltage) will power the PHY. If the node power is removed, the bus power will allow the PHY to continue operating as a bus repeater, therefore maintaining the integrity of the bus.

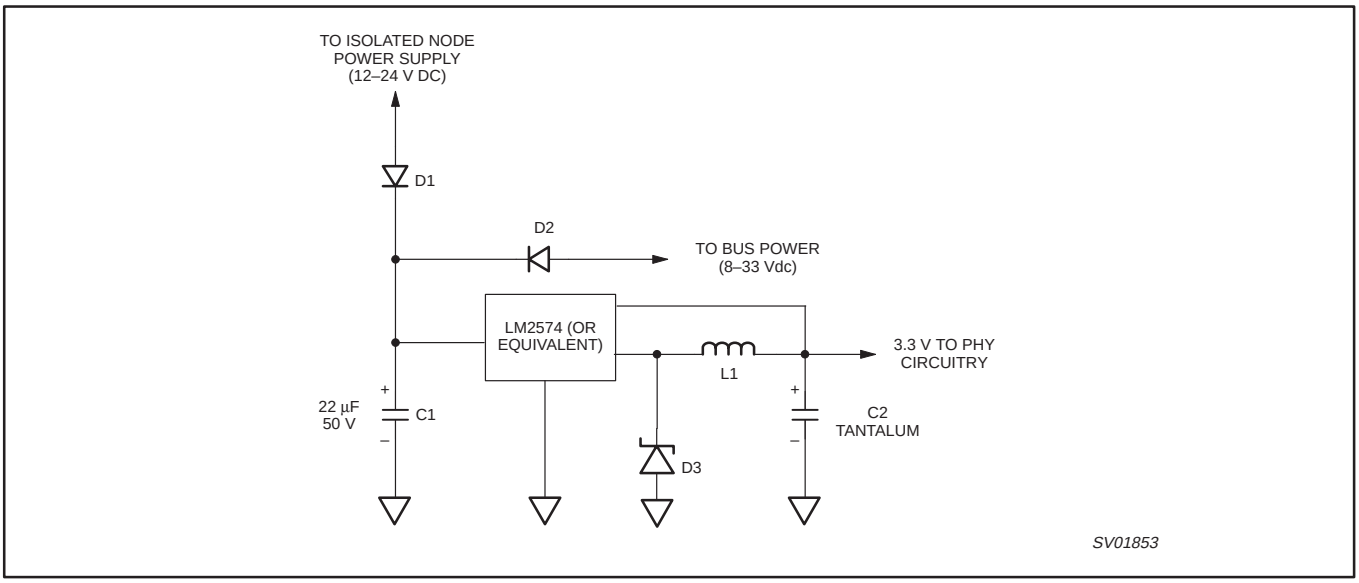

Figure 20. Using bus power to supply isolated PHY circuitry

SECTION 4: QUICK REFERENCE TO INTER-PIN COUPLING OF PHILIPS LINK AND PHY CHIPS

This section is provided as a distillation of data from section 2. It's meant to allow quick access to coupling methods used for various Philips links and PHYs. [If you interconnect a Philips link or PHY to another vendor's part, please email 1394@philips.com for information concerning application specifics.]

As an example, let's take the L21-P11A interface situation. The link chip is the Philips PDI1394L21 part and the PHY chip is the PDI1394P11ABx part. Data lines 0 to 3 are each coupled with a coupling capacitor (1 nF). Since the P11A PHY is a 200 Mbps part, link chip data lines 4 through 7 are not coupled to the PHY, but rather tied low through pull down resistors (10 kΩ). The PHY control lines (0 and 1) are coupled using a coupling capacitor (1 nF) on each line. LREQ and SYSCLK are also coupled using coupling capacitors (1 nF). The design should use an active PHY reset, the optical coupler circuit number 1 shown is recommended. The LINKON (LKON) function is not available on the L21 chip, so this pin on the PHY is not coupled to the link/application domain. Using LPS wired to the link power supply will require use of an opto coupler; circuit number two is recommended. Circuit number 2 is again recommended if the node design requires PHY to power down. And finally, if the node needs to know when other nodes on the bus are powered, we recommend coupling CNA to the link/application domain by means of opto coupler circuit number 3.

The use of optical coupling instead of a coupling capacitor on some of the link-PHY interface lines is required due to the slow (or DC) signal changes on these functions. As stated previously, the fast SYSCLOCK synchronized signals such as the LREQ and data bus lines have transition rates and equivalent frequency spectra which allow them to pass easily across the coupling capacitors. Optoparts are not used on the high frequency signals lines because they: 1) cost more, and 2) are not fast enough to faithfully communicate the signal from one domain to the other. We have attempted to make the link-PHY isolated interface as simple and as low cost as possible.

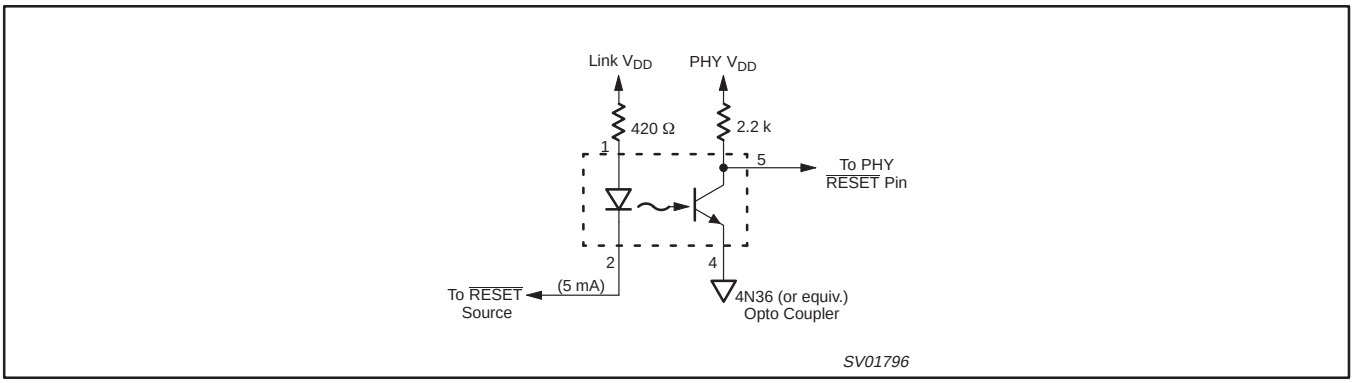

Figure 21. Optical coupler circuit Number 1

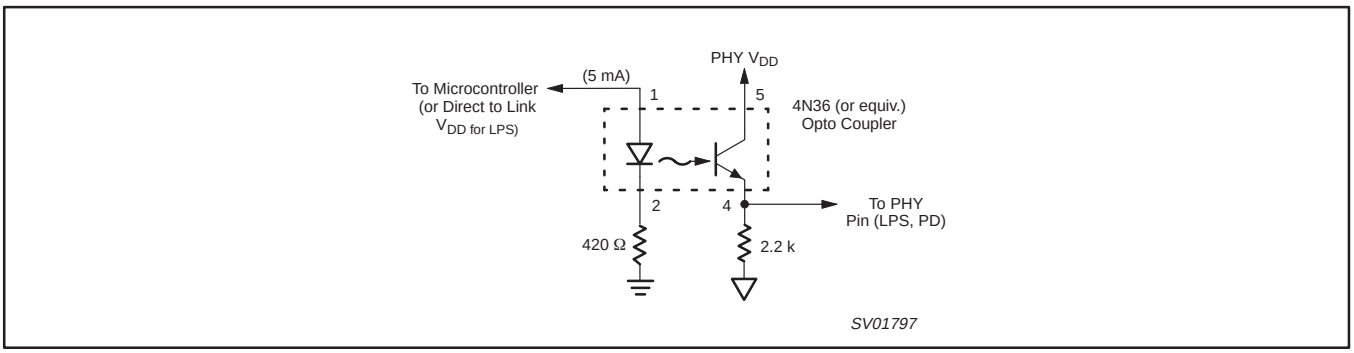

Figure 22. Optical coupler circuit Number 2

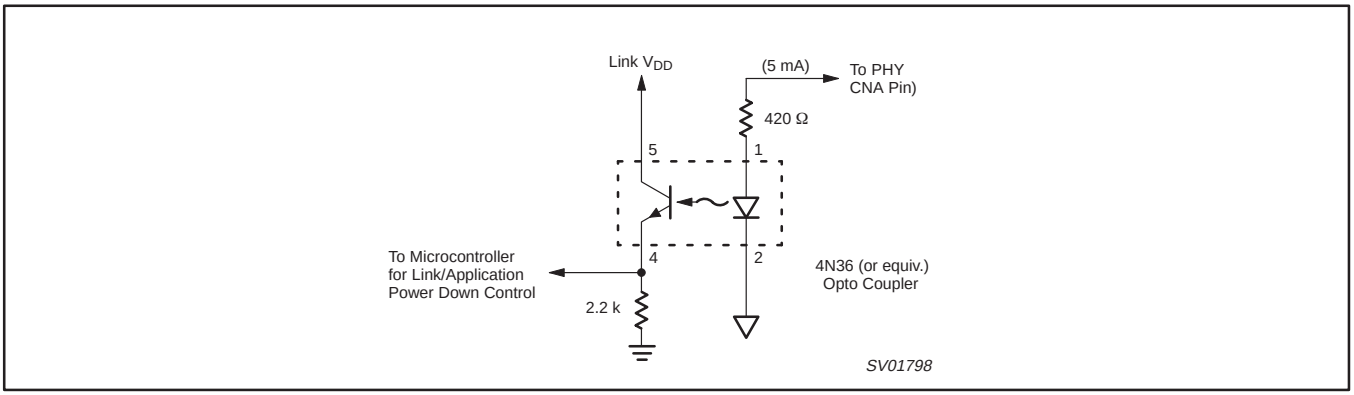

Figure 23. Optical coupler circuit Number 3

Isolated Link-PHY Interface

Table 1. Isolation options according to Link-PHY interface (Note: Set both Link ISO– and PHY ISO_N pins "HIGH")

Pin Name	L11 – P11A	L11 – P2x	L21 – P11A	L21 – P2x	L4x – P11A	L4x – P2x
D0 – D3	CC	CC	CC	CC	CC	CC
D4 – D7	NC	CC	NC	CC	NC	CC
CTL0, 1	CC	CC	CC	CC	CC	CC
LREQ	CC	CC	CC	CC	CC	CC
SYSCLK	CC	CC	CC	CC	CC	CC
RESET	OPTO1	OPTO1	OPTO1	OPTO1	OPTO1	OPTO1
LNKON	NC	NC	NC	NC	CC+	CC+
LPS	OPTO2	OPTO2	OPTO2	OPTO2	CCL+ or OPTO2	CCL+
PD	OPTO2	OPTO2	OPTO2	OPTO2	OPTO2	OPTO2
CNA	OPTO3	OPTO3	OPTO3	OPTO3	OPTO3	OPTO3
OTHER NOTES						
Use 39 K Ohm pull-down resistors on signal lines?	YES–YES	YES–NO	YES–YES	YES–NO	NO–YES	NO–NO
Minimum reset timing power-up	3 millisec	3 millisec	3 millisec	3 millisec	3 millisec	3 millisec
Hot reset (minimum)	100 µS	100 µS	100 µS	100 µS	100 µS	30 µS

CC = Coupling Capacitor (1 nF)

CCL = Coupling Capacitor (3.3 nF)

\+ = Resistor biasing circuit required (see Link and PHY data sheets)

NC = No Connection on Opposite Part

OPTO1 = Use optical coupler circuit number 1

OPTO2 = Use optical coupler circuit number 2

OPTO3 = Use optical coupler circuit number 3

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IEEE 1394 bus node galvanic isolation and power supply design

AN2452

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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