APPLICATION NOTE

AN242
Skew definitions

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INTRODUCTION

Skew specifications are like any other AC electrical specification. The measurements are taken at certain conditions which may or, more likely, may not match a specific condition in a system application. However, like other AC specifications the skew specification is valuable as a "bench mark" for estimating certain circuit characteristics. Skew specifications are most valuable in clock–driving applications and applications where duty cycle characteristics are important. Three specific skew specifications are addressed in this note.

Typical test conditions under which the skews may be tested are:

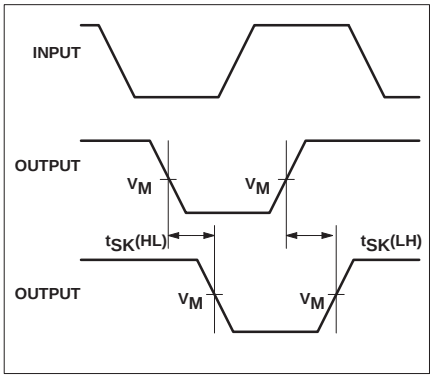
Test load: 50pF, 500Ω
All outputs switching
0°C, 25°C, 70°C
V_{CC} = 4.5V, 5.0V, 5.5V
Input conditions—V_{IL} = 0V to V_{IH} = 3V

Only data paths are tested for skew characteristics (AC measurements such as MR to output are *not* specified).

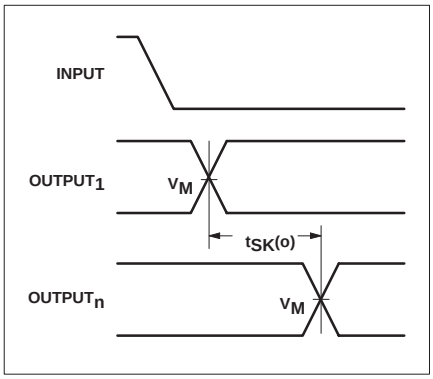
1. Output Skew $t_{SK}(o)$

JEDEC definition: "The difference between two concurrent propagation delay times that originate at either a single input or two inputs switching simultaneously and terminate at different outputs."

This skew generally characterizes like–going edges of a single IC only. It compares t_{PLH} versus t_{PLH} (or t_{PHL} vs. t_{PHL}) for two or more output data paths. This parameter is very useful in describing output distribution capabilities of a device. $t_{SK}(o)$ would be most valuable to customers using the device as a clock driver, distributing clock signals. $t_{SK}(o)$ could be further subdivided into $t_{SK}(LH)$ (output rising edge) and $t_{SK}(HL)$ (output falling edge) skews.



In some instances it may be necessary to compare opposite–going edges as in the case of complementary outputs driving positive–edge and negative–edge triggered clocks. Another case may be a need to simply compare t_{PHL} and t_{PLH} propagation delays on parallel paths.

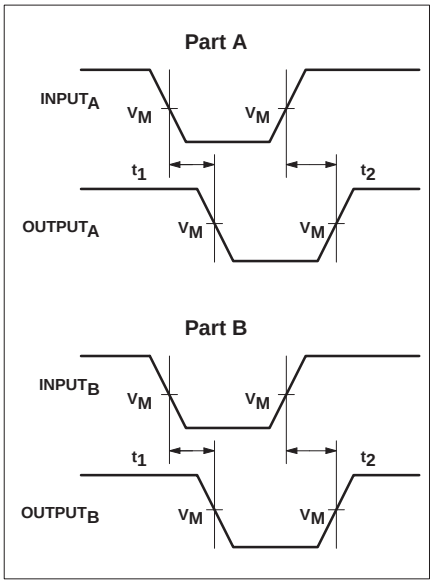


2. Process Skew $t_{SK}(x)$

JEDEC definition: "The difference between identically specified propagation delay times on any two samples of an IC at identical operating conditions."

This parameter addresses the issue of process variations by quantifying the difference between propagation delays that are caused by lot–to–lot variations. It does not include variations due to differences in supply voltage, operation temperature, output load, input edge rates, etc.

This parameter could be viewed as a $t_{SK}(o)$ skew over several like devices.

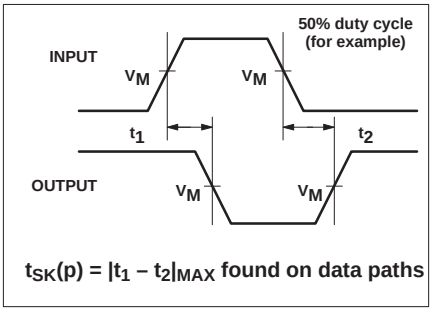


$t_{SK}(x)$ compares t_1 to t_1 and/or t_2 to t_2, etc., under identical conditions.

3. Pulse Skew $t_{SK}(p)$

JEDEC definition: "The difference between the propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch."

This parameter is used to quantify duty cycle characteristics. Some applications require a nearly perfect 50% duty cycle. $t_{SK}(p)$ specifies the duty cycle retention characteristics of the device.



$t_{SK}(p) = |t_1 - t_2|_{MAX}$ found on data paths

In essence this compares the input pulse width to the output pulse width—thus comparing the input duty cycle versus the resulting output duty cycle.

NOTES

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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