Interfacing 3V and 5V applications AN240

Authors: Tinus van de Wouw (Nijmegen) / Todd Andersen (Albuquerque)

1.0 THE NEED FOR INTERFACING BETWEEN 3V AND 5V SYSTEMS

Many reasons exist to introduce 3V[1] systems, notably the lower power consumption for mobile applications and the introduction of parts that use technologies with such fine geometries that 5V is simply not allowed any more.

The introduction of the 3V standard as supply voltage has resulted in many design activities for digital systems. Very often, however, there is a gradual transition from 5V to 3V, since not always are all required components available, or the system is rather complex so that 3V is introduced in part of a system. As an example, customers wish to use an existing and proven CPU, while a new, more complex ASIC with added features can only be made with 3V. Or vice versa!

With the introduction of new standards such as 2.2-2.7V or even 1.7V we expect that interfacing between systems that use different supply voltages will be an actual issue for many years to come. This application note specifically addresses the interfacing between 3V and 5V systems, but the results can be applied for interfacing between other voltage levels as well.

We will discuss how one can ensure reliable information exchange and how to prevent current flow between both supply voltages when interfacing logic with memories, ASICs, PLDs and microprocessors at different supply voltages.

2.0 LEVEL SHIFTING - INPUT AND OUTPUT LEVELS

We obviously want a reliable signal transfer from the 5V system to the 3V system and vice versa. This implies that the output voltages should be such that the input levels are exceeded.

2.1 TTL and CMOS Switching Levels

As a reminder, digital circuits have input levels defined: one voltage (V_{IL}) below which the circuit certainly sees it as a logical “0” and another voltage (V_{IH}) above which the input is guaranteed “1”.

Digital circuits normally come in two versions:

- TTL levels: V_{IL} = 0.8V, V_{IH} = 2.0V
- CMOS levels: $V_{IL} = 0.3 * V_{CC}$, $V_{IH} = 0.7 * V_{CC}$.
  For systems with $V_{CC} = 5.0 \pm 0.5$V this practically means:
  V_{IL} = 1.35V, V_{IH} = 3.85V.

2.2 Level Shifting from 5V to 3V

All 5V families have an output voltage swing that is large enough to drive 3V reliably. As described in Section 4.0, outputs may be as high as 3.5V for many “TTL” output stages, to the full 5V for many CMOS outputs. Therefore, as far as switching levels are concerned, there are no problems in interfacing from 5V to a 3V system.

2.3 Level Shifting from 3V to 5V

All 3V logic families deliver practically the full output voltage swing of 3V, so they can drive TTL switching levels without problems (see Fig. 1).

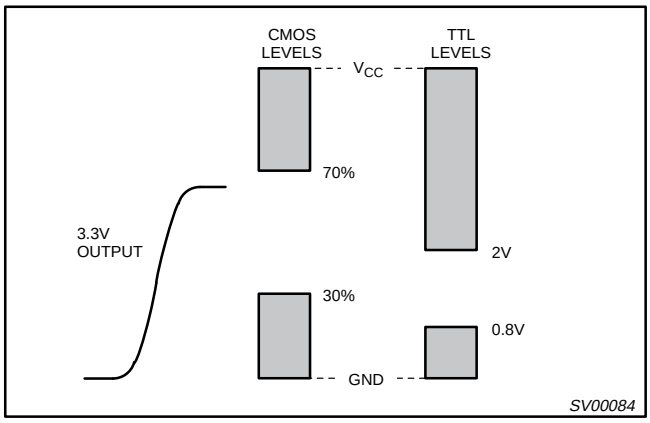


Figure 1. Switching Levels

One issue remains: a 3V system driving a 5V one that has CMOS input levels. This cannot be reliably done by standard 3V logic families, even when using pull-up resistors, simply because under worst case conditions, the output voltage is not high enough to guarantee that the signal will be seen as a logical “1”. Philips Semiconductors developed special dual V_{CC} levelshifters to address that situation (see Section 6.0).

3.0 INPUT STRUCTURES OF DIGITAL CIRCUITS

Before discussing further issues on 3-5V interfacing we should start by investigating the inputs of digital circuits in order to understand what care one should take to prevent problems.

3.1 ESD Input Protection Circuits

Virtually all inputs of a digital circuit contain an ESD protection circuit that prevents damage against electrostatic discharge. This circuit is present between the physical input pin and the active circuit. Two popular schemes are given in Fig. 2.

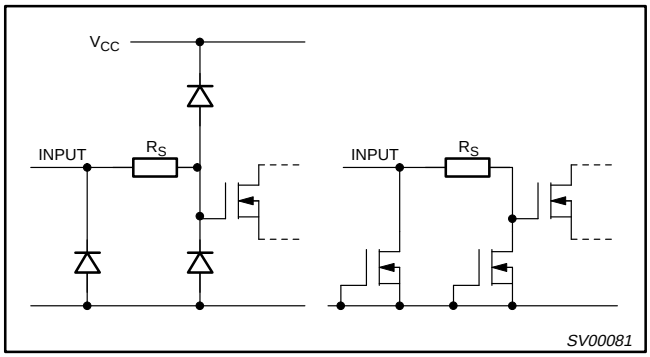


Figure 2. ESD Protection Circuits

The classic CMOS scheme as shown left provides protection against negative zaps by the diodes to ground. Positive zaps are clamped by the diode to V_{CC}. The real disadvantage is that the maximum input voltage of such a circuit is limited to V_{CC} + 0.5V. For a V_{CC} of 3V the allowed input voltage is too low for direct interfacing to most 5V systems.

1. We use the expression “3V” when a supply voltage is used between 2.7 and 3.6V.

Modern low voltage circuits use a double transistor circuit as shown right that was pioneered in our ABT families. Two transistors (Bipolar or MOS) act as fast Zener diodes protecting against positive zaps. Now, there is no diode to V_{CC} and the maximum input voltage is not limited by V_{CC}.

Typically, such circuits have a breakdown voltage between 7 and 10V, easily allowing input voltages from any 5V system.

LV is the only family that employs a classic protection circuit, all other Philips Semiconductors low voltage logic families have the dual transistor protection circuit.

3.2 Bus Hold Circuits

ALVC, LVC16 and LVT families use bus hold circuits as shown in Fig. 3. A bus hold circuit holds the input at the most recent value when the input is left floating by using a small MOS transistor as pull-up or pull-down device.

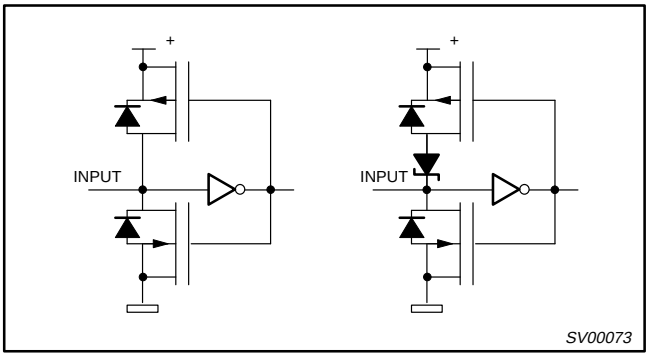


Figure 3. Bus hold circuits

A bus hold circuit for CMOS as shown left has also a diode between the input and V_{CC} which is formed by the intrinsic diode between the source and drain of the upper PMOS. This means that for ALVC and LVC16 the input voltage is limited to V_{CC} + 0.5V.

A different bus hold circuit is used in LVT parts as shown right due to the versatility of the QUBiC process which allows the use of a series Schottky diode so that there is no current path to V_{CC} in the bus hold circuit used for LVT.

4.0 OUTPUT STAGES OF DIGITAL CIRCUITS

Output structures of digital circuits (see Figs. 4 and 8) determine the output voltage swing. Circuits may swing between GND and V_{CC} or the swing may be limited by voltages developed internally.

Also, output structures determine the behavior when the output pin is taken above V_{CC}, which may be the case when two outputs are tied together on a common bus.

4.1 Bipolar Output Stage

A typical bipolar output structure does not have the full output voltage swing. When a 5V output is active HIGH, the output voltage is limited to $V_{CC} - 2 * V_{BE}$ (= approx. 3.6V). Therefore, quite often, interfacing with 3V systems works without currents flowing from the 5V supply into the 3V supply, or the current is so low that there is no real problem.

4.2 CMOS output stage

The output for a typical CMOS part swings fully between GND and V_{CC}.

One important point to note is that there is an intrinsic diode between the source and the drain of the upper PMOS as shown in Fig. 4. This may cause a current to flow from the output to V_{CC} when the voltage on the output pin is lifted higher than one diode voltage above V_{CC}.

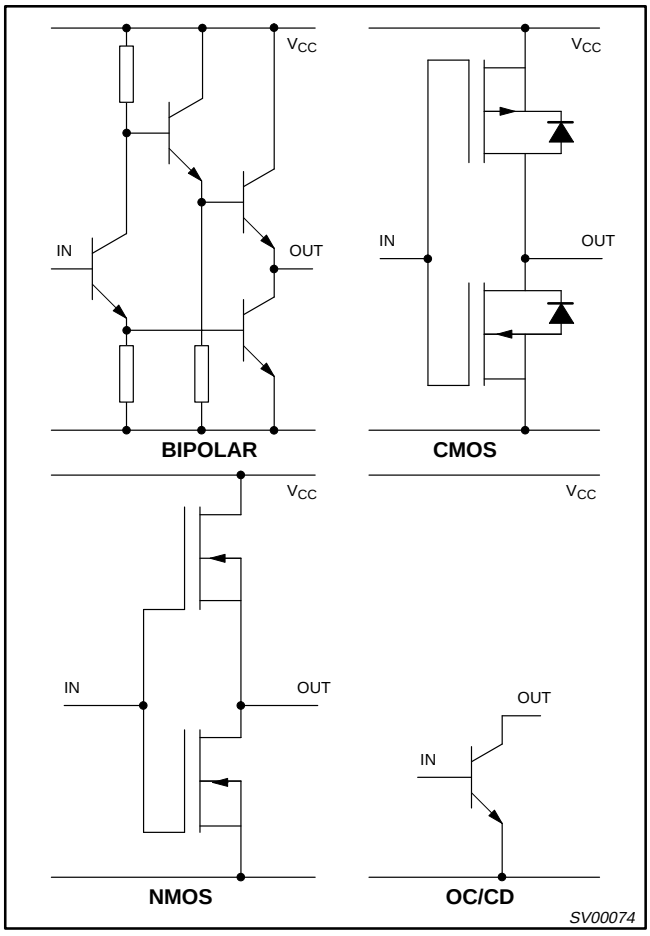


Figure 4. Typical digital output structures

4.3 Other MOS Output Structures

Some other MOS output stages such as many SRAM and DRAM circuits may have a circuit that shows a behavior similar to a bipolar output stage. An example is given Fig. 4: the upper NMOS limits the output voltage to $V_{CC} - V_{TH}$ (= approx. 3.5V). Such a circuit often works fine when driving 3V systems.

4.4 Open Collector/Open Drain

Some parts have an “Open Collector” or “Open Drain” output stage and there is no internal circuit to pull the output high. Normally a pull-up resistor connects the output to a voltage that can be higher than V_{CC}. Obviously such parts allow easy interfacing, but for speed reasons the pull-up resistor often needs to be relatively small, so the use of pull-up resistors increases power losses.

4.5 The BiCMOS Output

A BiCMOS output combines the advantages of bipolar (i.e. high output drive, low noise) and CMOS (full output voltage swing, low standby current). The output stage of Philips Semiconductors BiCMOS parts has some specific features that will be discussed in Section 6.1.

5.0 CURRENT FLOW FROM +5V TO +3V OR TO GROUND

A particular issue to address is the flow of current from the 5V power supply to the 3V supply. Then, the 3V supply may be charged up to a higher voltage which is potentially hazardous, affecting all connected 3V ICs. In addition the current provides extra power losses and may damage parts, although normally the driver capability is such that no damage occurs.

One other issue to study is the behavior of parts when either the 5V or 3V supply line is made 0V (suspend or power-down mode). In such a case high currents may flow from V_{CC} to ground.

5.1 Current Flow from the 5V Supply into a 3V Input

In mixed mode systems there is always data transmission from 5V to 3V. In such a case a 5V output drives a 3V input circuit. A potentially damaging current can only flow when two conditions are met: first, the 5V driver should be able to deliver current when the output voltage exceeds approximately 3.5V; second, the input circuit of the 3V part driven should have a current path from its input pin to V_{CC}. One has to carefully consider both aspects and check especially for a current path from the inputs of 3V parts to V_{CC}. Even with 5V parts that have limited output voltage swings, considerable currents may flow under worst case conditions.

5.2 Transceivers

The 3V part driven is often a transceiver, so the 'input' is effectively an input paralleled by an output. This means that the behavior of an output when its voltage exceeds V_{CC} is also important. More specifically, a CMOS transceiver has its output's intrinsic diode tied to V_{CC} that still provides a current path even when the part is in 3-State.

A similar situation may occur in the case of bus contention, when both outputs try to drive the bus HIGH. Fig. 5 shows the current paths via the active part and via the intrinsic diode of a CMOS output stage.

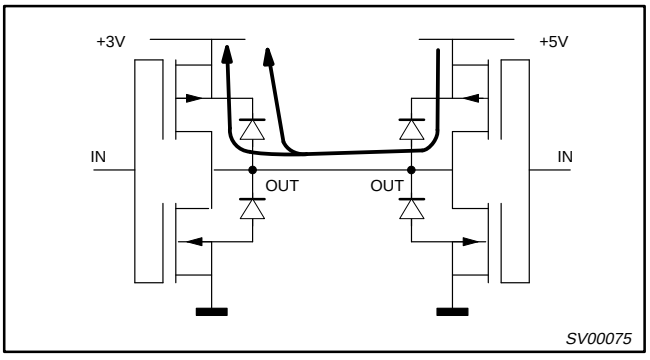


Figure 5. Currents from +5 to +3V

5.3 Suspend Mode or Power-down Mode

For energy savings parts of systems may be powered down, i.e., the supply voltage is made zero (called suspend mode or power-down mode) and the same observations can be made as above. In general, when a part allows 5V on its output under normal operating conditions, it also can withstand 5V on its output when V_{CC} is made zero. This is not always the case, however, especially for some competitive dual V_{CC} level shifters (see Section 6.1).

5.4 Summarizing Current Flow

When looking at unwanted currents from the 5V supply to the 3V supply, or in the case of suspend or power-down mode, we should study the following:

- The output capability of the driver (with V_{CC} = 5V)
- The input circuit of the driven part

When the driven part is a transceiver, we also have to look at:

- The behavior when the part is in 3-State: is there a diode to V_{CC}?
- Its output characteristics when the part is active HIGH in the case of bus contention.

6.0 PHILIPS SEMICONDUCTORS LOW VOLTAGE LOGIC FAMILIES

Philips Semiconductors has a wide range of logic families optimized for operation at 3V. Below we only discuss the properties for level shifting between 3 and 5V systems; other data can be found in the databook or brochures. In addition SPICE simulation models are available (see Section 7.0).

6.1 Main Interfacing Properties per Family

LV, which is derived from HCMOS, has a classical ESD protection circuit with a diode to V_{CC}; therefore its input interfacing capabilities are limited. The input voltage should not exceed V_{CC} + 0.5V (see Fig. 2 and Fig. 6) or the input current should be limited. As a result, one may use 5V outputs with a low drive capability as input for LV, or TTL outputs with a limited output voltage such as DRAM outputs described in Section 4.0. Obviously this is strongly dependent on the circuit layout of the driving 5V device.

LV has a standard CMOS output with a diode between the output and V_{CC}, so its output voltage is limited to V_{CC} + 0.5V.

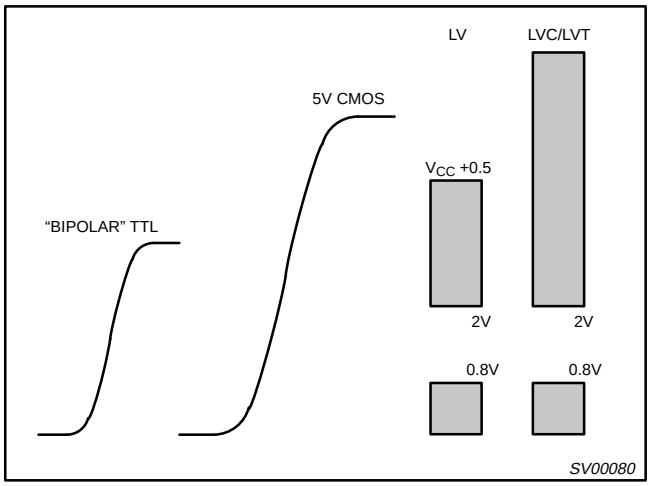


Figure 6. 5V Driving 3V

LVC has an input circuit without a diode to V_{CC}. Unidirectional devices, i.e., all parts that are not transceivers, can perfectly interface between 3V and 5V without any difficulty (see Fig. 6). Transceiver circuits, as described in Section 4.0, have a diode to V_{CC} in the output stage and have therefore limitations similar to LV.

The output voltage of LVC is limited to V_{CC} + 0.5V since it has a standard CMOS output with a diode between the output and V_{CC}.

Currently being introduced[2] is an enhancement to the LVC parts that have 3-State capability: 5V I/O tolerant (see Fig. 7). It works by dynamically tying the back gate to the highest possible voltage, either V_{CC} or V_{OUT}, such that the diode is never forward biased. This patented feature allows 5V on its output when the part is in 3-State. When the part is active HIGH, obviously there is still a current path from the output to V_{CC} via the active PMOS.

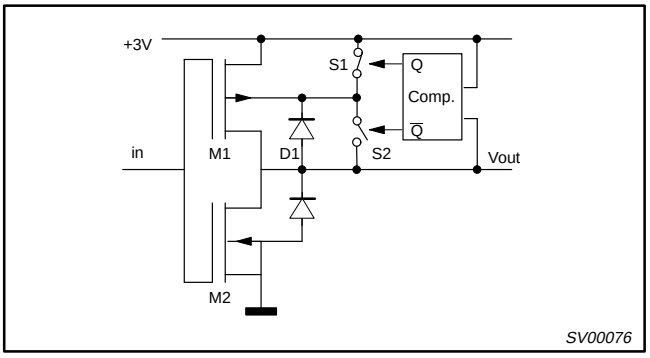


Figure 7. New LVC Output Structure

LVC16 parts have a bus hold circuit as described below under ALVC, limiting the 5V input tolerance to control pins only.

HLL behaves identical to LVC. Due to its high speed and high drive, the output is not 5V tolerant.

ALVC has an ESD protection circuit similar to LVC, but also employs bus hold circuits on its data inputs (i.e. not on its control inputs) as described in Section 3.2. Therefore, both unidirectional and bidirectional devices have the same limitations as LV. Its control inputs, such as OE and DIR, may be driven from both 3V and 5V. For speed reasons we do not plan a 5V tolerant version.

LVT uses QUBiC with its versatility in internal component options. LVT's bus hold has a built-in Schottky diode that prevents any currents from the input to $V_{CC,}$ as is the case for the bus hold used in ALVC.

In its output stage (see a simplified circuit in Fig. 8) the output diode to V_{CC} is eliminated using a Schottky diode, making LVT fully 5V compatible when the part is in 3-State.

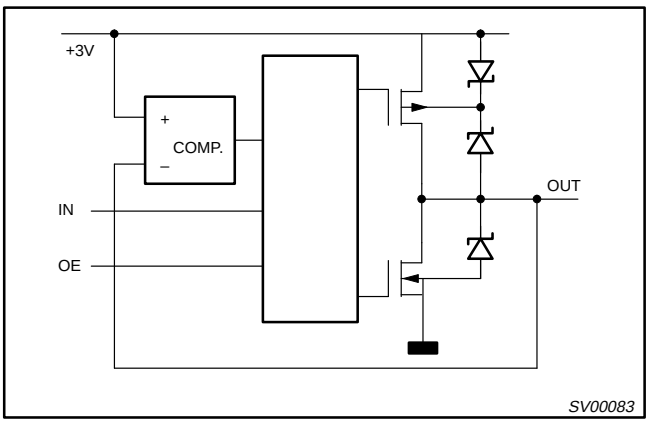


Figure 8. LVT's Output Circuit

Moreover, a special circuit has been incorporated that switches off the current path to V_{CC} when the output is pulled more than approximately 0.5V above V_{CC}. A comparator simply switches off the output stage, disregarding the state of the inputs and the control pins. This feature, called 'overvoltage protection', makes LVT fully 5V compatible and makes LVT the ideal choice for all sorts of mixed mode systems. There are no basic limitations in using LVT in mixed mode systems.

When the output voltage of LVT is lifted above V_{CC}, a current will flow, shown in Fig. 9. As one can see, where competitive devices have a current that can be considerable, a current of approximately 30mA is sufficient to toggle the overvoltage protection. The value of 30mA appears to be a good optimum to prevent noise signals from triggering the protection circuit. This implies that a simple pull-up resistor is not sufficient to pull the output into protection mode.

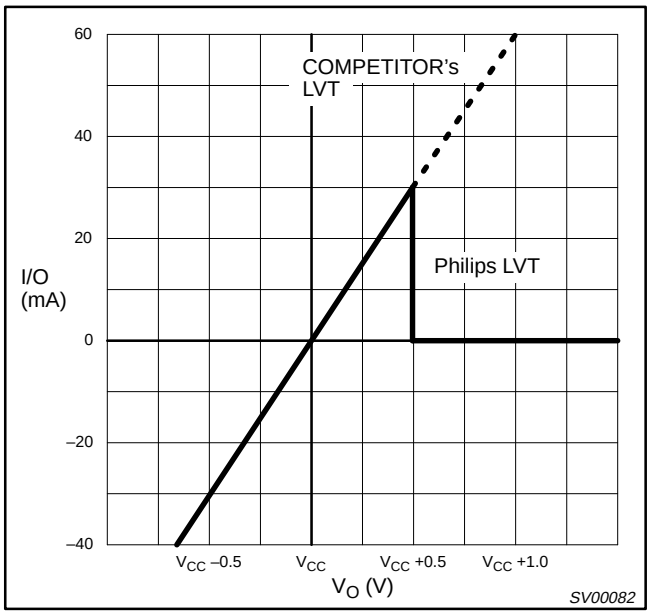


Figure 9. LVT I/O Current

It should be noted that this figure is valid when the output is active HIGH. When the output is in 3-State, no currents will flow.

Dual V_{CC} level shifters (74LVC4245 and 74ALVC164245, 8 and 16 bits resp.) are CMOS transceivers fed from both 3V and 5V supplies. The level shifting is done internally and the parts have full output voltage swings at both sides (see Fig. 10), making them ideal for level shifting purposes, especially when driving 5V CMOS levels.

2. First part available early 1996.

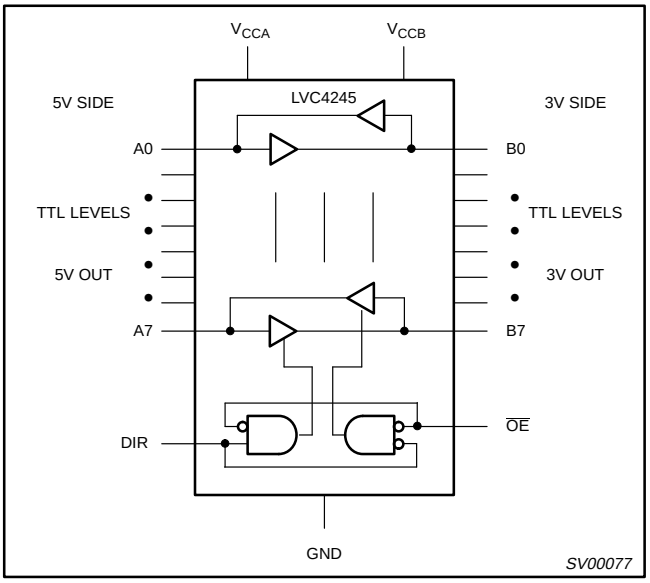


Figure 10. 74LVC4245

Dual V_{CC} level shifters are superior alternatives to the sometimes used input pull-up resistors, blocking diodes and other circuits that normally degrade speed and/or noise margins.

6.2 Summarizing Low Voltage Logic Interfacing Capabilities

Table 1 below sums up the input and output capabilities of our logic families and their behavior at suspend/power-down mode.

Table 1.

FEATURE	LV	LVC	LVC16 ALVC	LVT LVT16	DUAL V_{CC} LEVEL SHIFTERS
Drive 5V TTL levels	✓	✓	✓	✓	✓
Drive 5V CMOS levels	–	–	–	–	✓
5V on Input	–	✓	–	✓	✓[2]
5V on Control pins	–	✓	✓	✓	✓
5V on Output when in 3-State	–	–/✓[1]	–	✓	✓[2]
5V on Output when active HIGH	–	–	–	✓	✓[2]
Suspend/power down mode	–	–/✓[1]	–	✓	–

NOTES:
1. Feature to be introduced early 1996 for 3-State LVC parts.
2. Valid for side working from the +5V supply side when V_{CC} = 5V

6.3 Unidirectional Dataflow from 5V to 3V

Fig. 11 gives the situation for unidirectional data flow from 5V to 3V. Any 5V TTL part can basically drive the 5V tolerant inputs of LVC, HLL and LVT. The other families need a dual V_{CC} level shifter to prevent current flow from the 5V supply into the inputs of the 3V logic.

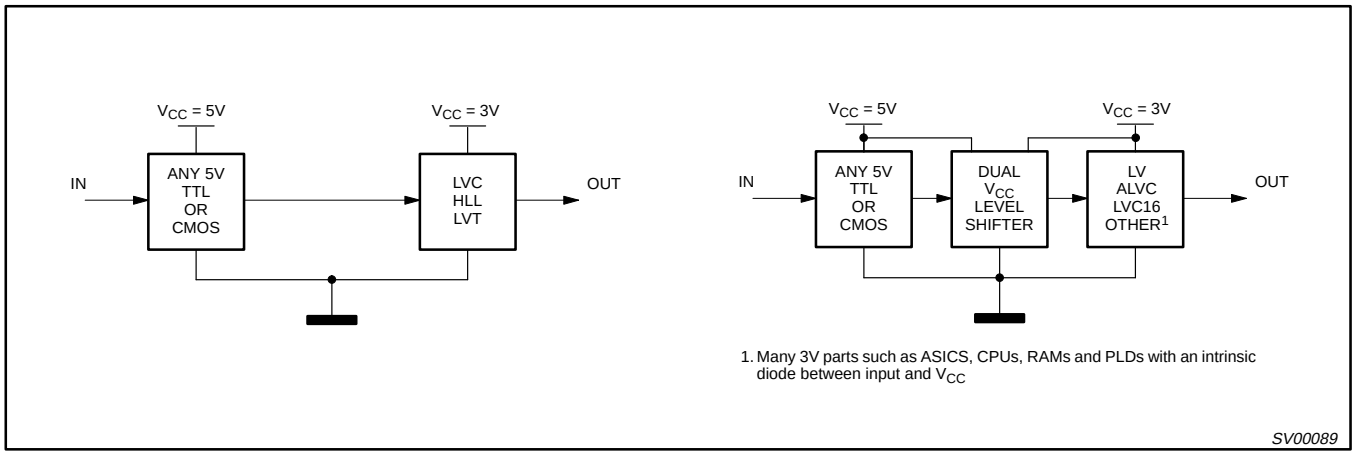


Figure 11. 5V Drivers to 3V Receivers

6.4 Unidirectional Dataflow from 3V to 5V

Fig. 12 Shows that driving 5V TTL can be done from any 3V logic family. When driving 5V CMOS levels, a dual V_{CC} level shifter is required to increase the output voltage swing.

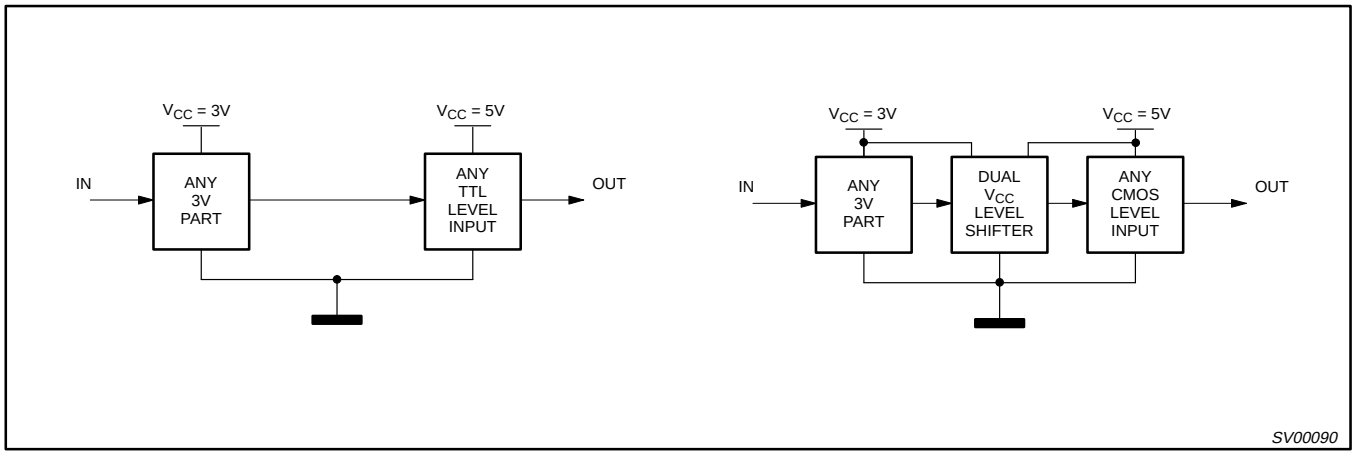
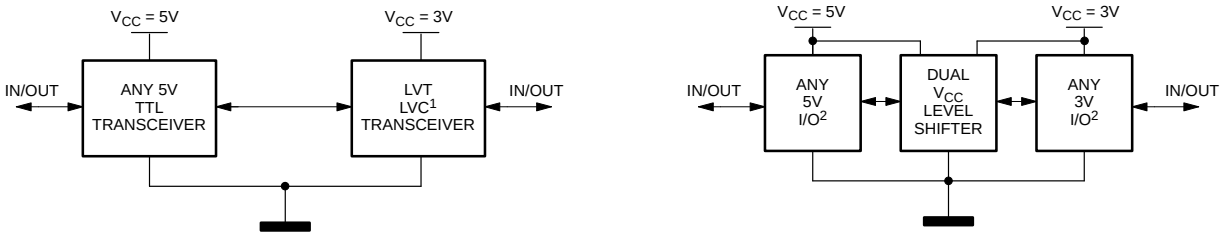


Figure 12. 3V Drivers to 5V Receivers

6.5 Bidirectional Data Communication Between 5V and 3V Systems

In many cases the data communication is bidirectional, both from 3V to 5V and from 5V to 3V. Parts that operate in both directions may be transceivers, but also other parts with a combined input/output (I/O), as shown in Fig. 13.



1. Revision to be introduced in early 1996

2. Combined input/output

SV00091

Figure 13. 5V Transceivers on Common Bus with 3V Transceivers

When either LVT or LVC with 5V tolerant outputs is used, a direct communication can be established between these and any 5V TTL level transceiver. When other low voltage families or parts with I/O are used, the dual V_{CC} levelshifters provide the transceiver function with built-in level shifting and preventing current flows between power supplies.

7.0 REFERENCES AND FURTHER READING

AUTHOR AND TITLE	ORDER NO.	ORDER NO. USA
Brian Martin, *Tips for straddling the 3V to 5V Fence* (EDN, Apr 4, 1994)	—	98 2902 010
Tinus van de Wouw, Rob Croes and Yong-in Shin, *Considerations for interfacing with Philips 3V HLL/LV with 5V ICs in mixed mode systems*, 1993	9398 706 29011	98 2902 003
Philips Semiconductors, Data Handbook IC24, *Low Voltage CMOS and BiCMOS families*, 1995	9398 652 71011	98 2902 002 02
Philips Semiconductors, *SPICE I/O models for 5V and 3.3V Standard Logic Families*, 1995	9397 750 00119	9397 750 00119

8.0 CONCLUSION

This report gives many details on how to properly communicate between 3V and 5V systems. Special characteristics of Philips Semiconductors low voltage logic families often allow easy and worry-free translation of data from one system to the other.