

APPLICATION NOTE

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74FXXX “Light Load” input products

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Major "Light Load" Input Features

- Patented "Light Load" NPN input structure
 - Normal Input pins = $\pm 20\mu\text{A}$ per input
 - Transceiver I/O pins = $\pm 70\mu\text{A}$ per I/O pin
 - Primarily capacitive loading = $< 10\text{pF}$
- Ideal for MOS CPU, peripherals, and semi-custom bus interfaces
- Patented turn-OFF speed-up circuit
- No significant speed disadvantage – standard 74F speeds
- PC board transmission line drive capability: $-15/64\text{mA } I_{OH}/I_{OL}$
- "Broadside" design in 20-, 24-, and 28-pin slim-DIP packages
- "Light Load" family includes:
 - 19 Buffers and line driver parts
 - 19 Shift register, register and latch parts
 - 19 Transceivers (no storage)
 - 8 Dual registered transceivers
 - 7 Arithmetic functions

Introduction

The Philips Semiconductors 74F "Light Load" product line is a high performance, TTL bus compatible series of very low input bias current ($\pm 20\mu\text{A}$), buffer/driver, transceiver, register, multiplexer and arithmetic MSI functions. The patented "Light Load", $\pm 20\mu\text{A}$ NPN input structure, shown in Figure 1, combined with a unique input speed-up circuit (also patented) makes this product line ideal for interfacing with all MOS devices, without any speed degradation. When compared to the I_{IL} of standard FAST inputs of $600\mu\text{A}$ (larger for some other logic families) this "Light Load" input shows a 30:1 reduction in I_{IL} loading ($600\mu\text{A}/20\mu\text{A}$).

These devices were specifically designed to meet the requirements of buffering low output drive MOS VLSI/LSI devices from the rigorous loading environment PC board/motherboard buses and system backplanes. The "Light Load" inputs and improved speed performance make this product line ideal for interfacing to low output drive capability, slower MOS CPU, peripherals and semi-custom chips used in most state-of-the-art logic designs today. Using these "Light Load" input bus products, MOS chip outputs will only have to drive the small amount of distributed PC trace capacitance and inductance loading. The MOS device output drive capability is not wasted on drivers/transceivers with large DC input current drive requirements.

See Table 1 for a complete listing of the part numbers and functions of the "Light Load" product line.

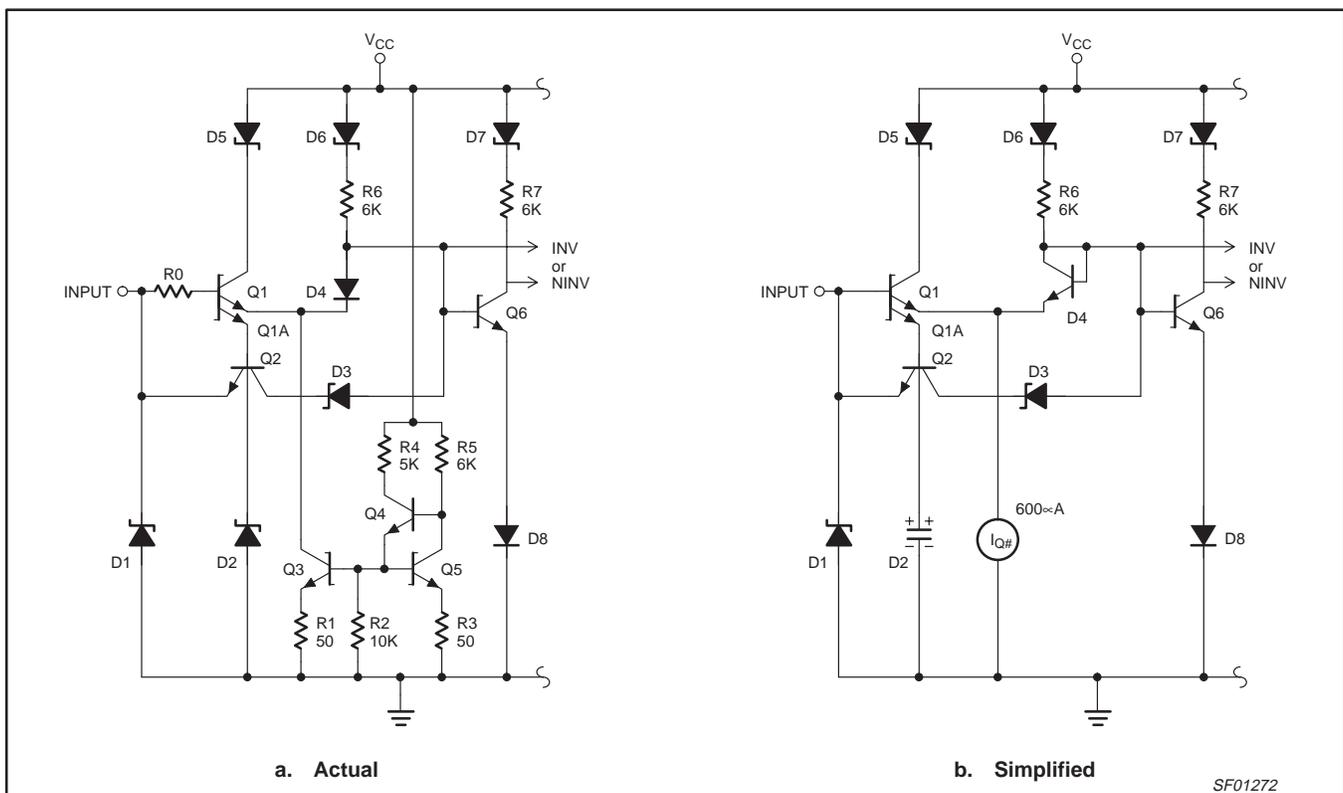


Figure 1. The "Light Load" and Speed-Up Circuit Input Structure (Actual & Simplified)

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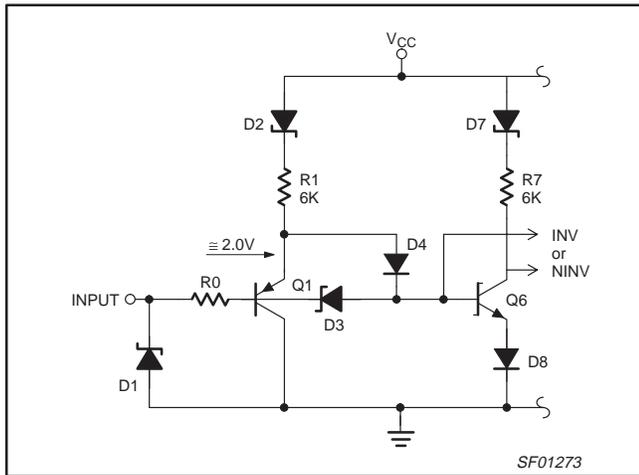


Figure 2. Future "Light Load" PNP Input

"Flow-Through" Design

Figure 3 illustrates the pin configurations of the 74F84X Latched Buffer series. Notice that all of the "Light Load" input data bus products use a "Flow-Through" design which allows logic signals to flow into one side and out of the other without crossing or folding back on signal paths such as the 74F24X octal series. Comparing the physical PC board signal bus path layout required for the 74F845 Octal Registered Buffer to that of the zig-zag signal path of the 74F240 Octal Inverting Buffer, you will see the significant advantages of this product line's "Flow-Through" design in simplifying the design and layout of large, bus-oriented PC boards.

The "Light Load" input product line combines "Flow-Through" design, high speed performance and high functional density into 20-, 24-, and 28-pin, 300-mil Slip-DIP packages significantly reducing system propagation delays, parts count, power dissipation, PC board area/complexity and, therefore, total cost while enhancing total system reliability.

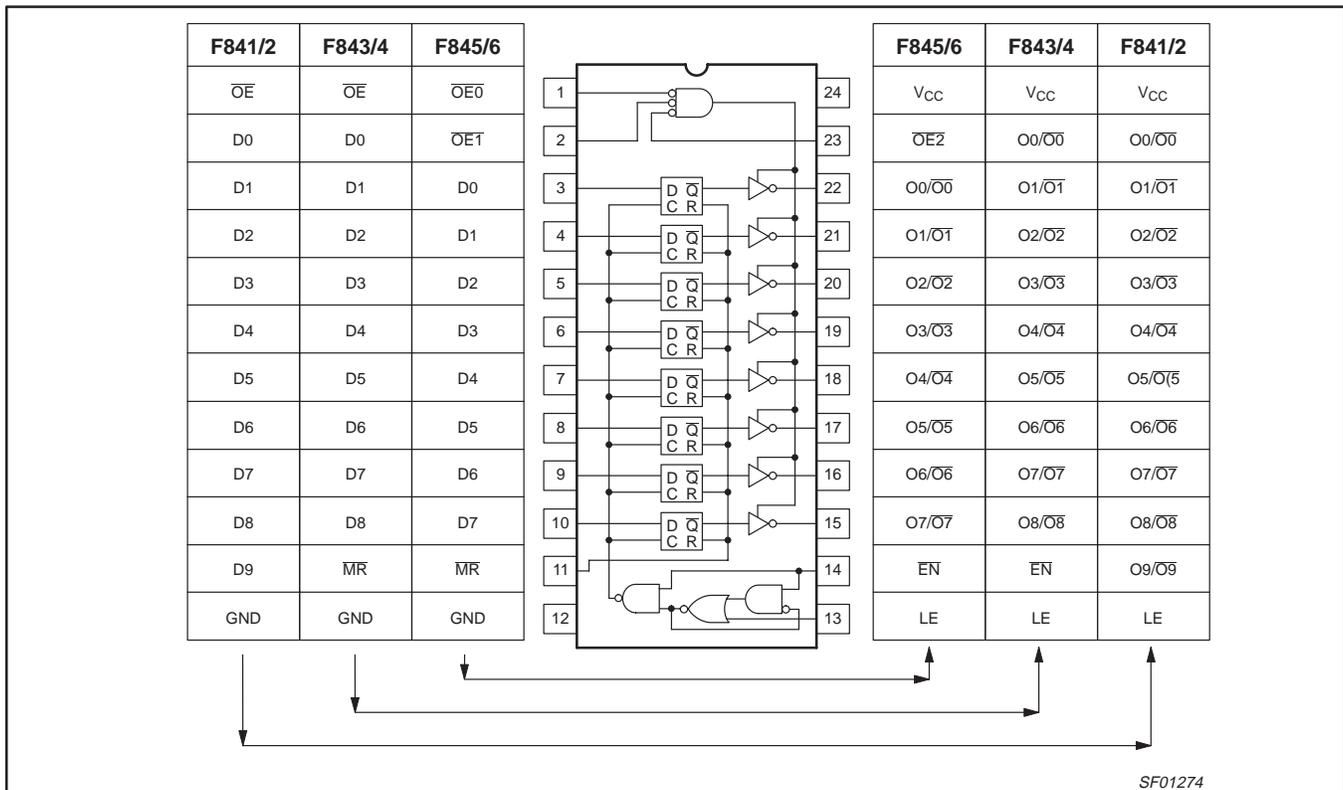


Figure 3. 74F84X Latched Buffer Pin Configurations

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Input Structure – Differential Amplifier

Figure 1 shows the circuit diagram of the patented “Light Load” NPN input (Q1/3, R6, & D4) and the Turn-OFF Speed-Up circuit (Q2, D2, & D3). This input structure is actually a linear differential amplifier consisting of Q1, D4 and a constant current sink made up of Q3/4/5 and R1/2/3. The input bias current of this amplifier is less than $\pm 20\mu\text{A}$ for V_I between 0.0V and 5.5V. The Turn-OFF Speed-Up circuit (D2/Q2/D3) quickly discharges Q6's base-collector stored-charge to ground. The following analysis assumes room temperature and 5.0V_{CC} operation.

The Q1's base is the input side of the differential amplifier and D4's anode is the reference side. When the input is HIGH (2.0V), Q1 is turned-ON and I_{CE} plus I_{BE} current flows into Q3's constant current sink network of $\sim 600\mu\text{A}$. Since D4's anode is clamped at 1.3V to 1.4V by the V_{BE} of Q6 plus D8's voltage drop, and since Q1's emitter voltage is pulling the cathode of D4 up to greater than $\sim 1.4\text{V}$ (the 2.0V_{IH} minus Q1's 0.6V_{BE}), R6's (6K) current cannot flow through D4 and forward biases Q6's base-emitter.

Since Q6 is a Schottky clamped transistor, it has a $V_{CEsat} \sim 0.5\text{V}$. When Q6 is turned-ON by R6, the voltage at its collector drops to $\sim 0.9\text{V}$ from ground (adding in D8 voltage drop), which turns-OFF the output totem-pole pull-down driver transistors and turns-ON the pull-up. This topic will be discussed in more detail in the next section (refer to Figure 4).

Input Structure – Constant Current Sink

The constant current sink produced by Q3/4/5 and R1/2/3/4/5 sinks a relatively constant $600\mu\text{A}$ to ground. This “current mirror” circuit drives the base-to-ground voltage of Q3 and Q5 to $Q5 V_{BE}$ plus the voltage drop across R3. Since Q3 and Q5 are identical, the voltage drops across R1 will equal that of R3. Therefore, the current through R1 equals the current through R3 times the ratio of R3:R1.

The base bias currents for Q3 and Q5 is supplied by Q4. Because of the relatively high β s of Q3 and Q5 (>50), their base currents of $\sim 10\mu\text{A}$ do not significantly effect the currents through R3 and R1 (β or BETA = transistor current gain). At 25°C and $V_{CC} = 5.0\text{V}$, R3's current is approximately equal to:

$$I_{R3} = [V_{CC} - (V_{BE-Q4} + V_{BE-Q5})]/(R3 + R5)$$

$$I_{R3} = (5.0\text{V} - 1.2\text{V})/(50\Omega + 6000\Omega) \cong 600\mu\text{A}$$

Therefore:

$$I_{CE-Q3} \cong I_{R1} = I_{R5} \times (R3/R1) \cong 600\mu\text{A}$$

With Q1's β also greater than 50, the HIGH logic level input bias current is less than $20\mu\text{A}$:

$$I_{OH} = I_{CE-Q3}/\text{BETA}_{Q1} \cong 600\mu\text{A}/>50 < 12\mu\text{A}$$

The “Light Load” PNP Input

We will soon be introducing a new product line of “Light Load” PNP devices. One of the first products will be the 74F821 through 74F826 Registered Buffers, which will have the same pin configurations and options as the 74F841 through 74F846 Latched Buffers (see Figure 3). The 74F82X series will provide a positive-going edge triggered clock input to its 8-, 9-, and 10-bit register storage parts versus the 74F84X series' HIGH level Latch Enabled latches.

With Philips Semiconductors latest oxide-isolated process, a new, high performance “Light Load” PNP input structure will soon be available. This new PNP input, shown in Figure 2, provides a high impedance AND input structure versus the NPN input OR input and reduces the chip power dissipation by eliminating the requirement for a constant current source for each input.

The PNP input is still a differential amplifier with the cathode of D3 referenced to $2 V_{BE}$ voltage drops from ground. When the input is HIGH ($V_{IH} \geq 2V$), no Q1 emitter-base current can flow because the anode of D3 is clamped to the $2 V_{BE}$. As D4 forward biased with the current from R1, the output driver transistor (Q6) turns ON. When the input is LOW ($V_{IL} \leq 0.8\text{V}$), Q1's emitter-base junction is forward biased, which turns ON the β amplified emitter-collector current of Q1. When Q1 is ON, the anode of D4 is clamped OFF by the input V_{IL} voltage plus Q1's emitter-base drop ($V_{IL} + Q1 V_{BE} \leq 0.8\text{V} + 0.6\text{V} = 1.4\text{V}$). Therefore, the input threshold at the base of Q1 is $\cong 1.4\text{V}$ ($2 V_{BE}$) at 25°C.

With the β of Q1 typically greater than 100, the V_{IL} input bias current is guaranteed to be less than $20\mu\text{A}$. With the input HIGH, the input leakage is also guaranteed to be less than $20\mu\text{A}$. The β amplification of Q1 is basically the only difference between this PNP input's $20\mu\text{A}$ I_{IL} and the standard diode input's I_{IL} of $600\mu\text{A}$.

When the base of Q1 is switched LOW, the Schottky diode D3 provides a turn-OFF speed-up path to ground, which quickly discharges the base of the driver transistor (Q6).

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Output Structures

A characteristic example of the output structures found throughout the 74FXXX Light Load product line is the 74F657 Parity Bus Transceiver, which has two basic output designs. Figure 4 illustrates the 74F657's output structure designs of these output structures: A_N Port's output (Figure 4b) is guaranteed to handle -3/+24mA (2.4/0.55V V_{OH}/V_{OL}), and the B_N Port (Figure 4a) can drive greater than -15/+64mA (2.0/0.55V V_{OH}/V_{OL}). The A_N Port is designed to drive the chip side of the PC board to backplane interface, while the B_N Port is capable of driving PC board data transmission lines and backplane signal line with a characteristic impedance as low as 70Ω.

Referring back to Figure 1a, the base drive current for Q9/10/11 comes from either R6 for an inverting output or R7, if the output is non-inverting. For the inverting case, D4 is back-biased when the base voltage applied to Q1 (≥2.0V_{OH}) and Q9 base drive is supplied from R6. Q9's base is clamped at the sum of base-emitter forward biased voltage drops of Q9/10/11 and Q12. Q12's base drive primarily comes from R10/11/12 when Q9/10/11 are ON.

When Q9/10/11 begin to turn-ON, the base drive for Q12 must first overcome the R13/D13 base clamp before current can flow into Q12's base. During the output voltage HIGH to LOW transition, this delay minimizes totem-pole feed-through current into the ground lead by allowing the collector of Q11 (Phase Splitter Transistor - Q_{PS}) to pull down toward 1 V_{BE} + 1 V_{CEsat} and, thereby, turning-OFF the Q13/14 Darlington totem-pole output pull-up driver before Q12 completely turns-ON.

When the gate input switches from V_{IH} to V_{IL} (≤ 0.8V), the charge stored in D2 discharges through the base-emitter of Q2. Q2 (through D3) quickly pulls the bases of Q9/10/11 toward ground. When the collector of Q9 rises high enough (-1.3V) to forward bias the Q12

base clamping network of D9/R8/R9/Q7/Q8, Q12 is quickly turned-OFF before the Q13/14 totem-pole pull-up can turn-ON. This design minimizes feed-through ground during the output voltage LOW to HIGH transition.

The 3-State, totem-pole output structures of both the A_N and B_N ports have Schottky blocking diodes, D15, in their pull-ups. Their purpose is to block leakage current from flowing into the outputs when V_{CC} is either open or shorted to ground. These diodes will not let current flow until the output voltage reaches 5.5V.

The I_{OS} limiting resistors, R15, limit the amount of current that can be sourced from the HIGH to ground. Note that R15 is 12Ω for the A_N outputs. Therefore, under the same conditions, the B_N output pull-up structure will be able to source 2.5 times more current than the A_N outputs.

Minimizing Ground Bounce

Refer to *Application Note AN213 "74F30XXX Family Applications"* for a detailed discussion of "ground bounce" and internal noise generation due to reduced ground lead inductance. When a TTL output switches from LOW to HIGH or HIGH to LOW, some feed-through or crossover current will be injected into the ground lead of the IC while both the pull-up and pull-down output drive structures are ON simultaneously. The larger the number of switched outputs, the larger the feed-through current and "ground bounce".

"Ground bounce" directly affects the input threshold of a gate, and therefore, its noise sensitivity. The newer output structure design used in the "Light Load" NPN input product line allow all outputs to switch simultaneously with minimal "ground bounce".

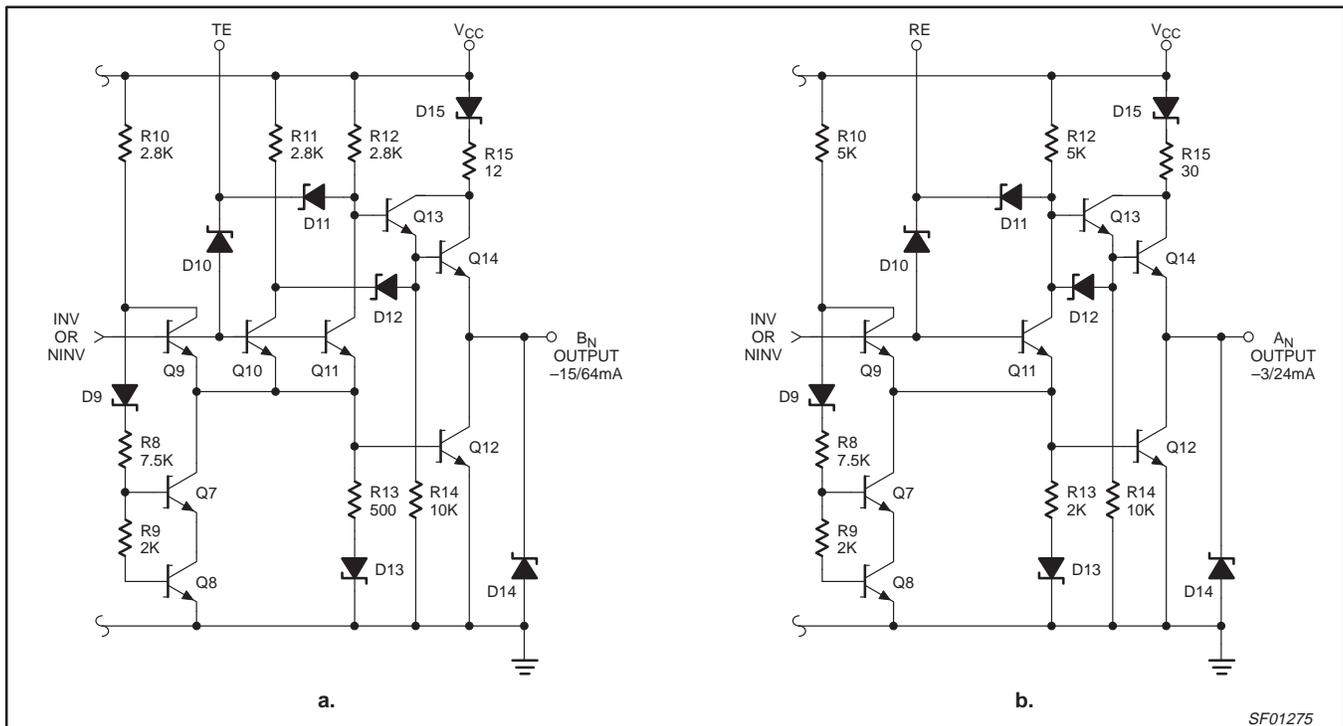


Figure 4. Two Typical "Light Load" Output Structures (74F657)

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Table 1. The 74F "Light Load" Input Products

Part Number	# Bits	Polarity	Output	Broad-side	I _{OH} /I _{OL} MIN	Storage	Speed	Parity	Comments
"Light Load" Buffers and Line Drivers									
74F125/6	4-bit	NINV	3-St	No	-15/64mA	None	6.5ns	No	Separate output enables (F125 = \overline{EN} ; F126 = EN)
74F365/6	6-bit	NINV	3-St	No	-15/64mA	None	7.5ns	No	Common output enable
74F367/8	6-bit	INV	3-St	No	-15/64mA	None	7.5ns	No	Two output enables controlling 3 outputs each
74F455/6	8-bit	INV/NINV	3-St	Yes	-15/64mA	None	7.5ns	Yes	Multiple/Ctr package GND pin, $\Sigma_E, \Sigma_O = -15/64mA$
74F540/1	8-bit	INV/NINV	3-St	Yes	-15/64mA	None	7.5ns	No	Broadside pinout of F240
74655A/6A	8-bit	INV/NINV	3-St	Yes	-15/64mA	None	7.5ns	Yes	$\Sigma_E, \Sigma_O = -15/64mA$
74F804/1804	6-bit	2I-NAND	3-St	No	-48/48mA	None	4.0ns	No	PNP Hex 2-Input NAND gate, F1804 has center supply pins
74F805/1805	6-bit	2I-NOR	3-St	No	-48/48mA	None	4.0ns	No	PNP Hex 2-Input NOR gate, F1805 has center supply pins
74F808/1808	6-bit	2I-AND	3-St	No	-48/48mA	None	5.0ns	No	PNP Hex 2-Input AND gate, F1808 has center supply pins
74F827/8	10-bit	NINV/INV	3-St	Yes	-15/64mA	None	9.0ns	No	
74F832/1832	6-bit	2I-OR	3-St	No	-48/48mA	None	5.5ns	No	PNP Hex 2-Input OR gate, F1832 has center supply pins
74F1240/1	8-bit	INV/NINV	3-St	No	-15/64mA	None	6.5ns	No	Light Load pin replacement for F240/1
74F1244	8-bit	INV/NINV	3-St	No	-15/64mA	None	7.0ns	No	Light Load pin replacement for F244
74F30240/4	8-bit	INV/NINV	OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30 Ω PC board data transmission line driver
"Light Load" Registers and Latches									
74F166	8-bit	NINV	3-St	Yes	-1/20mA	S/R	110MHz	No	Serial/Parallel-In, Serial-Out
74F195	4-bit	NINV	3-St	Yes	-1/20mA	S/R	110MHz	No	Serial/Parallel-In, Serial-Out
74F273	8-bit	NINV	3-St	No	-1/20mA	S/R	120MHz	No	D-type flip-flops
74F377	8-bit	NINV	3-St	No	-1/20mA	S/R	100MHz	No	D-type flip-flops
74F595	8-bit	NINV	3-St	Yes	-3/20mA	S/R	80MHz	No	S or P-In, Serial-Out with D-register output storage
74F597	8-bit	NINV	3-St	Yes	-3/20mA	S/R	80MHz	No	S or P-In, Serial-Out with D-register input storage
74F598	8-bit	NINV	3-St	Yes	-3/20mA	S/R	80MHz	No	F597 with multiplexed inputs and outputs
74F821/2	10-bit	NINV/INV	3-St	Yes	-15/64mA	Reg	100MHz	No	Data, Master Reset, Output Enables & Clock EN inputs
74F823/4	9-bit	NINV/INV	3-St	Yes	-15/64mA	Reg	100MHz	No	Data, Master Reset, Output Enables & Clock EN inputs
74F825/6	8-bit	NINV/INV	3-St	Yes	-15/64mA	Reg	100MHz	No	Data, Master Reset, Output Enables & Clock EN inputs
74F841/2	10-bit	NINV/INV	3-St	Yes	-15/48mA	Latch	100MHz	No	Data, Master Reset, Output Enables & LE Enable inputs
74F843/4	9-bit	NINV/INV	3-St	Yes	-15/48mA	Latch	100MHz	No	Data, Master Reset, Output Enables & LE Enable inputs
74F845/6	8-bit	NINV/INV	3-St	Yes	-15/48mA	Latch	100MHz	No	Data, Master Reset, Output Enables & LE Enable inputs

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Part Number	# Bits	Polarity	Output	Broad-side	I _{OH} /I _{OL} MIN	Storage	Speed	Parity	Comments
"Light Load" Transceivers/Latched or Registered Transceivers									
74F545	8-bit	NINV	A _N = 3-St	Yes	-3/24mA	None	7.0ns	No	Pin-for-pin replacement for the Intel 8286
			B _N = 3-St	Yes	-15/64mA	None	7.0ns	No	
74F588	8-bit	NINV	A _N = 3-St	Yes	-3/24mA	None	7.5ns	No	IEEE-488/GPIB with output line termination resistors
			B _N = 3-St	Yes	-15/64mA	None	7.5ns	No	
74F620/23	8-bit	INV/NINV	B _N = 3-St	Yes	-15/64mA	None	7.5ns	No	A _N ↔ B _N , A _N = -3/24mA
74F621/22	8-bit	NINV/INV	B _N = OC	Yes	OC/64mA	None	13.0ns	No	A _N ↔ B _N , A _N = OC/24mA
74F640	8-bit	INV	A/B = 3-St	Yes	-15/64mA	None	7.5ns	No	A _N ↔ B _N
74F641/42	8-bit	NINV/INV	A/B = OC	Yes	OC/64mA	None	13.0ns	No	A _N ↔ B _N
74F646/48	8-bit	NINV/INV	A/B = 3-St	Yes	-15/64mA	2-Reg	11.5ns	No	A _N ↔ B _N , Registers for A _N & B _N ports, 80MHz (Min.)
74F647/49	8-bit	NINV/INV	A/B = OC	Yes	OC/64mA	2-Reg	19.5ns	No	A _N ↔ B _N , Registers for A _N & B _N ports, 40MHz (Min.)
74F651/2	8-bit	INV/NINV	A/B = 3-St	Yes	-15/64mA	2-Reg	12.5ns	No	A _N ↔ B _N , Registers for A _N & B _N ports, 80MHz (Min.)
74F653	8-bit	NINV/INV	B _N = 3-St	Yes	-15/64mA	B _N -Reg	11.0ns	No	A _N → B _N , B _N port = 85MHz (Min.)
			A _N = OC	Yes	OC/64mA	A _N -Reg	20.0ns	No	B _N → A _N , A _N port = 45MHz (Min.)
74F657	8-bit	NINV	B _N = 3-St	Yes	-15/64mA	None	8.0ns	Yes	A _N ↔ B _N , Parity I/O, Odd/Even In & Error Out
74F861/2	10-bit	NINV/INV	A/B = 3-St	Yes	-15/64mA	None	10.0ns	No	A _N ↔ B _N
74F863/4	9-bit	NINV/INV	A/B = 3-St	Yes	-15/64mA	None	10.0ns	No	A _N ↔ B _N
74F1242/3	8-bit	INV	A/B = 3-St	No	-15/64mA	None	7.5ns	No	A _N ↔ B _N , Light Load pin replacements for F240/1
74F1245	8-bit	INV	A/B = 3-St	Yes	-15/64mA	None	6.5ns	No	A _N ↔ B _N , Light Load pin replacements for F245
74F30245	8-bit	NINV	B _N = OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω transmission line driver, B _N = 0.6mA I _{IL}
			A _N = 3-St	Yes	-3/24mA	None	7.0ns	No	
74F30640	8-bit	INV	B _N = OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω transmission line driver, B _N = 0.6mA I _{IL}
			A _N = 3-St	Yes	-3/24mA	None	7.0ns	No	
"Light Load" Transceivers/Latched or Registered Transceivers									
74F85	4-bit	INV/NINV	3-St	No	-1/20mA	None	14.5ns	No	4-bit magnitude comparator
74F280B	9-bit	NINV	3-St	Yes	-1/20mA	None	14.5ns	Yes	Parity generator/checker
74F604	16-bit	NINV	3-St/OC	Yes	-3/24mA	D-Reg	80MHz	No	Dual 8-bit registered octal multiplexer

NOTES:

All parameters are worst-case, unless otherwise specified.

3-St = 3-State

OC = Open Collector

Reg = LOW-to-HIGH edge clocked D-type register

Latch = HIGH logic level on the latch enable logic data passes directly through D-type latch

= HIGH-to-LOW logic level transition of the latch enable, data is stored in the D-type latch

S/R = Shift Register

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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