APPLICATION NOTE

ABSTRACT

The SA1630 is a quadrature IF transceiver IC intended to be used for WLAN and other wireless datacom applications. The SA1630 evaluation board, along with its associated software, is designed to facilitate the evaluation of this IC. It provides SMA, and header connectors for easy connection to external test equipment. Several balun transformers are provided to easily convert the required differential signals at the IC to and from the single-ended signals at the test equipment. A 10 switch dip is used for mode selection and external VGA programming, an external VCO for generating the LO, a connection port for monitoring the LO signal, a jumper for easily breaking the PLL, an LED for indicating a locked condition, easy connection to individual circuit supply lines and Tx input DC bias points and required matching components are all included on this evaluation board.

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SA1630 IF transceiver demonstration board

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GENERAL DESCRIPTION

The SA1630 is a quadrature IF transceiver IC intended to be used for WLAN and other wireless datacom applications. It can be used for IF frequencies from 70 to 400 MHz, and data rates in excess of 11 Mbps. The receive path has a bandwidth of approximately 7.5 MHz and 80 dB of voltage gain. It incorporates 70 dB of programmable linear gain control composed of 54 dB of gain and 16 dB of attenuation with a resolution of 2 dB, a pair of quadrature down-conversion mixers and a pair of baseband amplifiers designed to clamp symmetrically above 1 V_{p-p} across a 1K ‖ 15 pF load in order to avoid DC shift at the interface to the baseband processor. The transmit path contains I and Q channel up-converter mixers with an input bandwidth of more than 22 MHz. The SA1630 also contains an integrated reference and main divider, phase detector and programmable charge pump output currents for phase locking an external VCO. Thus, an external frequency synthesizer is no longer needed, which presents a significant cost savings to the system designer. The required quadrature LO signals are internally generated and the resulting output composed of the sum of the I and Q channel up-converter mixers yields a single sideband suppressed carrier output of typically 475 μA with carrier and sideband suppression of typically 36 dBc and 47 dBc, respectively. The associated Tx noise floor is approximately –156 dBc/Hz. The SA1630 provides several programmable operation modes which can be used to minimize power consumption or allow the Rx DC bias circuitry to remain active for ac coupling of the Rx baseband outputs. Other programmable options include the ability to operate the Tx I and Q channel mixers independently to verify proper Tx operation; an integrated 2.5 V regulated reference output can be selected during Tx mode; and the comparison frequency signals derived from the reference and main input signals can be directed to the lock detect pin to verify proper phase locked loop operation.

The SA1630 evaluation board, along with its associated software, is designed to facilitate the evaluation of this IC. It provides SMA, and header connectors for easy connection to external test equipment. Several balun transformers are provided to easily convert the required differential signals at the IC to and from the single-ended signals at the test equipment. A 10 switch dip is used for mode selection and external VGA programming, an external VCO for generating the LO, a connection port for monitoring the LO signal, a jumper for easily breaking the PLL, an LED for indicating a locked condition, easy connection to individual circuit supply lines and Tx input DC bias points and required matching components are all included on this evaluation board.

PIN AND EXTERNAL PART DESCRIPTION

The following pin and external part descriptions for the schematic shown in Figure 1 are provided to familiarize yourself with the details of the SA1630 evaluation board as quickly as possible.

Pin 1 (V_{CC} VGA24) and Pin 48 (GND)

These are the DC supply connections to a portion of the Rx programmable gain control stages. Capacitors C1 (0.1 μF) and C39 (2.2 μF) are ac decoupling caps, and should be placed as close to the IC as possible. This supply line is connected to pin 3 of the 8-pin header connector and also to the common V_{CC} post via a 0 Ω resistor. The current consumption of this stage can be evaluated by removing the 0 Ω resistor and connecting V_{CC} VGA to an isolated power supply at pin 3 of the 8-pin header connector.

Pin 2 (GND VGA) and Pin 3 (V_{CC} VGA)

These are the DC supply connections to a portion of the Rx programmable gain control stages. Capacitors C2 (0.1 μF) and C40 (2.2 μF) are ac decoupling caps and should be placed as close to the IC as possible.

Pin 4 (PLL_ON)

This pin enables/disables the integrated phase locked loop circuitry. A high voltage placed at this pin through switch 2 of the 10 switch DIP SW1 activates the circuitry. A low voltage at this pin disables the PLL and places the part in a low current sleep mode state. Capacitor C3 (330 pF) is provided to smooth out switching transients. Pin 4 is one of three pins used to select between the various operational modes of the IC. It must be high to enable the other modes. (Note: The OFF position designated on the 10 switch DIP package corresponds to V_{CC} and switch #1 should be in the ON position to connect V_{CC} to the other switches.)

Pin 5 (RX_ON)

This pin, together with pin 23 (TX_ON) controls the various different Tx and Rx operational modes. Capacitor C4 (330 pF) is provided to smooth out switching transients. A high or low voltage can be connected to this pin through switch 3 of the 10 switch DIP SW1. This pin must be in a high state to select Rx operation of the IC. If this pin is left high while also setting pin 23 (TX_ON) high for Tx operation, the Rx bias circuitry will remain active during Tx operation. This is important if the Rx outputs are ac coupled in the targeted application. (Note: the OFF position designated on the 10 switch dip package corresponds to V_{CC} and switch #1 should be in the ON position to connect V_{CC} to the other switches.)

Pin 6 (GND)

This is a ground connection to the IC and should be connected to the PCB ground as close to the IC as possible.

Pins 7 to 12 (C0 to C5)

These are the external gain control programming pins. A high or low voltage is connected to these pins though resistors R1–R9 (1K) and switches 5–10 on the 10 switch DIP SW1. The gain control can be programmed via the three wire bus connection, or externally using these pins. The default programming mode when the IC is first powered up is to enable external programming using these pins. Each of these pins is connected to a post to easily check the state of the pin. (Note: the OFF position designated on the 10 switch dip package corresponds to V_{CC} and switch #1 should be in the ON position to connect V_{CC} to the other switches.)

Pin 13 (GND-BB), Pin 14 (GND-BB), and Pin 15 (V_{CC}_BB)

These are the DC supply connections to the Rx baseband output circuitry. Capacitors C6 (2.2 μF) and C7 (0.1 μF) are ac decoupling caps and should be placed as close to the IC as possible. This supply is connected through pin 2 of the P2 connector on the PCB.

Pin 16 (QRX_OUT) and Pin 17 (IRX_OUT)

These are the Rx baseband output pins. Resistors R11 (1 k) and R13 (1 k) provide the specified output load. Capacitors C8 (0.1 μF), C9 (0.1 μF), C10 (0.1 μF), and C11 (0.1 μF) are DC blocking caps. Resistors R10(430) and R12(430) reduce the loading effects when 50 Ω measurement equipment is connected the SMA connectors. These pins are also connected to a test point post for convenient connection to an active FET probe.

Pin 18 (QTX_IN) and Pin 19 (QTX_INX)

These are the differential Q-channel Tx baseband input pins. These pins are connected to a 16:1 impedance balun transformer, which converts the 50 Ω single-ended input at the PCB to the required differential inputs at the pins. Also, the DC bias point (approximately $V_{CC}/2$) is connected to these input pins through the secondary center-tap of the balun. This connection is made at pin 1 of the connector P2 on the PCB. Capacitors C12 (0.1 μF) and C13 (2.2 μF) are ac decoupling caps.

Pin 20 (ITX_IN) and Pin 21 (ITX_IN)

These are the differential I-channel Tx baseband input pins. They are connected to circuitry identical to that described for pins 18 and 19.

Pin 22 (V_{CC}_DIG) and Pin 23 (GND_DIG)

These are the DC supply connections to the internal digital circuity. Capacitors C14 (0.1 μF) and C16 (2.2 μF) are ac decoupling caps and should be placed as close to the IC as possible. This supply is connected through pin 8 of the P2 connector on the PCB.

Pin 23 (TX_ON)

This pin, together with pin 5 (RX_ON) controls the various different Tx and Rx operational modes. Capacitor C15 (330 pF) is provided to smooth out switching transients. A high or low voltage can be connected to this pin through switch 4 of the 10 switch DIP SW1. (Note: The OFF position designated on the 10 switch dip package corresponds to V_{CC}, and switch #1 should be in the ON position to connect V_{CC} to the other switches.)

Pin 25 (CLK_INX) and Pin 26 (CLK_IN)

These are the differential reference oscillator inputs. This signal is brought to the IC single-ended by ac grounding pin 25 with capacitor C17 (0.01 μF). Capacitor C18 (0.01 μF) is a DC blocking capacitor, and R16(51) sets the impedance at the port to 50 Ω to simplify input power calculations.

Pin 27 (GND_LO)

This pin is connected to the internal ground of the LO circuitry. This pin should be connected to PCB ground, and as close to the IC as possible.

Pin 28 (LO_IN) and Pin 29 (LO_INX)

These are the differential local oscillator pins. These pins are connected to a 4:1 impedance balun transformer through the DC blocking capacitors C19 (0.01 μF) and C20 (0.01 μF). R19 (50 Ω) is placed at the primary to simplify input power calculations. The T-network composed of R20, R21 and R22 (all 18 Ω) splits the power delivered by the VCO evenly between the LO input circuitry and the SMA connection port when 50 Ω test equipment is present.

Pin 30 (LOCK)

This is the lock detect pin which should light up when lock is achieved. This pin is also used in test modes to monitor the comparison frequencies into the phase detector. Capacitor C22 (0.1 μF) is a DC blocking capacitor when this pin is used for this purpose. Resistor R23 (1 K) is a current limiting resistor to protect the diode.

Pin 31 (STROBE), Pin 32 (CLOCK), and Pin 33 (DATA)

These pins are the three wire bus interface used to program the internal registers. They are connected to pins 1, 2, and 3 of the 6-pin three wire bus header connector on the PCB. This header is then connected to the three wire bus interface card on the PC via ribbon cable.

Pin 34 (V_{CC}_CP) and Pin 36 (GND_CP)

These are the internal DC supply connections for the internal phase detector charge pump circuitry. Capacitors C27 (0.1 μF) and C29 (2.2 μF) are ac decoupling caps, and should be placed as close to the IC as possible.

Pin 35 (CP)

This pin is the phase detector charge pump output. It is connected to the loop filter composed of resistor R24 (4.7 K) and capacitors C23 (470 pF) and C24 (4.7 nF). This loop filter is connected to the 704 MHz voltage controlled oscillator through jumper SW2. Capacitors C25 (0.1 μF) and C26 (2.2 μF) provide ac decoupling for the VCO supply line. A jumper is provided to allow an easy way to break the loop.

Pin 37 (I_REF)

This pin sets the current of the phase detector charge pump output. This current is set by resistor R25 (51 K). Capacitors C28 (10 pF) and C30 (10 pF) provide ac decoupling, and should be placed as close to the IC as possible. The current setting resistor is calculated according to the equation:

$$R_{ext} = \frac{(V_{CC}\_CP - 1.6)}{31.2\ \mu A} \quad (1)$$

Pin 38 (V_REF)

This pin provides a 2.5 V regulated reference voltage in the two transmit modes. Test point TP4 is provided for convenient connection, and C31 (18 nF), R26 (20 K), and R27 (1.6 K) provide the required load and filtering.

Pin 39 (V_{CC}_TXRX), Pin 40 (GND_TXRX), and Pin 41 (GND_TXRX)

These pins are the DC supply connections to the internal TXRX circuitry. Pins 40 and 41 should be shorted together and connected to PCB ground. Capacitors C32 (0.1 μF), C33 (2.2 μF), and C34 (0.1 μF) are ac decoupling caps, and should be placed as close to the IC as possible.

Pin 42 (TXIF_OUT) and Pin 43 (TXIF_OUTX)

These pins are the differential transmit open collector outputs. Inductor L1 (150 nH) is part of the tuned balun circuitry which resonates out the pin capacitances. R28 (430) decreases the selectivity of the inductor to preserve wideband operation. The balun transformer T4 provides a 4:1 impedance transformation, as well as converting the balanced differential output signal to a single-ended signal. It also provides a DC connection from V_{CC} to the open collector outputs through the secondary center tap. L2 (22 nH) brings the Tx output port to 50 Ω, and capacitor C36 (100 pF) is a DC blocking cap.

Pin 44 (GND_SHL) and Pin 47 (GND_SHL)

These pins are connected to a ground shield internal to the IC. These pins should be connected to PCB ground as close to the IC as possible.

Pin 45 (RXIF_INX) and Pin 46 (RXIF_IN)

These are the differential RX IF input pins. Inductor L3 (100 nH) is part of the tuned balun circuitry which resonates out the pin capacitances, and the capacitance added by capacitors C37 (2.7 pF) and C38 (2.7 pF). R29 (5.1 K) decreases the selectivity of the inductor to preserve wideband operation. The balun transformer T5 provides a 1:4 impedance transformation as well as converting the single-ended input signal to a balanced differential output signal. R30 (0) is a 0 Ω surface mount connection where a DC blocking cap can easily be added if needed.

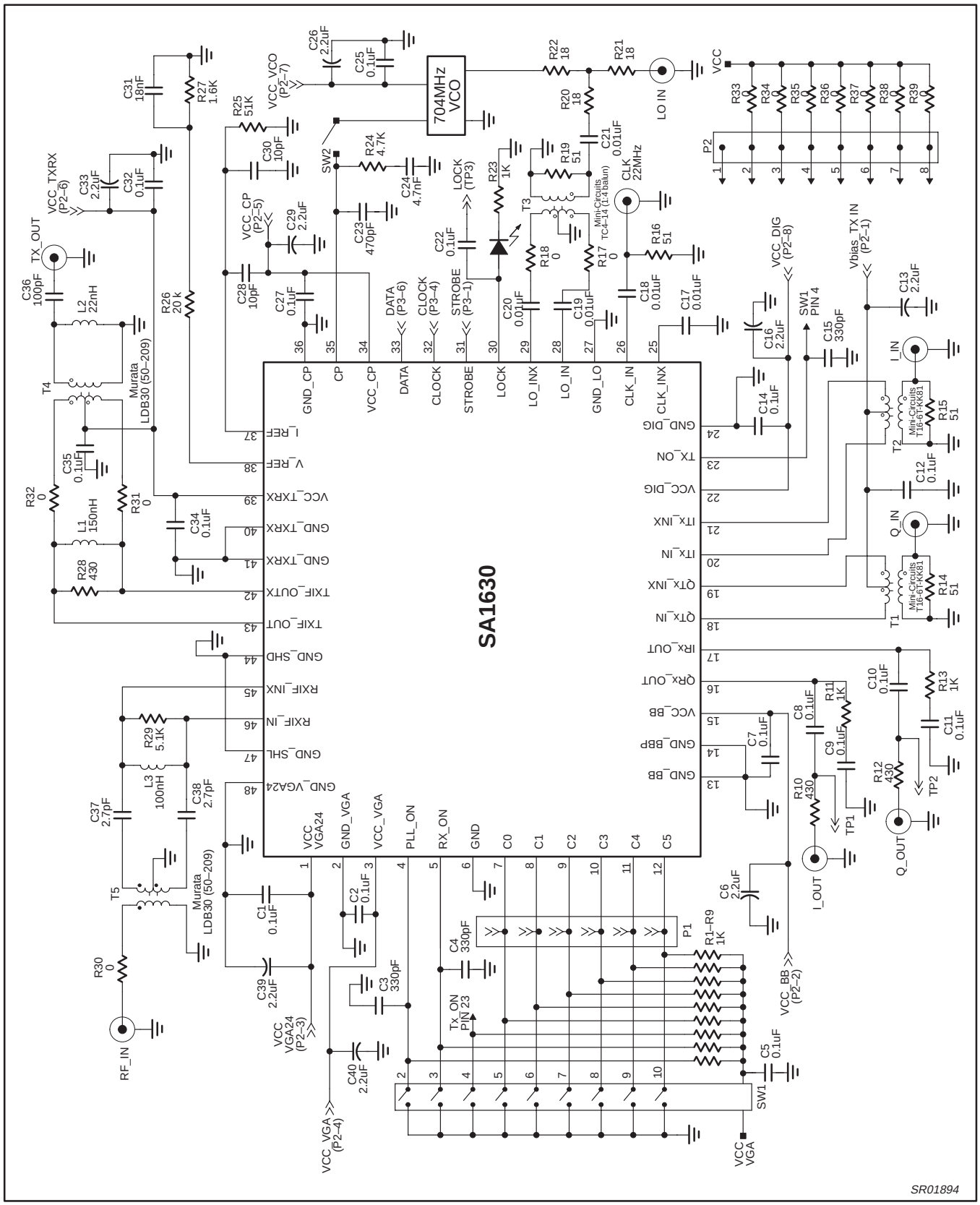

Figure 1. SA1630 IF transceiver demonstration board schematic

MEASURED SETUPS AND MEASURED DATA

DC verifications

Figure 2 shows the basic DC supply connections and mode select switch settings for verifying DC current consumption and for checking the DC bias voltages at each pin. These voltages are tabulated below and are useful for verifying proper operation of the part on the PCB, as well as being useful to customers configuring other external circuitry to the IC.

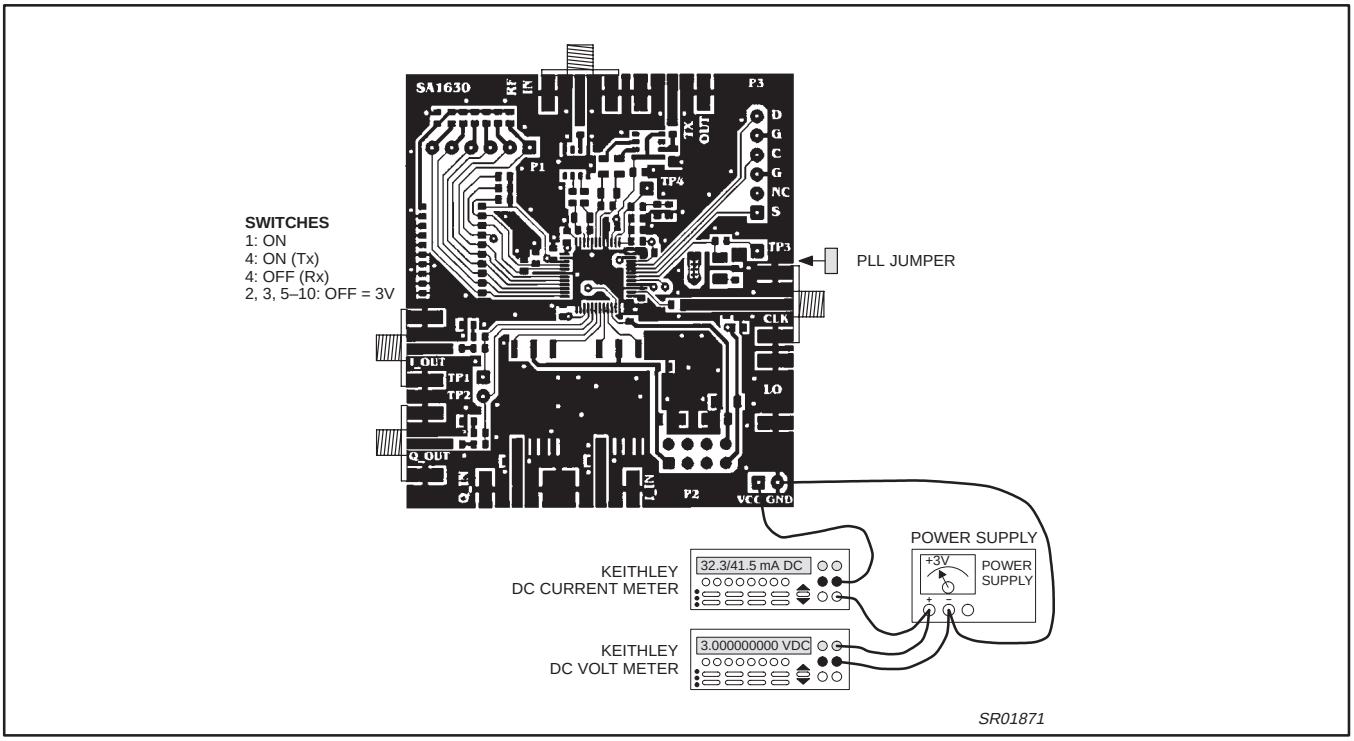

Figure 2. DC supply setup and mode select switch settings

Table 1. DC bias pin voltages for quick part functionality checks

Tx/Rx standby mode: all switches HIGH (OFF position).

Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage
1	3.0	13	0.0	25	2.0	37	1.6
2	0.0	14	0.0	26	2.0	38	2.5
3	3.0	15	3.0	27	0.0	39	3.0
4	3.0	16	1.9	28	2.0	40	0.0
5	3.0	17	1.9	29	2.0	41	0.0
6	0.0	18	2.9	30	0.2	42	3.0
7	3.0	19	2.9	31	0.0	43	3.0
8	3.0	20	2.9	32	0.0	44	0.0
9	3.0	21	2.9	33	0.0	45	1.8
10	3.0	22	3.0	34	3.0	46	1.8
11	3.0	23	3.0	35	0.0	47	0.0
12	3.0	24	0.0	36	0.0	48	0.0

Rx path voltage gain measurement

Figure 3 shows the necessary connections needed to evaluate the receive path. A signal generator is used to supply the 22 MHz, –10 dBm CLK reference frequency. Check to make sure the lock detection LED is glowing brightly. The RF input is set to 353 MHz, which is 1 MHz offset from the LO frequency. Thus, generating a 1 MHz tone at the output. The input level required to obtain a $1V_{p-p}$ signal at the output is used to calculate the Rx gain, as outlined below in the Question and Answer section. The datasheet specifications are met if a $1V_{p-p}$ output is obtained with an input power of approximately –77 dBm or less. The output should be measured with high impedance probes attached at the test point posts provided.

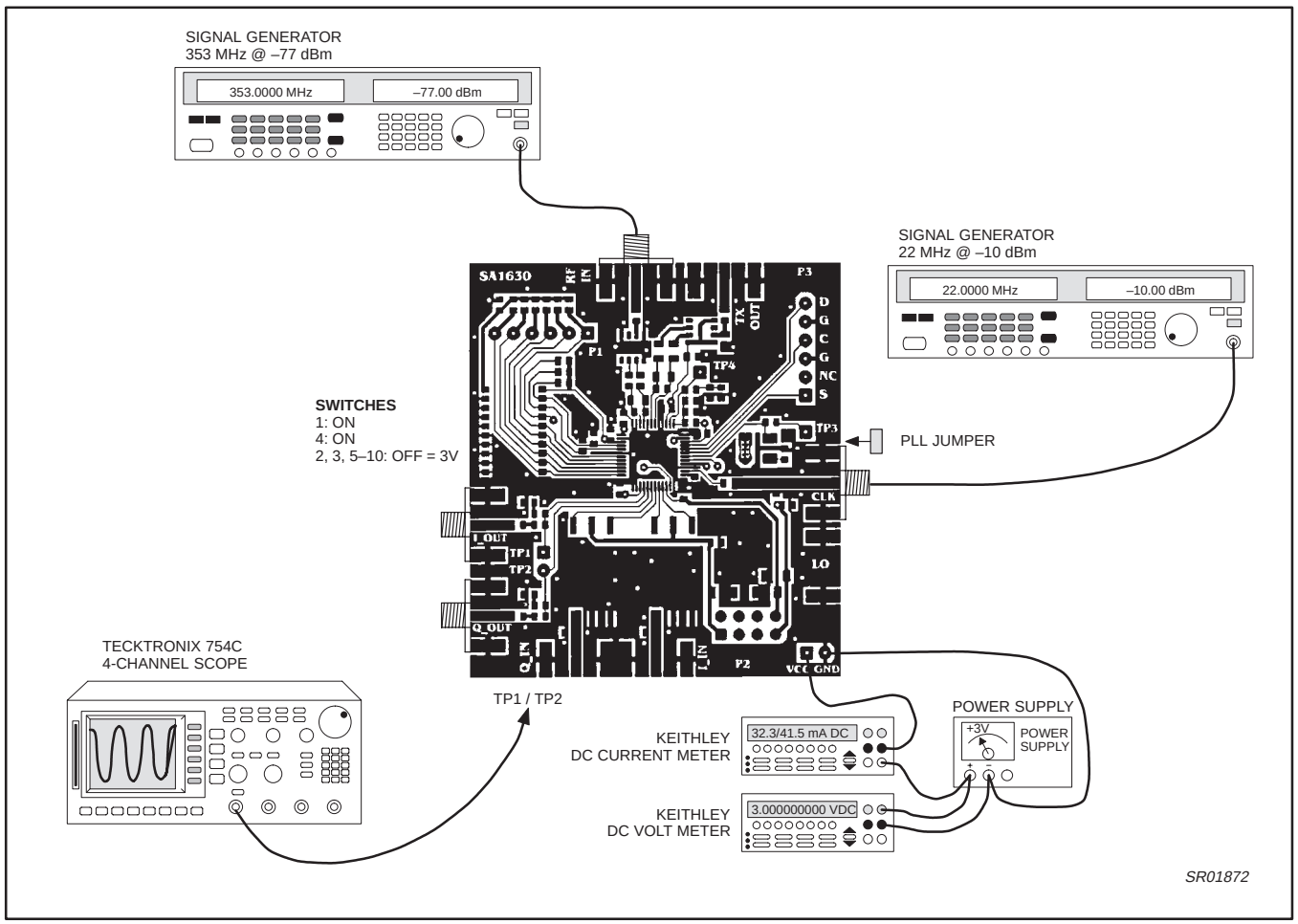

Figure 3. Set-up for Rx path voltage gain and symmetrical compression measurements

Symmetrical compression measurement

Figure 4 shows the symmetrical compression when the Rx input is over-driven. This is important to minimize DC shifts at the baseband processor interface.

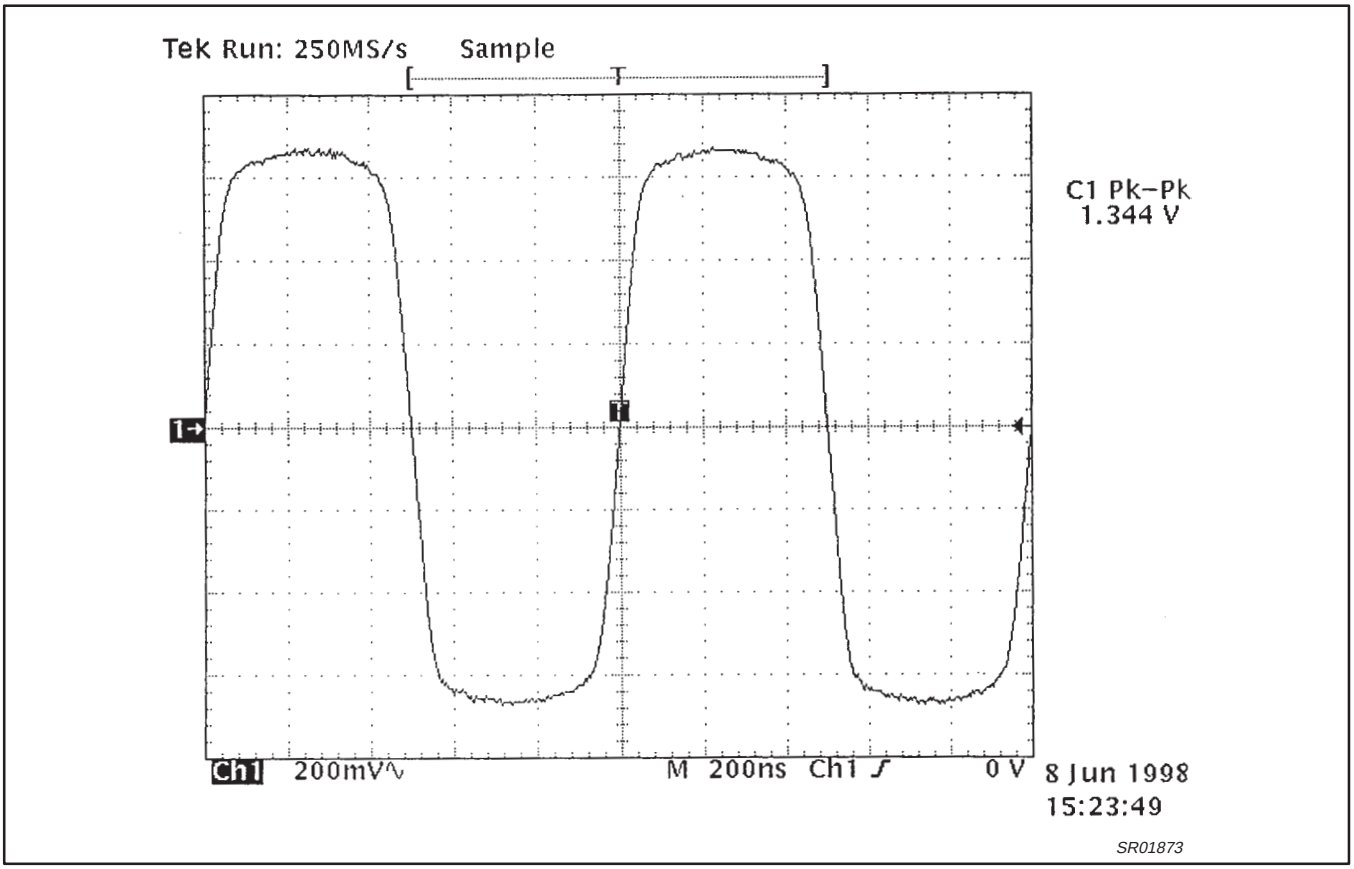

Figure 4. Symmetrical clamping at the Rx output when the Rx input is over-driven

Rx harmonic distortion measurement

Figure 5 shows the necessary connections required for measuring the receiver harmonic distortion. They are the same as those for the receive path measurements, only the Rx output is now measured using an active high-impedance FET probe connected to the test point posts. This test should be measured with the part programmed for maximum receiver gain.

Figures 6 through 9 show the measured values for the fundamental, second, third, and fourth harmonics. The HD2,3,4 parameter is calculated as follows:

$$HD2,3,4 = \frac{\sqrt{(H1^2) + (H2^2) + (H3^2)}}{H1} * * 100 \quad (2)$$

$$HD2,3,4 = \frac{\sqrt{(2.369^2) + (0.840^2) + (0.446^2)}}{276} * 100 = 0.925\%$$

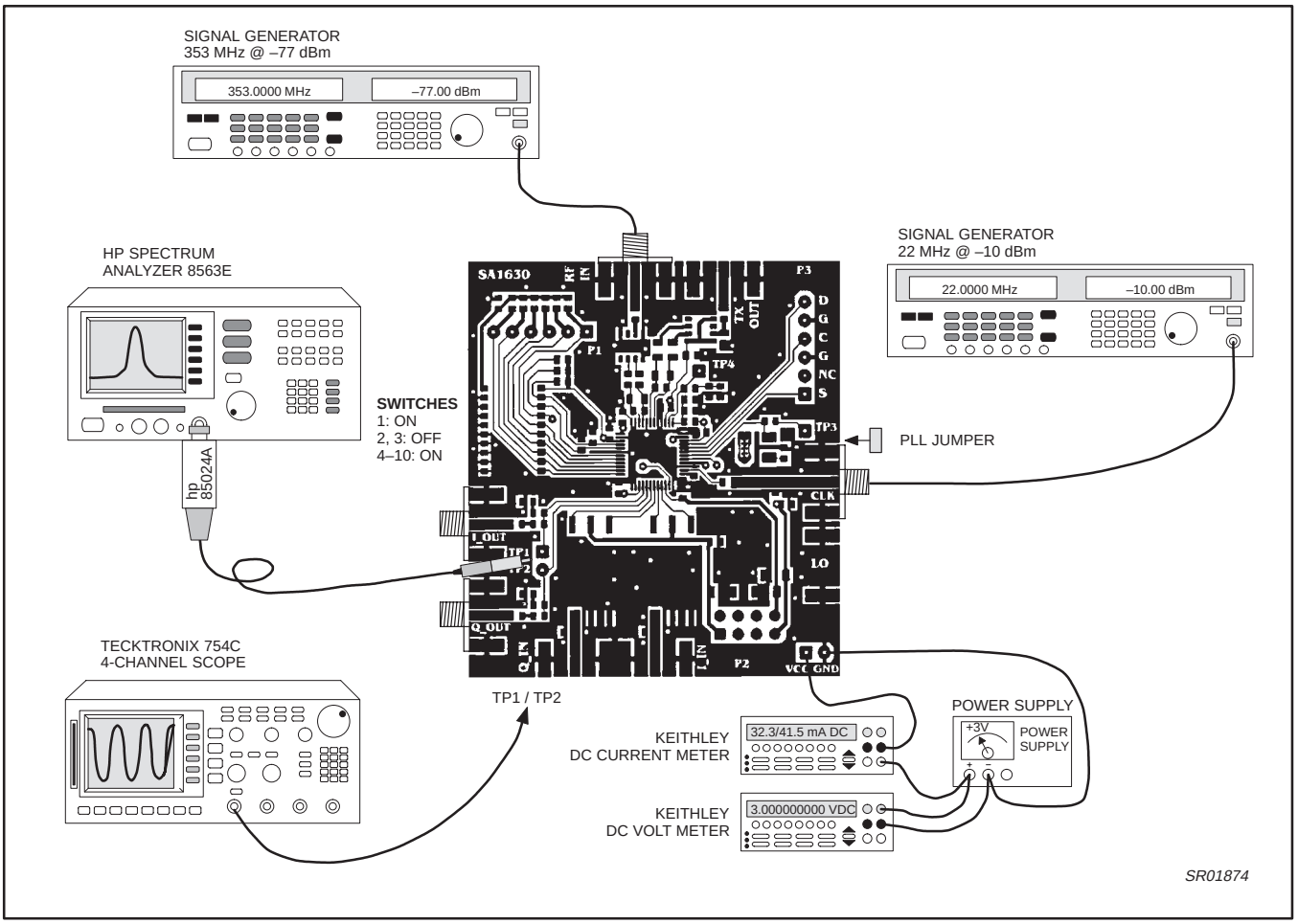

Figure 5. The set-up for measuring Rx harmonic distortion

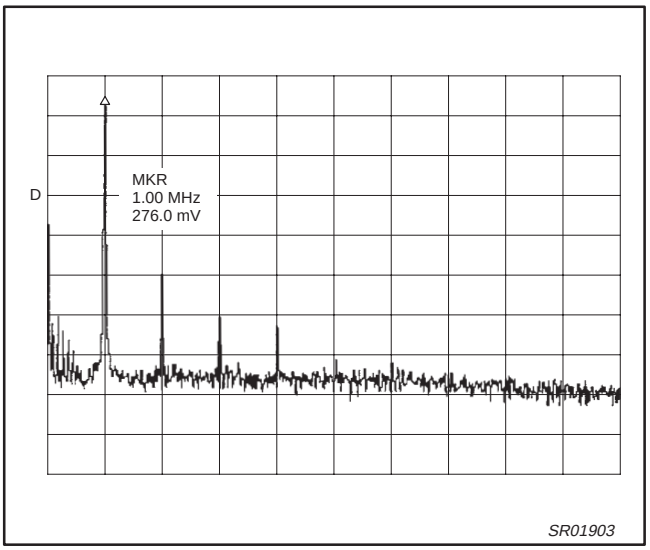

Figure 6. Voltage level of the Rx output fundamental

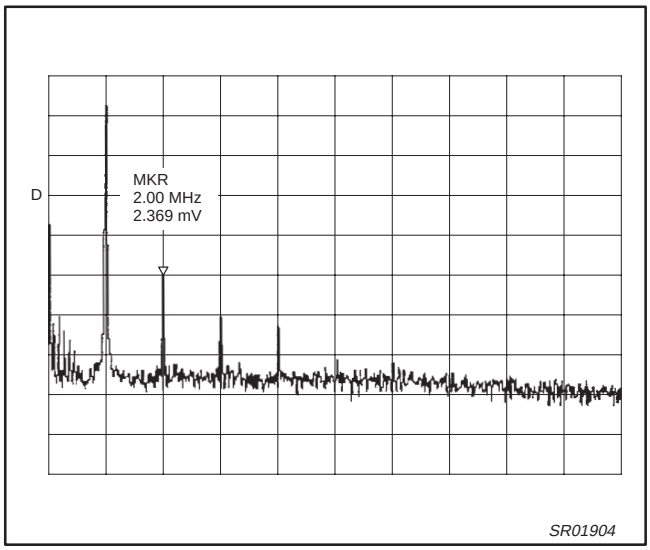

Figure 7. Voltage level of the Rx output 2nd harmonic

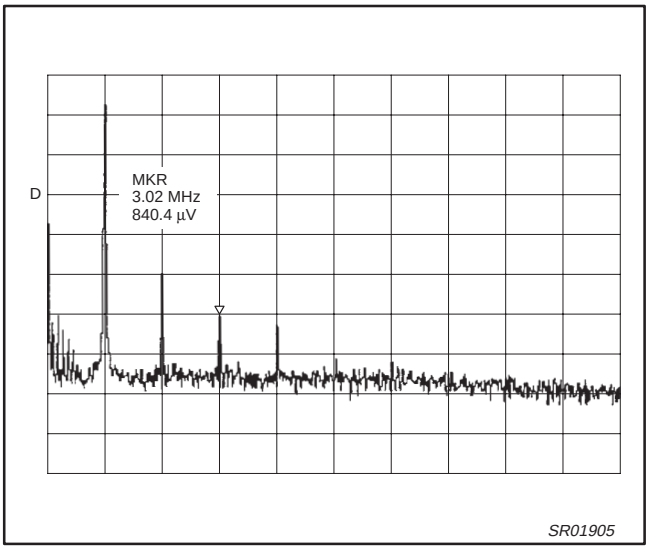

Figure 8. Voltage level of the Rx output 3rd harmonic

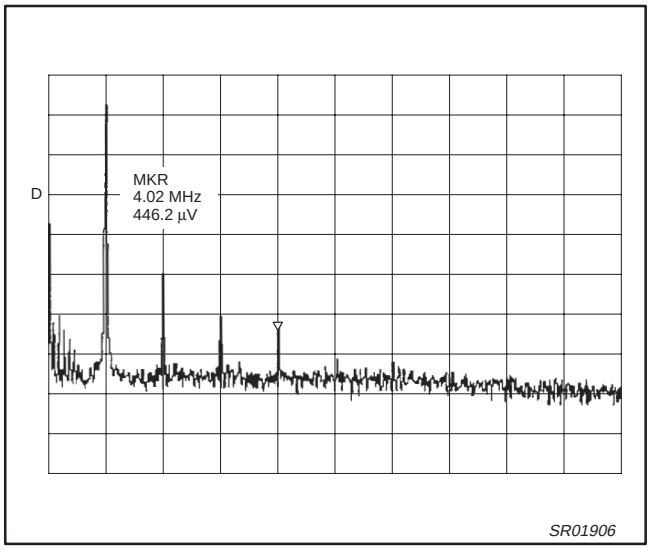

Figure 9. Voltage level of the Rx output 4th harmonic

Rx bandwidth measurement

The measurement set-up for determining the Rx bandwidth is identical to the harmonic distortion set-up shown in Figure 5. The spectrum analyzer should be set to maxhold while the Rx input frequency offset from the LO is increased from 1 MHz to 10 MHz. The Receive bandwidth is typically about 7.5 MHz, as shown in Figure 10.

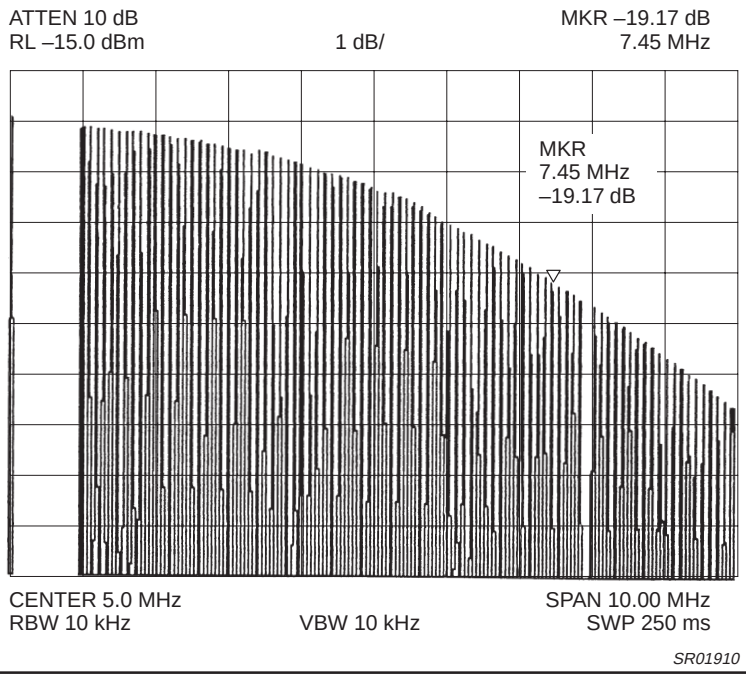

Figure 10. Rx 3 dB bandwidth measurement

Tx RMS output current, carrier suppression and sideband suppression measurements

Figure 11 shows the set-up necessary for obtaining Tx parameter measurements. The 1 MHz input tones need to be supplied from two signal generators that have their time references locked to each other to obtain the needed quadrature phase adjustment. The magnitude of these input signals need to be identical and the phase should be calibrated to as close to perfect quadrature as possible. The clock reference is again supplied by an external signal generator at 22 MHz, –10 dBm. The transmit output spectrum is viewed at the TXout port with a spectrum analyzer. To obtain carrier suppression, it is important to connect a DC voltage approximately equal to $V_{CC}/2$ to pin 1 of the 8-pin header connector as shown in Figure 11. This provides the proper DC bias to the Tx input pins through the secondary center-tap of the balun transformers. The amplitude of the input signals should be adjusted to provide a $1V_{p-p}$ input level at the Tx input pins. The measurement of this signal is made easily by connecting to the secondary terminals of the balun transformer. These signals are the C1 and C2 traces shown in Figure 12. Trace M1 is the $1V_{p-p}$ differential signal generated by mathematically subtracting trace C2 from trace C1. Typically, to obtain the $1V_{p-p}$ signal requires an output power of approximately –7.7 dBm from the signal generator.

Figures 13, 14, and 15 show the LO suppression, sideband suppression, and third harmonic distortion, respectively. The LO suppression is measured relative to the magnitude of the unsuppressed sideband, and should be 30 dBc or greater. The sideband suppression is also measured relative to the unsuppressed sideband and should be 35 dBc or greater. The third harmonic distortion product should be more than 45 dBc from the unsuppressed sideband.

The tx rms output current is simply calculated from the power measurement from equation (3).

For example, Figure 13 shows the measured output power at the port to be approximately –17 dBm. If we add 0.5 dB for losses through the balun transformer, we then get –16.5 dBm. Inserting this value in the equation yields a Tx rms output current of approximately 437 μA.

$$I_{rms} = \sqrt{10^{\left(\frac{P_{out}}{10}\right)} * \frac{1mW}{\text{load presented to the Tx pins} = \text{approx.}117\Omega}} \qquad (3)$$

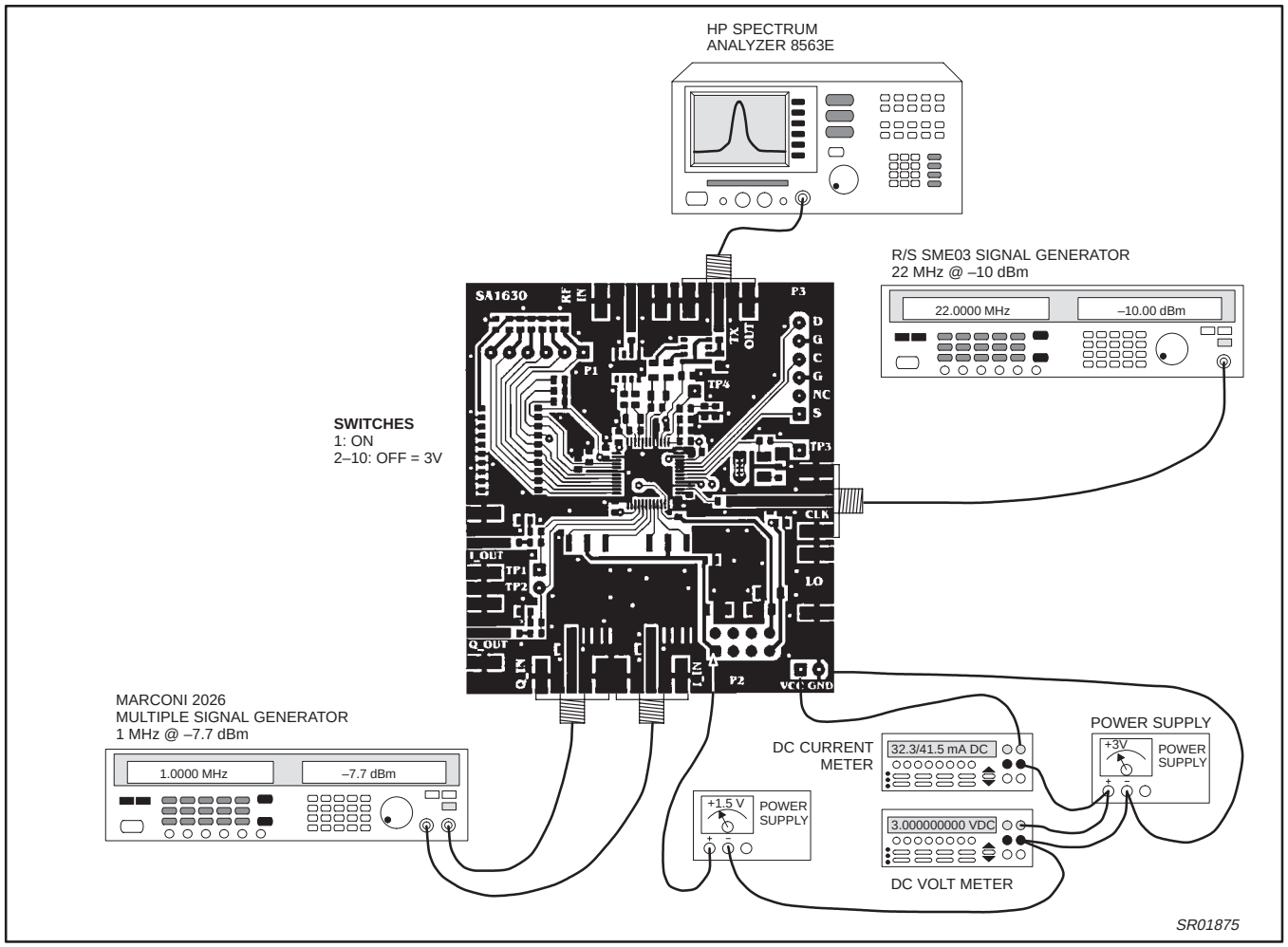

Figure 11. Tx measurement set-up

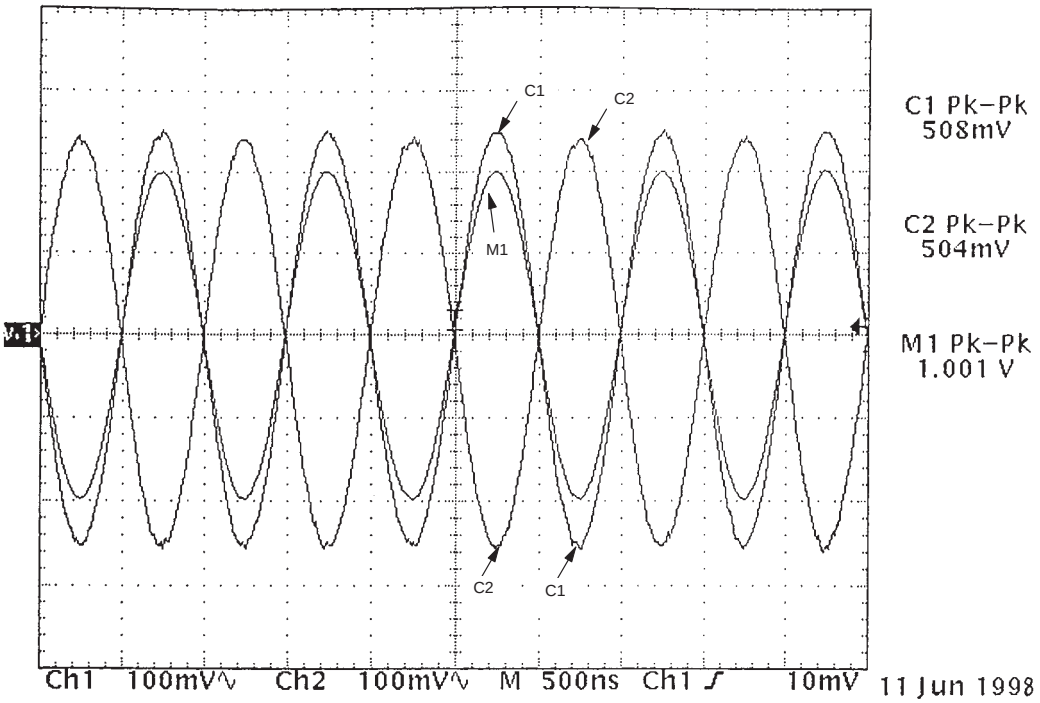

Figure 12. Calibrated $1V_{p-p}$ signal at the Tx input pins

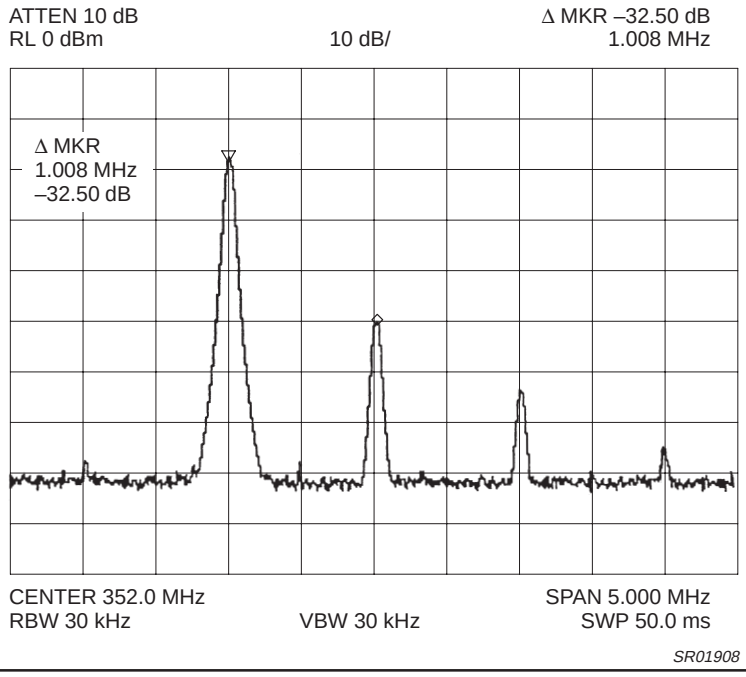

Figure 13. Tx output carrier suppression

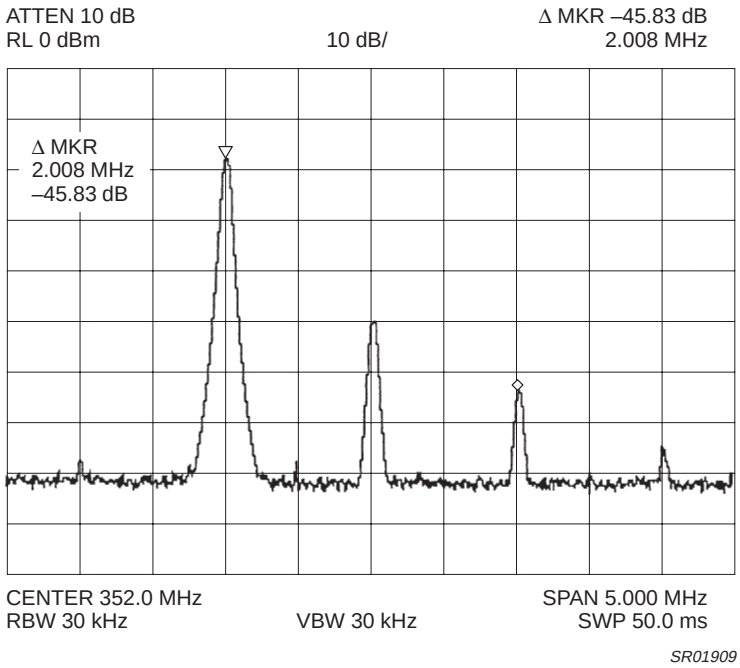

Figure 14. Tx output sideband suppression

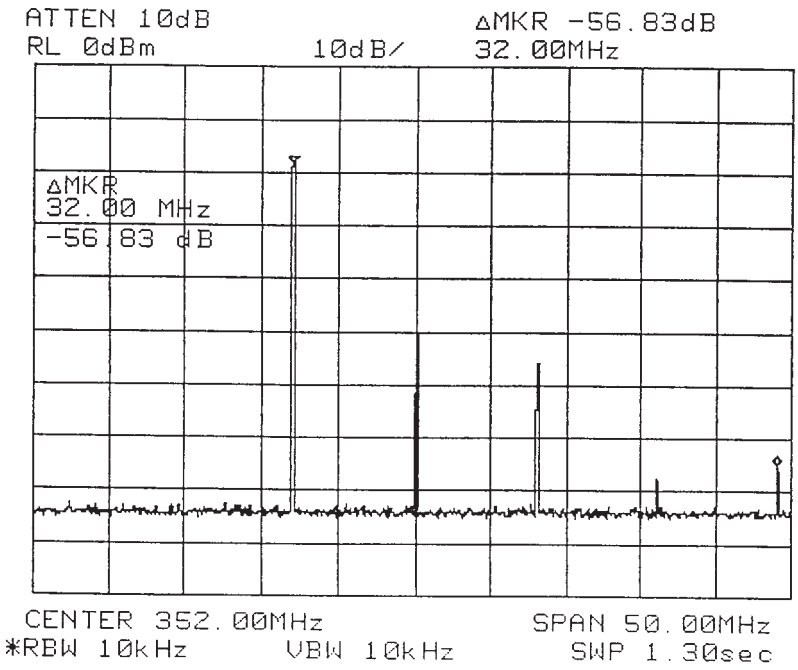

Figure 15. Tx output 3rd harmonic distortion

Tx input bandwidth measurement

The connections necessary for the Tx input bandwidth measurement is identical to that shown in Figure 11 with one notable exception. Only the I or the Q channel input signal should be connected. This creates a double sideband output, but we are only concerned with the bandwidth, so this is not a concern. The measurement is made by incrementing the input frequency and storing the result on the spectrum analyzer using the maxhold feature. The resulting spectrum is shown in Figure 16, and the bandwidth measurement is simply made on only one side of the spectrum. As shown, the Tx input bandwidth is well in excess of the 22 MHz specification.

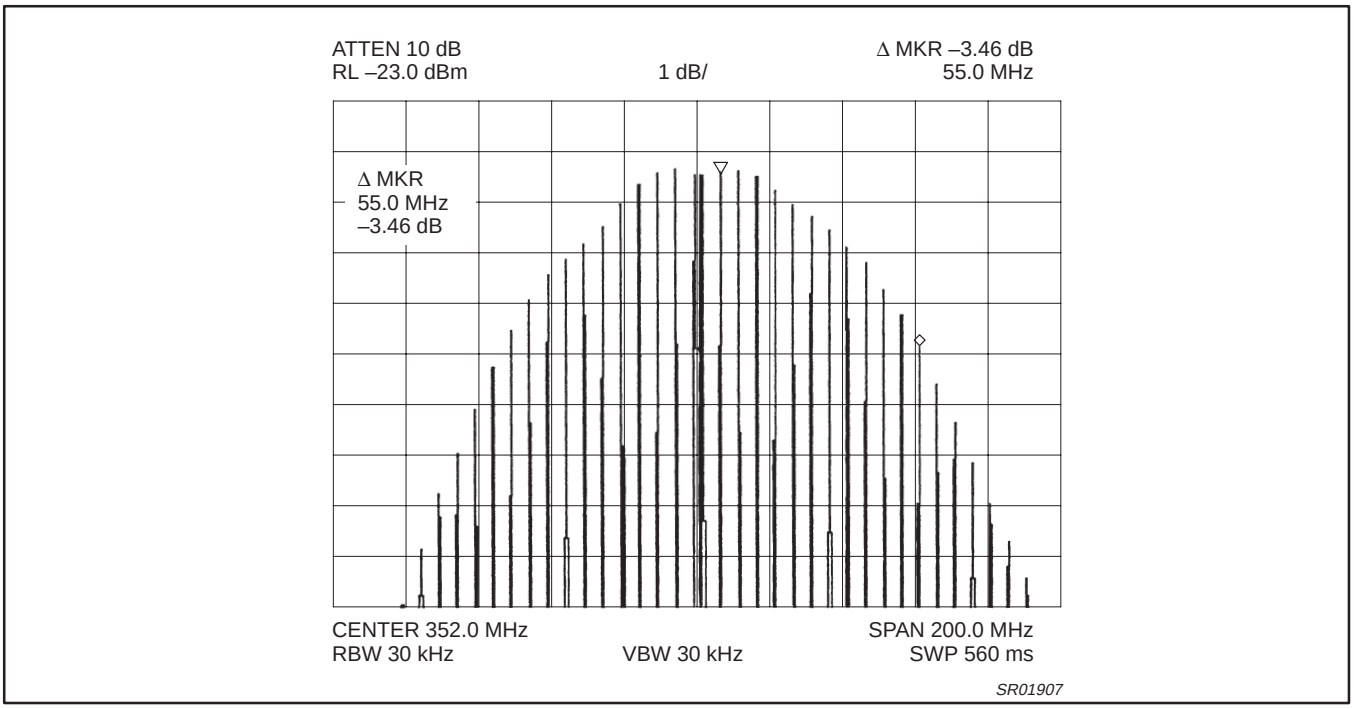

Figure 16. Tx input modulation bandwidth

Tx noise floor measurement

Figure 17 shows the necessary set-up for taking Tx noise floor measurements. Notice the LNA between the Tx output port and the spectrum analyzer. The Tx noise floor of the SA1630 is approximately the same as that of a typical spectrum analyzer. So, to reduce the noise of the measurement system, an LNA is used to effectively reduce the noise contribution of the wideband mixer in the spectrum analyzer. Figure 18 shows the measured gain of the LNA to be 22.3 dB, and Figure 19 shows the measured noise floor to be –134.7 dBm/Hz. (Be careful not to take the measurement away from any spurs that may be generated by the PCB board or the spectrum analyzer itself.) So the Tx noise floor is

–134.7 – 22.3 = –157 dBm/Hz

which is 1 dB better than the –156 dBm/Hz specification.

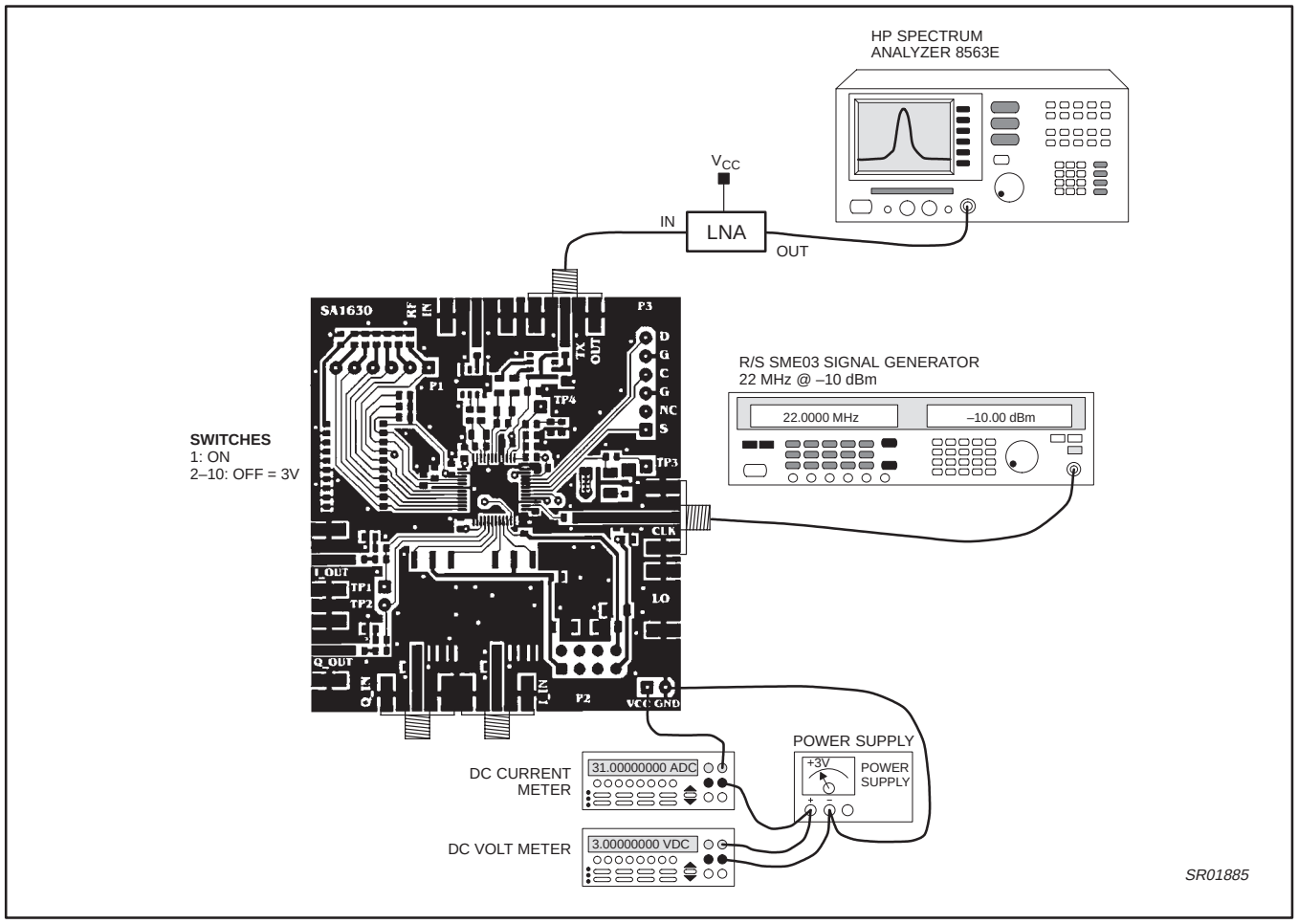

Figure 17. Tx noise floor measurement set-up

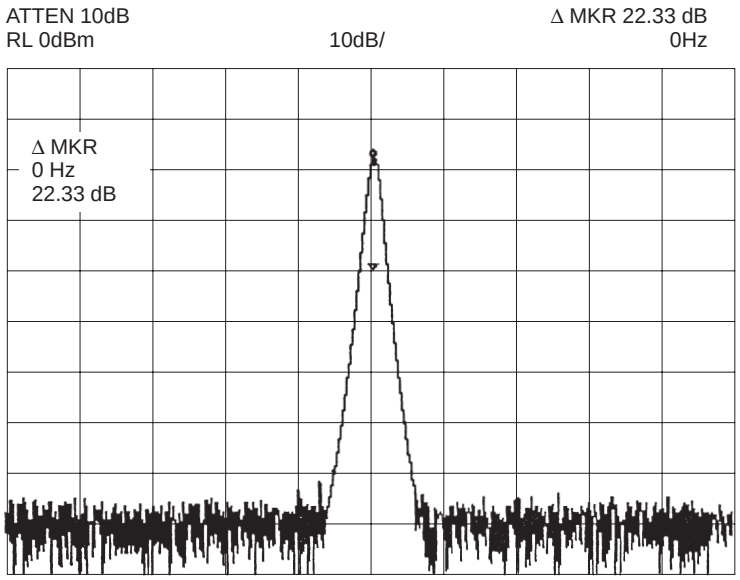

Figure 18. LNA gain of amplifier in Tx noise floor measurement set-up

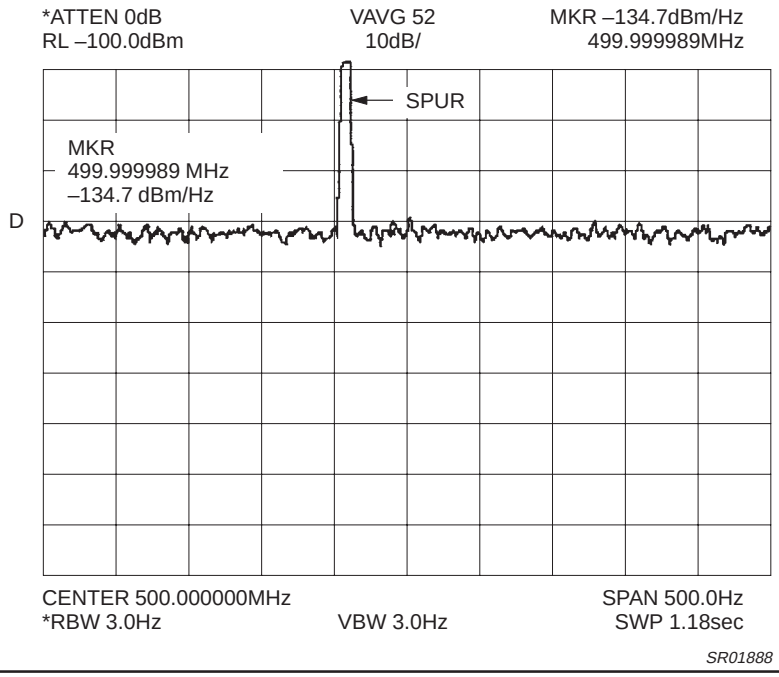

Figure 19. SA1630 Tx noise floor with 22.3 dB LNA in measurement system

ANSWERS TO COMMON QUESTIONS

Serial register and external AGC programming

Q: What is the easiest way to verify if the register programming via the three wire bus is operating correctly?

A: The easiest way to verify the functionality of the register programming is to change the reference divide ratio from 22 MHz to 8, 11, or 44 MHz while maintaining the Reference CLK input at 22 MHz. If the registers are being properly programmed, the LED should dim, indicating an out of lock condition. If this does not occur, check the three wire bus signals by selecting the “Repeat Last Word” button from the software. Connect STROBE, CLOCK and DATA to an oscilloscope. Trigger the scope from the STROBE signal.

Q: What are the LLL, I offset, and Q offset registers for?

A: In the predecessor to the SA1630, these registers were utilized to adjust for DC offset errors in the Rx outputs and to provide a feedback loop for correcting phase errors in the quadrature LO signals. These registers are not used in the SA1630 and cannot be programmed.

Q: Why is the Rx VGA Control programming table shown in the datasheet to achieve the 70 dB of AGC dynamic range discontinuous between decimal register values 15 and 23, and 31 and 52?

A: The AGC is composed of a combination of multiple amplifier stages and attenuators. The sequence in the datasheet was chosen to keep most of the gain in the early stages to optimize the overall noise figure of the Rx path. Note this discontinuous programming sequence when developing your own AGC control software or hardware.

Phase Locked Loop

Q: Why doesn’t the LED on my board indicated a locked condition?

A: Check the following:

- Make sure that the PLL_ON mode select switch #2 on the 10 switch DIP sets this pin HIGH. (This is the OFF position on the 10 switch DIP.)
- Make sure the jumper which connects the VCO to the loop filter is in position.
- Check the CLK signal to ensure it is the same as that selected in the software. If external programming is used, this will be the default value of 22 MHz.
- Check to make sure the main divide ratio is set correctly at LOin/2 (default = 352 MHz).
- Check to make sure that the supply voltage is reaching the VCO.
- Monitor the VCO output at the LO port with a spectrum analyzer to check if the signal is locked.

Q: What is the frequency range allowed for the reference frequency crystal?

A: The constraints on the IF frequency, together with the main and reference divide ratio ranges, suggest the following:

- FXTALmin = (IFmin/main div max)*ref div min
  = (70 MHz/511)*8
  = 1.0959 MHz
- FXTALmax= (IFmax/main div min)*ref div max
  = (400 MHz/64)*44
  = 275 MHz
- Measurements of the reference divider output have shown that the reference divider will work only up to approximately 200 MHz.

Q: Why is the VCO center frequency at 704 MHz when the IF frequency is 352 MHz?

A: Prior to the programmable main divider, there is an additional /2 divider internal to the IC.

Q: Why is the VCO mounted on the backside of the PCB?

A: At high AGC settings, the Rx path has approximately 85 dB of voltage gain. Harmonics of the VCO could potentially make their way to the RF input of the Receiver and saturate the AGC amps. The VCO was placed on the back side of the PCB in order to minimize the probability of this occurring.

Q: What is the 50 Ω T-network for at the LO port of the PCB?

A: The LO port on the PCB is for monitoring the PLL performance with a spectrum analyzer. The spectrum analyzer will present a 50 Ω impedance to this port. The objective of the T-network is to present a load of approximately 50 Ω to the 50 Ω output of the VCO and split the power delivered from the VCO evenly between the spectrum analyzer and the LO input circuitry. An 18 Ω resistor is placed in series with both the 50 Ω LO input and the 50 Ω spectrum analyzer, thus creating two parallel 68 Ω loads or a 34 Ω combined load. An additional 18 Ω resistor is also placed in series with this, which then presents 34 + 18 = 52 Ω to the VCO output.

Q: What is the sensitivity of the VCO?

A: The Murata MQE704 MHz VCO has a sensitivity of approximately 10.25 MHz/V.

Q: My PLL is not locking. How can I ensure that the proper signals are reaching the phase detector?

A: The SA1630 can be programmed into several test modes via the three wire bus interface. These test modes will redirect the divided down input signals of the phase detector to the lock detect pin where they can be verified. (See the datasheet for details.)

Receive path

Q: How do I determine the Rx voltage gain?

A: The receive voltage gain is defined as $G_v = 20 \log (V_{outrms}/V_{inrms})$. Program the IC for maximum Rx gain and increase the input power to the RF_{in} port until a $1V_{p-p}$ output is obtained. V_{outrms} in the above equation is then equal to $(1V_{p-p}/2)*0.707$. Next, V_{inrms} needs to be determined. The rms voltage at the RF_{in} port and the primary of the balun transformer is equal to $V_{portrms}$ = [10^(Pin/10)*0.05]^1/2 where Pin is given in dBm. The 1:4 impedance balun transformer will double this primary input voltage at the secondary. The next item to be determined is how much of this rms voltage at the secondary terminals is dropped across the Rx differential input pins. The differential input impedance between these pins is given in the datasheet as 6.6 kΩ//0.7 pF. This impedance and all impedance's parallel to it (i.e., 5.1 kΩ resistor and 100 nH inductor) represent approximately 160 Ω impedance at 352 MHz. The voltage at the secondary of the balun transformer is dropped across this 160 Ω and the impedance of the two 1.8 pF capacitors, which represent approximately 500 Ω at 352 MHz. So, 160/660 of the voltage at the secondary is dropped across the Rx input pins. When all of the above is considered, a rough approximation of V_{inrms} is approximately equal to $^1/_2$ of the rms voltage at the port. One other factor that should also be accounted for is approximately 0.5 dB of insertion loss through the transformer.

Example calculation for a –80 dBm input at 352 MHz to obtain a $1V_{p-p}$ output:

$$Gv = 20\log\frac{\left[\frac{1V_{p-p}}{2} * 0.707\right]}{\sqrt{10\left(\frac{(-80-0.5)}{10}\right)}} * 2 * \left(\frac{160}{660}\right) = 90.8dB$$

Q: Why is the Rx RF input return loss not optimized?

A: The SA1630 has several dB of margin from its max AGC Rx voltage gain specification. If too large of a signal reaches the RF Rx input the part will have trouble meeting its distortion specification. So, the RF input match was detuned to allow the part to more easily meet both of these specifications.

Q: Why is the Rx mode current higher than the Tx current?

A: If the SA1630 is programmed for maximum gain, the Rx mode current will include a substantial amount of power delivered to the multiple gain stages.

Q: What are the external AGC program voltages for maximum and minimum AGC gain?

A: AGCmax = C0 – C5 all low
AGCmin = C0 = low, C1–C5 = high.

Q: Why am I not able to obtain the expected AGC gain when using the external programming pins?

A: Incorrect levels placed at pins 7–12 is the most frequent cause for this problem. The OFF position on the 10 switch DIP package corresponds to placing a high voltage on the pin. **The OFF designator on the DIP package should be ignored** because it often causes the user to program the gain control pins in the opposite state they intended. The pin voltage levels can be easily verified at the test point posts provided.

Q: Why is the board not meeting the 3% THD specification?

A: The first thing to note is that the 3% distortion specification for the SA1630 is not "total harmonic distortion". The ATE testing of this device measures the fundamental and the first three harmonics only. When measuring this parameter, care should be taken to ensure that the Rx output is not being loaded by your test equipment. This can be done by connecting an active FET probe between the Rx output connection and the spectrum analyzer.

Q: Why is my board not meeting the 1.0 V_{p-p} output drive specification?

A: As mentioned above, care should be taken not to load the output with a 50 Ω test equipment port. Also, if you are in the AGCmin setting, note that the output drive specification for this AGC setting is specified lower than for the other settings.

Q: What is the impedance transformation of the Rx input balun?

A: The impedance transformation is 4:1.

Q: Why is the frequency response of the Rx path discontinuous while measuring Rx bandwidth?

A: An SMA connector is provided at the Rx output for convenient connection for monitoring the Rx output signal on a spectrum analyzer. However, this is not suggested for measuring the bandwidth of the Rx path because the excessive loading by the 50 Ω test equipment will cause the frequency response to be erratic. To avoid this excessive loading, this measurement should be done by connecting an active FET probe between the spectrum analyzer and the Rx output test point post.

Transmit path

Q: How do I determine the quadrature phase error of the IC?

A: First you must calibrate the input tones using a phase gain meter prior to injecting them into the Tx input ports. Note what the relative phase between the I and Q signal generators is. Next, adjust the phase difference between I and Q until the suppressed sideband reaches its minimum. The difference between the original phase setting and this new phase setting represents the quadrature phase error of the IC.

Q: Why am I not obtaining the single sideband suppressed carrier output I expect?

A: In general, degradation in sideband suppression is caused by either mismatched gain or quadrature phase error between the I and Q channels. Test modes are available which allow you to operate each channel independently. This allows you to verify that both the I and Q channels are operational. Make sure that you are not in one of these test modes while trying to measure sideband suppression. Operating just the I or Q channel by itself yields a double sideband output. Carrier suppression can be degraded if a DC differential voltage exists at the Tx baseband inputs. Check to make sure the Tx baseband input DC bias voltage (approximately $V_{CC}/2$) is properly connected to the center taps of the balun transformers.

Q: What power at the Tx input port do I need to supply to ensure 1 V_{p-p} at the input pins?

A: The transmit I and Q input each have a shunt 50 Ω resistor to allow the voltage calculations to be made directly from the power indicated on the signal generator. 1 V_{p-p} = 353.33 mVrms is required across the input pins. The balun transformer turns ratio is 4:1. So, the required voltage across the resistor at the primary of the balun is 353.33 mVrms/4 = 88.39 mVrms. The required power from the signal generator is approximately:

$$\text{PindBm} = \frac{10\log\left(\frac{353.33\text{mV}_{rms}}{4}\right)^2}{(50\Omega * 1\text{mW})} - 0.5\text{dB}$$

insertion loss of transformer = –7.6 dBm

Q: How do I measure Irms output current?

A: Irms output current is obtained from a power measurement at the Tx output. It is calculated using the following equation:

$$I_{rms} = \sqrt{10^{\left(\frac{P_{out}}{10}\right)} * \frac{1\text{mW}}{(\text{load presented to the Tx pins} = \text{approx. } 117\Omega)}}$$

Q: What is the impedance transformation of the Tx input balun?

A: The impedance transformation is 16:1.

Q: What is the impedance transformation of the Tx output balun?

A: The impedance transformation is 4:1.

Other areas of concern

Q: Why is the supply current greater than that specified in the datasheet?

A: The common V_{CC} connection supplies not only the SA1630, but also supplies power to the on-board VCO and other circuitry. Also, keep in mind that the supply current in Rx mode will be higher if any of the gain control stages have been turned on.

Q: Why are there two Transmit operation modes?

A: One transmit mode completely shuts down the Rx bias circuitry to save power. The other transmit mode allows the Rx bias circuitry to remain powered up to enable quick Tx to Rx transitions by keeping the Rx output ac coupling capacitors charged.

Q: How can I determine the insertion loss of a balun transformer?

A: The best method is to connect two baluns back to back. This enables you to make a simple two port insertion loss measurement using a spectrum analyzer or network analyzer.

Q: The specified Tx noise floor is below the noise floor of my spectrum analyzer. How can I measure this parameter?

A: This can be done by placing an additional low noise amplifier in the measurement system between the Tx output of the SA1630 and the input to the spectrum analyzer. This effectively reduces the noise floor of the measurement system, thus allowing the measurement to be made.

Q: What data rates can be demodulated using this part?

A: The data rate is dependent on the modulation scheme used. With modulation schemes which deliver multiple bits/symbol, the SA1630 can support data rates in excess of 11 Mbps.

Q: How do I evaluate the current consumption of an individual circuit block of this IC?

A: Sometimes systems do not require all of the functionality provided by the SA1630 and evaluating the power consumption of individual portions of the IC becomes important. All seven of the V_{CC} supply pins on the IC are ganged together and connected to the common supply connection post through 0 Ω resistors R33,34,35,36,37,38 and 39 on the backside of the PCB. Each of these V_{CC} supply pins are also connected to one of the pins of the 8-pin header connector on the topside of the PCB. To evaluate the current consumption of a particular circuit block you simply remove the appropriate resistor on the backside of the PCB and connect a separate power supply and current meter to the associated 8-pin header pin on the topside of the PCB. Table 2 summarizes the associated V_{CC} supply pins, 8-pin header pins and 0 Ω resistors.

Table 2.

SUPPLY DESCRIPTION	IC PIN	8-PIN HEADER PIN	0 Ω RESISTOR
Vbias TXIN	N/A	1	No resistor
V_{CC} BB	15	2	33
V_{CC} VGA24	1	3	34
V_{CC} VGA	2	4	35
V_{CC} CP	34	5	36
V_{CC} TXRX	39	6	37
V_{CC} VCO	N/A	7	38
V_{CC} DIG	22	8	39

HIGH FREQUENCY PIN IMPEDANCE INFORMATION

Figures 20, 21, and 22 are graphs of the equivalent differential impedance for the receiver input, transmit output, and local oscillator differential input ports. This information is provided to facilitate the process of designing this part into your system and can also be of use to those of you making use of design simulation tools.

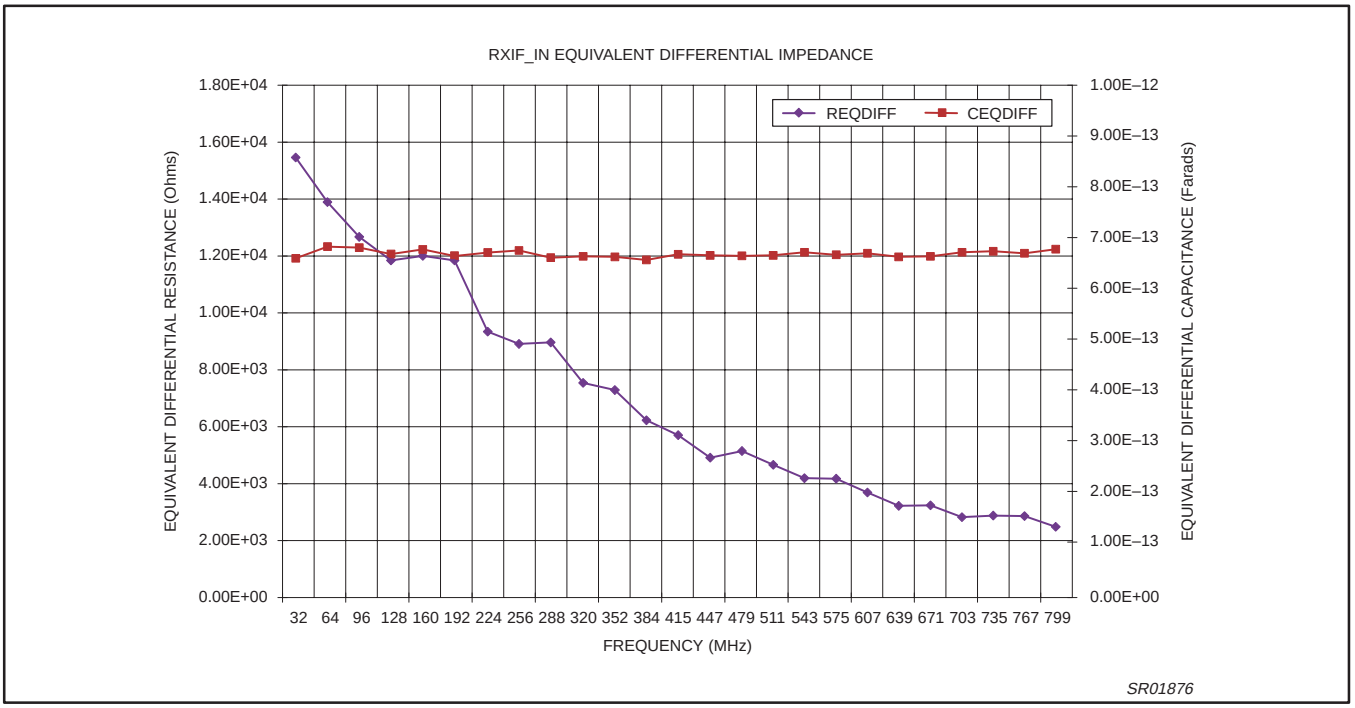

Figure 20. Rx input equivalent differential impedance variation over frequency

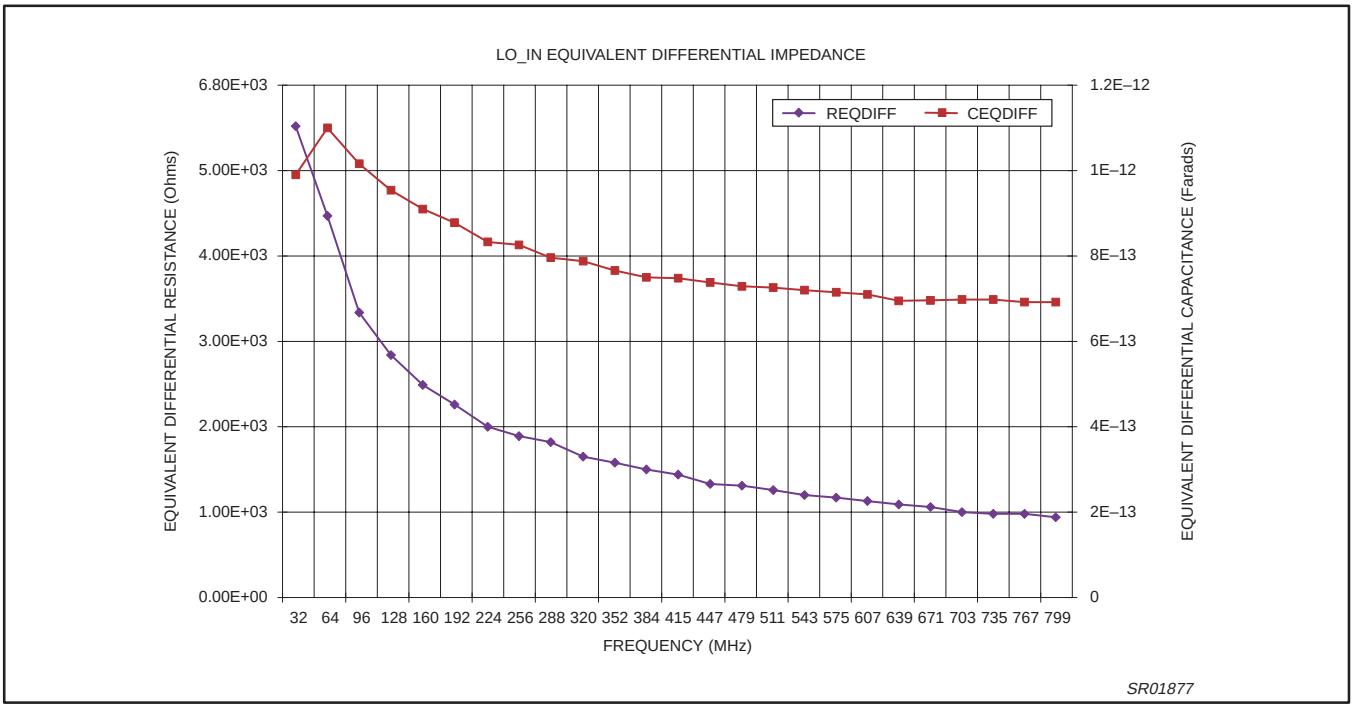

Figure 21. Tx output equivalent differential impedance variation over frequency

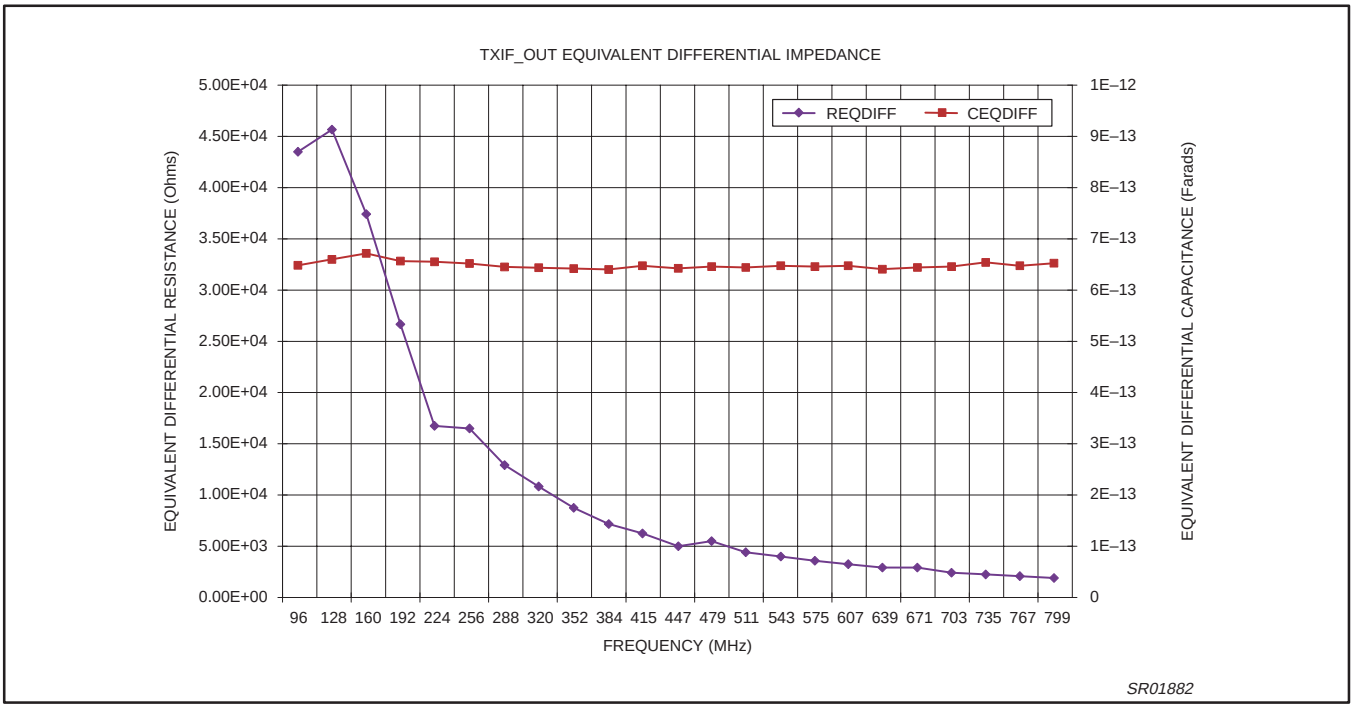

Figure 22. LO input equivalent differential impedance variation over frequency

QUANTITATIVE ANALYSIS RELATING I/Q MODULATION ERROR SOURCES TO CARRIER AND SIDEBAND SUPPRESSION PERFORMANCE SPECIFICATIONS

I/Q modulation description: What is I and Q; why do we use it, and how do we create it?

When a low frequency baseband signal containing the information to be sent through the communication channel is upconverted to a higher frequency carrier signal by mixing it with a local oscillator signal at the carrier frequency, the resulting output frequency spectrum will contain spectral content at the carrier frequency and two sidebands separated from the carrier by an offset equal to the original baseband frequency.

The information in the original baseband signal is fully contained in each of the sidebands. So the power and spectrum containing the carrier and the opposite sideband is essentially wasted. I/Q modulation is a method of creating the desired single sideband suppressed carrier output.

The I/Q modulated transmit output signal is created by sending the in-phase (I) baseband signal to a mixer to be multiplied by an in-phase local oscillator. The quadrature (Q) baseband signal is sent to another mixer to be multiplied by a quadrature local oscillator. The transmit output signal is simply the summed outputs of these two mixers. This is shown in Figure 23.

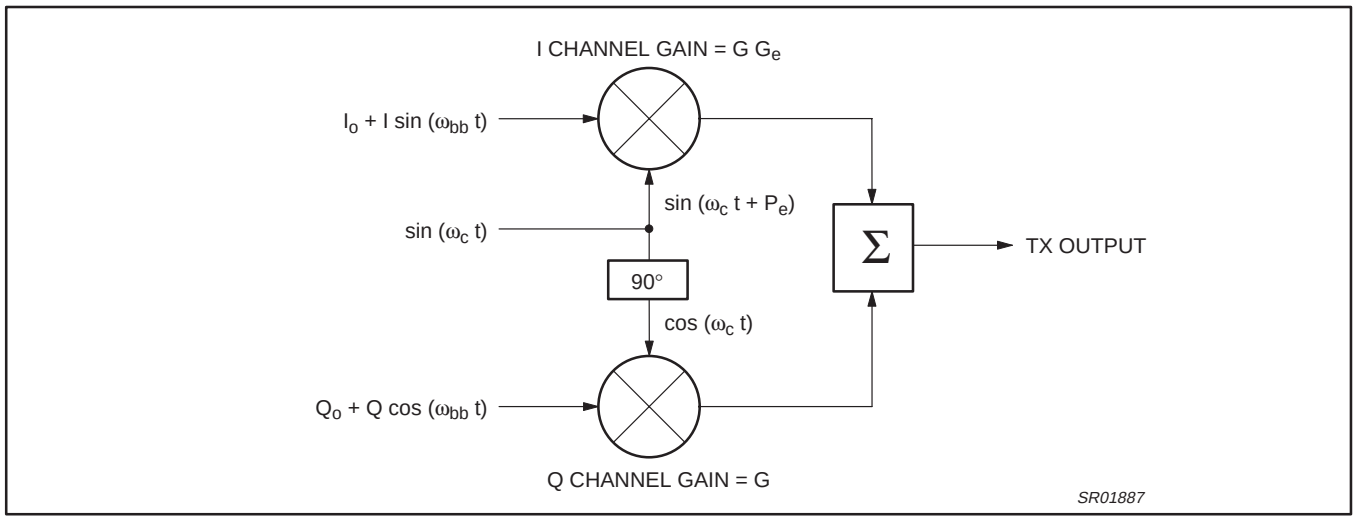

Figure 23. showing a conceptual schematic of I/Q modulation circuitry

Quantitative analysis

The following is a very detailed quantitative analysis of the relationships between amplitude mismatch and quadrature phase error on carrier and sideband suppression. Additional insight is obtained by considering several different scenarios and sets of assumptions. The various results are then compared against each other and also against the SA1630 datasheet specifications for carrier and sideband suppression. It is meant for those interested in how these types of relationships are derived and therefore all calculation steps have been included for this reason. If these derivations are not of interest to you, equations (130), (132) and Figures 24, 25, and 26 provide a reasonable summarization of the results of this analysis.

The in-phase and quadrature baseband input signals are defined by:

$I(0) + I \sin \omega_{bb} t$

$Q(0) + Q \cos \omega_{bb} t$

Where

I(0) and Q(0) represent DC offsets

I and Q represent the ac magnitude of the baseband signals

$\omega bb = 2 * \pi * F_{bb}$

Fbb represents the baseband frequency

t represents time

The gain and phase error will be arbitrarily assigned to the in-phase channel.

The gain of the in-phase channel mixer is therefore defined by $G * G_e$, where G is the gain of the in-phase and quadrature mixers, and G_e is the in-phase mixer gain and/or baseband input amplitude mismatch error ratio relative to the quadrature mixer gain and/or baseband input amplitude. $G_e = 1$ would indicate perfectly matched baseband input signal amplitudes and mixer gains.

The in-phase and quadrature local oscillator signals are defined by:

$\sin (\omega_c + \Theta)$ and $\cos (\omega_c t)$, respectively.

Where

$\omega_c = 2 * \pi * F_c$

F_c represents the local oscillator and/or carrier frequency.

Θ is the quadrature phase error relative to the quadrature local oscillator signal.

t represents time.

Summary of trigonometric relationships

Angle sum and difference relations

$\sin (a+b) = \sin a \cos b + \cos a \sin b$ (4)

$\sin (a–b) = \sin a \cos b – \cos a \sin b$ (5)

$\cos (a+b) = \cos a \cos b – \sin a \sin b$ (6)

$\cos (a–b) = \cos a \cos b + \sin a \sin b$ (7)

Function product relations

$\sin a \sin b = {}^1/_2 \cos (a–b) – {}^1/_2 \cos (a+b)$ (8)

$\cos a \cos b = {}^1/_2 \cos (a–b) + {}^1/_2 \cos (a+b)$ (9)

$\sin a \cos b = {}^1/_2 \sin (a+b) + {}^1/_2 \sin (a–b)$ (10)

$\cos a \sin b = {}^1/_2 \sin (a+b) + {}^1/_2 \sin (a–b)$ (11)

Function sum and difference relations

$\sin a + \sin b = 2 \sin {}^1/_2 (a+b) \cos {}^1/_2 (a–b)$ (12)

$\sin a – \sin b = 2 \cos {}^1/_2 (a+b) \sin {}^1/_2 (a–b)$ (13)

$\cos a + \cos b = 2 \cos {}^1/_2 (a+b) \cos {}^1/_2 (a–b)$ (14)

$\cos a – \cos b = – 2 \sin {}^1/_2 (a+b) \sin {}^1/_2 (a–b)$ (15)

Pythagorean relation

$(\sin a)^2 + (\cos a)^2 = 1$ (16)

Half angle relations

$$\sin\left(\frac{a}{2}\right) = \pm \sqrt{\frac{1 - \cos a}{2}} \quad (17)$$

$$\cos\left(\frac{a}{2}\right) = \pm \sqrt{\frac{1 + \cos a}{2}} \quad (18)$$

Small angle approximations

$\sin a = a$ (19)

$\cos a = 1$ (20)

where “a” is given in radians.

Function properties

$\sin –a = –\sin a$ (21)

$\cos –a = \cos a$ (22)

I channel mixer output calculation

The in-phase channel mixer output is then:

$$\text{I mixer output} = [I(0) + I \sin \omega bb\ t] * [GG_e \sin (\omega_c t + \Theta)] \quad (23)$$

Using the trigonometric identity in Equation (4), $\sin (\omega_c + \Theta)\ t$ can be rewritten as:

$$\text{Sin } (\omega_c t + \Theta) = \sin \omega_c t \cos \Theta + \cos \omega_c t \sin \Theta \quad (24)$$

Substituting Equation (24) into Equation (23) gives:

$$\text{I mixer output} = [I(0) + I \sin \omega_{bb} t] * [GG_e \cos \Theta \sin \omega_c t + GG_e \sin \Theta \cos \omega_c t] \quad (25)$$

Expanding Equation (25) gives:

$$\text{I mixer output} = I(0)\ GG_e \cos \Theta \sin \omega_c t + I(0)\ GG_e \sin \Theta \cos \omega_c t + I\ GG_e \cos \Theta \sin \omega_{bb} t \sin \omega_c t + I\ GG_e \sin \Theta \sin \omega_{bb} t \cos \omega_c t \quad (26)$$

Using the identity in Equation (8)

$$\sin \omega_{bb} t \sin \omega_c t = {}^1/_2 \cos (\omega_{bb} t - \omega_c t) - {}^1/_2 \cos (\omega_{bb} t + \omega_c t) \quad (27)$$

Using the function property in Equation (22) allows Equation (27) to be rewritten as:

$$\sin \omega_{bb} t \sin \omega_c t = {}^1/_2 \cos (\omega_c t - \omega_{bb} t) - {}^1/_2 \cos (\omega_c t + \omega_{bb} t) \quad (28)$$

Using the identity in Equation (10)

$$\sin \omega_{bb} t \cos \omega_c t = {}^1/_2 \sin (\omega_{bb} t + \omega_c t) + {}^1/_2 \sin (\omega_{bb} t - \omega_c t) \quad (29)$$

Using the function property in Equation (21) allows Equation (29) to be rewritten as:

$$\sin \omega_{bb} t \cos \omega_c t = {}^1/_2 \sin (\omega_c t + \omega_{bb} t) - {}^1/_2 \sin (\omega_c t - \omega_{bb} t) \quad (30)$$

Substituting (28) and (30) into (26) and defining the following:

$$A = {}^1/_2\ GG_e \cos \Theta$$

$$B = {}^1/_2\ GG_e \sin \Theta$$

$$\omega_h = \omega_c + \omega_{bb}$$

$$\omega_l = \omega_c - \omega_{bb}$$

gives the following:

$$\text{I mixer output} = 2A\ I(0) \sin \omega_c t + 2B\ I(0) \cos \omega_c t + A\ I \cos \omega_l t - A\ I \cos \omega_h t + B\ I \sin \omega_h t - B\ I \sin \omega_l t \quad (31)$$

Q channel mixer output calculation

The quadrature channel mixer output is much easier to derive because we have associated all the gain and phase error terms with the I channel mixer. The quadrature channel mixer output is:

$$\text{Q mixer output} = [Q(0) + Q \cos \omega_{bb} t] * [G \cos \omega_c t] \quad (32)$$

Expanding Equation (32) gives:

$$\text{Q mixer output} = G\ Q(0) \cos \omega_c t + G\ Q \cos \omega_{bb} t \cos \omega_c t \quad (33)$$

Using the trigonometric function product relation in Equation (9)

$$\text{Q mixer output} = G\ Q(0) \cos \omega_c t + G\ Q\ [{}^1/_2 \cos (\omega_{bb} t - \omega_c t) + {}^1/_2 \cos (\omega_{bb} t + \omega_c t)] \quad (34)$$

Using the function properties given in Equations (21) and (22), Equation (33) can be rewritten as:

$$\text{Q mixer output} = G\ Q(0) \cos \omega_c t + G\ Q\ {}^1/_2 \cos (\omega_c t - \omega_{bb} t) + G\ Q\ {}^1/_2 \cos (\omega_c t + \omega_{bb} t) \quad (35)$$

Inserting the definitions for ω_l and ω_h given previously yields:

$$\text{Q mixer output} = G\ Q(0) \cos \omega_c t + {}^1/_2\ G\ Q \cos \omega_l t + {}^1/_2\ G\ Q \cos \omega_h t \quad (36)$$

Transmit output equations

The transmit output is simply the I mixer output summed with the Q mixer output. Combining Equations (31) and (36) gives:

$$\text{Tx output} = 2A\,I(0)\sin\omega_c t + 2B\,I(0)\cos\omega_c t + A\,I\cos\omega_l t - A\,I\cos\omega_h t + B\,I\sin\omega_h t - B\,I\sin\omega_l t + G\,Q(0)\cos\omega_c t + {}^1/_2\,G\,Q\cos\omega_l t + {}^1/_2\,G\,Q\cos\omega_h t \quad (37)$$

From this equation we can group the terms by frequency. There are three different frequencies: the upper sideband ω_h; the lower sideband ω_l; and the carrier frequency ω_c.

$$\text{Tx output} = \text{Carrier (C)} + \text{upper sideband (USB)} + \text{lower sideband (LSB)} \quad (38)$$

$$C = 2A\,I(0)\sin\omega_c t + 2B\,I(0)\cos\omega_c t + G\,Q(0)\cos\omega_c t \quad (39)$$

$$USB = -A\,I\cos\omega_h t + B\,I\sin\omega_h t + {}^1/_2\,G\,Q\cos\omega_h t \quad (40)$$

$$LSB = A\,I\cos\omega_l t - B\,I\sin\omega_l t + {}^1/_2\,G\,Q\cos\omega_l t \quad (41)$$

Where again A and B are the factors which incorporate the gain and phase error and are defined as:

$$A = {}^1/_2\,GG_e\cos\Theta \quad (42)$$

$$B = {}^1/_2\,GG_e\sin\Theta \quad (43)$$

$$\omega_h = \omega_c + \omega_{bb} \quad (44)$$

$$\omega_l = \omega_c - \omega_{bb} \quad (45)$$

Ideal case

In order to gain some insight into how this Tx modulation scheme provides the required single-sideband suppressed carrier output signal, let's first take a look at the Tx output equations under ideal conditions.

Let's assume the following:

$G_e = 1$ (channel mixer gains and baseband input signal amplitudes are perfectly matched) (46)

$\Theta = 0$ (there is no quadrature phase error) (47)

$I(0) = Q(0) = 0$ (there is no input offset error) (48)

$I = Q = M$ (the baseband input signal amplitudes are equal) (49)

Substituting Equations (46) and (47) into Equations (42) and (43) gives:

$$A = {}^1/_2\,G * 1 * \cos 0 = {}^1/_2\,G \quad (50)$$

$$B = {}^1/_2\,G * 1 * \sin 0 = 0 \quad (51)$$

Substituting Equation (48) into Equation (39) gives:

$$C = 0 + 0 + 0 = 0 \quad (52)$$

Substituting Equations (49), (50), and (51) into equation (40) gives:

$$USB = -{}^1/_2\,G\,M\cos\omega_h t + 0 + {}^1/_2\,G\,M\cos\omega_h t = 0 \quad (53)$$

Substituting Equations (49), (50), and (51) into equation (41) gives:

$$LSB = +{}^1/_2\,G\,M\cos\omega_l t - 0 + {}^1/_2\,G\,M\cos\omega_l t = G\,M\cos\omega_l t \quad (54)$$

Equations (52), (53), and (54) suggest that under "ideal" conditions, the resulting transmit output signal contains the single lower sideband signal with a magnitude equal to the magnitude of the ac input signal times the mixer gain. They also show that the carrier and upper sideband signals are completely suppressed!

OBTAINING INSIGHT BY CONSIDERING AMPLITUDE AND PHASE ERRORS SEPARATELY

Mixer gain mismatch and/or baseband input signal amplitude mismatch error only

First, it should be noted in the transmit output Equations (39), (40), and (41) that the baseband input signal amplitudes I and Q are always multiplied by the mixer gain G. Therefore, the amplitude mismatch error ratio term G_e represents not only just the mixer gain mismatch error, but the combination of mixer gain mismatch error and baseband input signal amplitude mismatch error.

To gain some further insight into the effect of mixer gain mismatch and/or baseband input signal amplitude mismatch error on the transmit output signal, let's again rewrite the transmit output equations without assuming that this error term is ideal. Let's now assume the following:

G_e not = 1 (channel mixer gains are **NOT** perfectly matched) (55)

$\Theta = 0$ (there is no quadrature phase error) (56)

$I(0) = Q(0) = 0$ (there is no input offset error) (57)

$I = Q = M$ (the baseband input signal amplitudes are equal (58)

Substituting Equations (55) and (56) into Equations (42) and (43) yields:

$A = {}^1/_2\ G\ G_e \cos 0 = {}^1/_2\ G\ G_e$ (59)

$B = {}^1/_2\ G\ G_e \sin 0 = 0$ (60)

Substituting Equations (57), (58), (59) and (60) into Equations (39), (40), and (41) gives:

$C = 0 + 0 + 0 = 0$ (61)

$USB = -{}^1/_2\ G\ G_e\ M \cos \omega_h t + 0 + {}^1/_2\ G\ M \cos \omega_h t = {}^1/_2\ G\ M\ (1-G_e) \cos \omega_h t$ (62)

$LSB = {}^1/_2\ G\ G_e\ M \cos \omega_l t - 0 + {}^1/_2\ G\ M \cos \omega_l t = {}^1/_2\ G\ M\ (1+G_e) \cos \omega_l t$ (63)

Equation (61) shows that if baseband input signal amplitude and/or mixer gain mismatch are the only errors in the system, the carrier suppression performance is unaffected.

Equations (62) and (63) show that if the amplitude mismatch error ratio is significantly less than 1, then the USB signal will no longer be completely cancelled, and the LSB signal amplitude will be significantly less than G M.

Let's now relate these equations to the datasheet specifications.

$$\text{Sideband Suppression(SBS)} = 20 \log\left[\frac{\text{mag(USB)}}{\text{mag(LSB)}}\right] \quad (64)$$

$mag\ (USB) = {}^1/_2\ G\ M\ (1-G_e)$ (65)

$mag\ (LSB) = {}^1/_2\ G\ M\ (1+G_e)$ (66)

Substituting Equations (65) and (66) into Equation (64) gives:

$$SBS = 20 \log\left[\frac{(1 - G_e)}{(1 + G_e)}\right] \quad (67)$$

Solving Equation (67) for G_e as a function of SBS yields:

$$G_e = \frac{(1 - K)}{(1 + K)} \quad \text{where } K = 10^{(SBS/20)} \quad (68)$$

The SA1630 datasheet specifies that the minimum sideband suppression is –35dB. Substituting this into Equation (68) gives a maximum amplitude mismatch error ratio of 0.965, which says that the combined baseband amplitude mismatch and mixer gain mismatch error must be less than

$20 \log G_e = 20 \log 0.965 = 0.3\ dB$ (69)

assuming there are no other errors in the system. Practically speaking, phase error is also a significant source of error that affects SBS performance, and therefore the amplitude mismatch error requirement is much more stringent than indicated here.

Quadrature phase error only

So, now let's take a look at the effects of quadrature phase error by itself, while assuming all the other sources of error are ideal. This is done by assuming the following:

$G_e = 1$ (channel mixer gains and baseband input signal amplitudes are perfectly matched) (70)

Θ **not = 0 (quadrature phase error)** (71)

I(0) = Q(0) = 0 (there is no input offset error) (72)

I = Q = M (the baseband input signal amplitudes are equal) (73)

Substituting Equations (70) and (71) into Equations (42) and (43) gives:

$A = {}^1/_2\ G * 1 * \cos\Theta = {}^1/_2\ G \cos\Theta$ (74)

$B = {}^1/_2\ G * 1 * \sin\Theta = {}^1/_2\ G \sin\Theta$ (75)

Substituting Equations (72), (73), (74), and (75) into Equations (39), (40), and (41) yields:

$C = 0 + 0 + 0 = 0$ (76)

$USB = -{}^1/_2\ G\ M \cos\Theta \cos\omega_h t + {}^1/_2\ G\ M \sin\Theta \sin\omega_h t + {}^1/_2\ G\ M \cos\omega_h t$ (77)

$LSB = {}^1/_2\ G\ M \cos\Theta \cos\omega_l t - {}^1/_2\ G\ M \sin\Theta \sin\omega_l t + {}^1/_2\ G\ M \cos\omega_l t$ (78)

Grouping the phase error terms together in Equation (77) gives:

$USB = -{}^1/_2\ G\ M (\cos\Theta \cos\omega_h t - \sin\Theta \sin\omega_h t) + {}^1/_2\ G\ M \cos\omega_h t$ (79)

Using the trigonometric angle sum and difference relation in Equation (6) yields:

$USB = -{}^1/_2\ G\ M [\cos(\Theta + \omega_h t) - \cos\omega_h t]$ (80)

Applying the trigonometric function sum and difference relation in Equation (15) gives:

$USB = -{}^1/_2\ G\ M [-2 \sin {}^1/_2 (\Theta + \omega_h t + \omega_h t) \sin {}^1/_2 (\Theta + \omega_h t - \omega_h t)]$ (81)

Collecting terms gives:

$USB = G\ M [\sin(\omega_h t + \Theta/2)] (\sin\Theta/2)$ (82)

Applying the small angle approximation in Equation (19) yields:

$$USB = GM\left(\frac{\theta}{2}\right)\sin\left(\omega_h t + \frac{\theta}{2}\right)$$ (83)

Now let's work on the LSB equation in a similar fashion. Grouping the phase error terms in Equation (78) together yields:

$LSB = {}^1/_2\ G\ M (\cos\Theta \cos\omega_l t - \sin\Theta \sin\omega l t) + {}^1/_2\ G\ M \cos\omega_l t$ (84)

Again, using the trigonometric angle sum and difference relation in Equation (6) yields:

$LSB = {}^1/_2\ G\ M [\cos(\Theta + \omega_l t) + \cos\omega_l t]$ (85)

Using the trigonometric function sum and difference relation in Equation (14) gives:

$LSB = {}^1/_2\ G\ M [2 \cos {}^1/_2\ (\Theta + \omega_l t + \omega_l t) \cos {}^1/_2 (\Theta + \omega_l t - \omega_l t)]$ (86)

Collecting terms yields:

$LSB = G\ M \cos(\Theta/2) \cos(\omega_l t + \Theta/2)$ (87)

Applying the small angle approximation in Equation (20) gives:

$LSB = G\ M \cos(\omega l t + \Theta/2)$ (88)

Now let's compare these equation to the datasheet specifications.

From Equations (83) and (88) :

mag (USB) = G M (Θ/2) (89)

mag (LSB) = G M (90)

Substituting Equations (89) and (90) into Equation (64) gives:

$SBS = 20 \log [G\ M (\Theta/2) / G\ M] = 20 \log (\Theta/2)$ (91)

If the phase error is given in degrees instead of radians

$SBS = 20 \log (\Theta * \pi/360)$ (92)

Solving Equation (92) for phase error yields:

$$\Theta = (K * 360) / \pi \text{ where } K = 10^{(SBS/20)} \quad (93)$$

The datasheet minimum sideband suppression specification is –35 dBc. Inserting this into Equation (93) shows that the maximum amount of quadrature phase error that can be tolerated while still meeting datasheet specifications and assuming there are no other errors in the system is

$$\Theta = 2.0 \text{ degrees} \quad (94)$$

As shown previously, amplitude mismatch errors also contribute to decreasing sideband suppression performance, and therefore the actual maximum amount of phase error that can be tolerated should be somewhat less than this.

Offset error only

In the discussions above, Equations (40) and (41) show the sideband frequency content as being independent of the offset error terms I(0) and Q(0) and the offset error terms affect the carrier suppression performance only. So, Equation (39) need only be considered when evaluating the effect of offset errors while assuming ideal quadrature phase and amplitude matching conditions. With this in mind, let's make the following assumptions:

$G_e = 1$ (channel mixer gains and baseband input signal amplitudes are perfectly matched) (95)

$\Theta = 0$ (there is no quadrature phase error) (96)

I(0) not = Q(0) not = 0 (input offset error) (97)

I = Q = M (the baseband input signal amplitudes are equal) (98)

Substituting Equations (95) and (96) into Equations (42) and (43) gives:

$$A = {}^1/_2\, G * 1 * \cos 0 = {}^1/_2\, G \quad (99)$$

$$B = {}^1/_2\, G * 1 * \sin 0 = 0 \quad (100)$$

Substituting Equations (97), (98), (99), and (100) into Equation (39) yields:

$$C = 2\ {}^1/_2\, G\, I(0) \sin \omega_c t + 0 + G\, Q(0) \cos \omega_c t = G\, I(0) \sin \omega_c t + G\, Q(0) \cos \omega_c t \quad (101)$$

$$\text{Carrier Suppression(CS)} = 20 \log\left[\frac{\text{mag(C)}}{\text{mag(LSB)}}\right] \quad (102)$$

The expression for LSB under ideal quadrature phase and amplitude matching conditions is shown in Equation (54).
From Equations (54) and (101):

$$\text{mag(C)} = G\sqrt{I(0)^2 + Q(0)^2} \quad (103)$$

$$\text{mag (LSB)} = G\, M \quad (104)$$

Substituting Equations (103) and (104) into Equation (102) gives:

$$CS = 20 \log\left[\frac{G\sqrt{I(0)^2 + Q(0)^2}}{GM}\right] = 20 \log\left[\frac{\sqrt{I(0)^2 + Q(0)^2}}{M}\right] \quad (105)$$

Let's compare this equation to the SA1630 datasheet specifications for carrier suppression and differential peak-to-peak baseband input level.

If we assume that the I(0) and Q(0) are equal:

$$X(0) = I(0) = Q(0) \quad (106)$$

Substitute Equation (106) into Equation (105) and solve for an expression relating the maximum offset error as a function of carrier suppression and input signal amplitude yields:

$$X(0) = \frac{KM}{\sqrt{2}} \quad \text{where } K = 10^{(CS/20)} \quad (107)$$

Relating the RMS voltage M to an equivalent differential peak-to-peak baseband input level gives:

$$M = \left(\frac{V_{p-p}}{2}\right) * \left(\frac{1}{\sqrt{2}}\right) \quad (108)$$

Substituting Equation (108) into Equation (107) gives:

$$X(0) = K\frac{V_{p-p}}{4} \quad \text{where again } K = 10^{(CS/20)} \quad (109)$$

The datasheet specifies a minimum of –30 dBc of carrier suppression with a differential input amplitude of 1 V_{p-p}. Substituting these values into Equation (109) gives:

$$X(0) = \frac{[1V_{p-p} * 10^{(-30/20)}]}{4} = 7.9mV \quad (110)$$

Equation (110) tells us that for an ac input amplitude of $1V_{p-p}$, if the DC input offsets I(0) and Q(0) are assumed equal, and we assume ideal quadrature phase and amplitude matching, the maximum DC offset allowed at the baseband inputs in order to meet the –30 dBc carrier suppression specification is 7.9 mV. This value is most likely optimistic, but serves as an excellent reference when we look at the effects of quadrature phase error and amplitude mismatch error on carrier suppression.

MORE PRACTICAL CONSIDERATIONS

Now that we have a better understanding of how offset, quadrature phase, and amplitude mismatch errors effect the carrier and sideband suppression performance individually, let's take a more practical look and consider the effects of simultaneous quadrature phase and amplitude mismatch error on both carrier and sideband suppression.

Effect of simultaneous quadrature phase and amplitude errors on the carrier signal

Substituting the small angle approximations of Equations (19) and (20) into Equations (42) and (43) gives:

$$A = {}^1/_2\, G\, G_e \quad (111)$$

$$B = {}^1/_2\, G\, G_e\, \Theta \quad (112)$$

Substituting Equations (111) and (112) into the carrier signal expression Equation (39) gives:

$$C = G\, G_e\, I(0) \sin \omega_c t + G\, G_e\, \Theta\, I(0) \cos \omega_c t + G\, Q(0) \cos \omega_c t \quad (113)$$

Grouping terms gives:

$$C = G\, [(G_e\, I(0)) \sin \omega_c t + (G_e\, \Theta\, I(0) + Q(0)) \cos \omega_c t] \quad (114)$$

The magnitude of this signal will then be

$$mag(C) = G \sqrt{(G_e\ I(0))^2 + (G_e\theta\ I(0) + Q(0))^2} \quad (115)$$

If we again assume that the offsets I(0) and Q(0) are equal and substituting Equation (106) into Equation (115) then

$$mag(C) = G \sqrt{(G_e\ X(0))^2 + (G_e\theta\ X(0) + X(0))^2} \quad (116)$$

Expanding Equation (116) gives:

$$mag(C) = G \sqrt{G_e{}^2\ X(0)^2 + (G_e\theta)^2\ X(0)^2 + 2(G_e\theta)\ X(0)^2 + X(0)^2} \quad (117)$$

Pulling the common $X(0)^2$ term out of the square root yields:

$$mag(C) = GX(0) \sqrt{G_e{}^2 + G_e\theta)^2 + 2G_e\theta + 1} \quad (118)$$

Equation (118) shows an expression relating the magnitude of the unwanted carrier signal as a function of input offset error, and the quadrature phase and amplitude mismatch errors are completely contained within the square root term in the equation.

Note that if we assume zero quadrature phase error ($\Theta = 0$) and perfectly matched amplitude and gain ($G_e = 1$), Equation (118) reduces to:

$$mag(C) = GX(0) \sqrt{1^2 + (1 * 0)^2 + 2 * 1 * 0 + 1} = GX(0) \sqrt{2} \quad (119)$$

which agrees with Equation (103) when the offsets I(0) and Q(0) are assumed equal.

The carrier suppression performance cannot yet be evaluated because this value is relative to the wanted sideband signal, which in our case is the LSB signal. So, let's now consider the effects of simultaneous phase error and amplitude error on the upper and lower sideband signals.

EFFECT OF SIMULTANEOUS QUADRATURE PHASE AND AMPLITUDE ERRORS ON THE SIDEBAND SIGNALS

Upper sideband

Again applying the small angle approximations of Equations (19) and (20) to Equations (42) and (43) yields:

$$A = {}^1/_2\ G\ G_e \quad (120)$$

$$B = {}^1/_2\ G\ G_e\ \Theta \quad (121)$$

Substituting Equations (120) and (121) into the expression for the upper sideband signal in Equation (40), and assuming the baseband input signals are equal, I = Q = M (recall, the ac amplitude mismatches are lumped into the mismatch ratio G_e) gives:

$$USB = -{}^1/_2\ G\ G_e\ M \cos \omega_h t + {}^1/_2\ G\ G_e\ \Theta\ M \sin \omega_h t + {}^1/_2\ G\ M \cos \omega_h t \quad (122)$$

Factoring out common terms gives:

$$USB = {}^1/_2\ G\ M\ [G_e\ \Theta \sin \omega_h t + \cos \omega_h t - G_e \cos \omega_h t] \quad (123)$$

Grouping common quadrature component terms gives:

$$USB = {}^1/_2\ G\ M\ [\ (G_e\ \Theta) \sin \omega_h t + (1-G_e) \cos \omega_h t] \quad (124)$$

Therefore,

$$mag(USB) = \frac{1}{2} GM \sqrt{(G_e\theta)^2 + (1 - G_e)^2} \quad (125)$$

Equation (125) shows that the magnitude of the upper sideband signal incorporates a $(1–G_e)$ term due to the effects of amplitude mismatch as was derived in Equation (65), as well as a new $(G_e\ \Theta)$ term which reflects the interaction of having both amplitude mismatch error and quadrature phase error simultaneously.

Also note, if we assume no quadrature phase error ($\Theta = 0$) and perfect baseband signal amplitude and mixer gain matching, Equation (125) still indicates the complete suppression of the upper sideband signal as previously derived in Equation (53).

$$Mag(USB) = \frac{1}{2} GM \sqrt{(1 * 0)^2 + (1 - 1)^2} = 0 \quad (126)$$

Lower sideband

The lower sideband signal can then be analyzed in a similar fashion. Substituting Equations (120) and (121) into the expression for the lower sideband signal in Equation (41) and again assuming the baseband input signals are equal I = Q = M (recall, the ac amplitude mismatches are lumped in to the mismatch ratio, G_e) gives:

$$LSB = {}^1/_2\ G\ G_e\ M \cos \omega_l t - {}^1/_2\ G\ G_e\ \Theta\ M \sin \omega_l t + {}^1/_2\ G\ M \cos \omega_l t \quad (127)$$

Factoring out common terms gives:

$$LSB = {}^1/_2\ G\ M\ [G_e \cos \omega_l t + \cos \omega_l t - G_e\ \Theta \sin \omega_l t] \quad (128)$$

Grouping common quadrature component terms gives:

$$LSB = {}^1/_2\ G\ M\ [(1+G_e) \cos \omega_l t - (G_e\ \Theta) \sin \omega_l t] \quad (129)$$

Therefore,

$$mag(LSB) = \frac{1}{2} GM \sqrt{(1 + G_e)^2 + (G_e\theta)^2} \quad (130)$$

Equation (130) shows that the magnitude of the lower sideband signal incorporates a $(1+G_e)$ term due to the effects of amplitude mismatch as was derived in Equation (66), as well as a new $(G_e\ \Theta)$ term which reflects the interaction of having both amplitude mismatch error and quadrature phase error simultaneously.

Also note, if we assume no quadrature phase error ($\Theta = 0$) and perfect baseband signal amplitude and mixer gain matching, Equation (130) indicates the magnitude of the lower sideband signal is:

$$mag(LSB) = \frac{1}{2} GM \sqrt{(1 + 1)^2 + (1 * 0)^2} = GM \quad (131)$$

as previously derived in Equation (54).

Carrier suppression

Substituting Equations (118) and (130) into Equation (102) gives:

$$CS = 20\log\left\{\frac{GX(0)\sqrt{G_e{}^2 + (G_e\theta)^2 + 2G_e\theta + 1}}{\frac{1}{2}GM\sqrt{(1 + G_e)^2 + (G_e\theta)^2}}\right\} \quad (132)$$

Reducing and rearranging terms yields:

$$CS = 20\log\left[\frac{2X(0)}{M}\right] * \sqrt{\frac{((G_e\theta)^2 + (G_e{}^2 + 1) + (2G_e\theta))}{((G_e\theta)^2 + (G_e{}^2 + 1) + (2G_e))}} \quad (133)$$

Equation (133) shows us a couple of things. First, carrier suppression is a strong function of the DC offset to ac amplitude of the baseband input signal. Secondly, notice that the numerator and denominator of the portion of the equation under the radical are almost identical. They differ by only a factor of Θ in the last term. So, we expect that carrier suppression should be a weak function of quadrature phase noise error and virtually completely insensitive to amplitude mismatch errors.

To verify the strong sensitivity of carrier suppression to the DC offset of the baseband input signal, let's assume some arbitrary values for amplitude mismatch and quadrature phase error and graph this relationship. The graph in Figure 24 shows that approximately 6.5 mV of baseband input DC offset can be tolerated while still meeting the SA1630's –30 dBc carrier suppression specification. Thus, this result which takes into account amplitude mismatch and quadrature phases errors, is somewhat less than that predicted in Equation (110), where these effects were neglected.

To evaluate the relative sensitivity of carrier suppression to amplitude mismatch and quadrature phase error, let's set the baseband DC offset to an arbitrary value of 3 mV and graph this relationship. The graph in Figure 25 shows the carrier suppression varies less than only 0.4 dB while quadrature phase error is varied by as much as 5 degrees and remains nearly constant with changes in amplitude mismatch error.

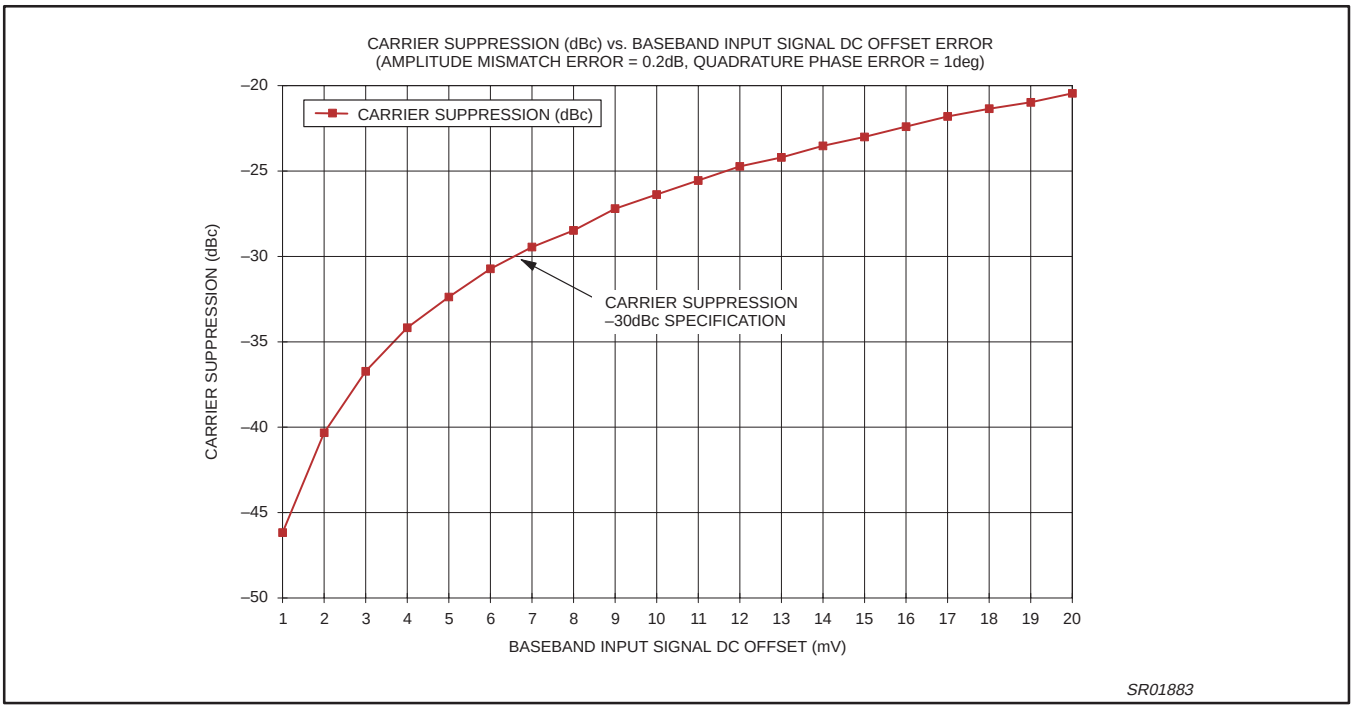

Figure 24. Carrier suppression as a function of baseband input signal DC offset

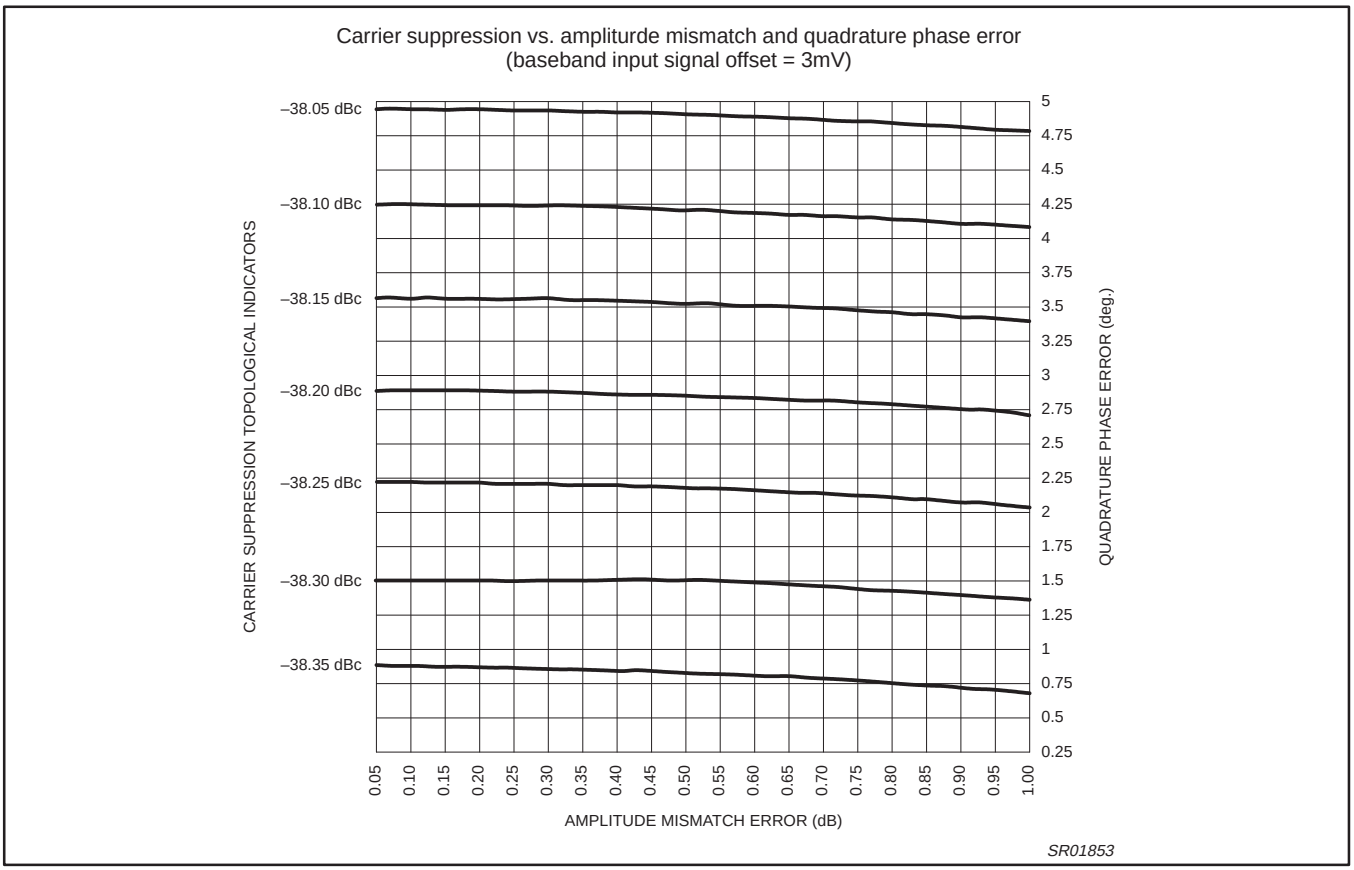

Figure 25. Carrier suppression vs. amplitude mismatch and quadrature phase error

Sideband suppression

An expression relating SBS to amplitude mismatch and quadrature phase error can be obtained by substituting Equations (125) and (130) into Equation (64).

$$SBS = 20\log\frac{\frac{1}{2}GM\sqrt{(G_e\theta)^2 + (1 - G_e)^2}}{\frac{1}{2}GM\sqrt{(1 + G_e)^2 + (G_e\theta)^2}} \quad (134)$$

Reducing and rearranging terms yields:

$$SBS = 20\log\sqrt{\frac{(G_e\theta)^2 + (G_e{}^2 + 1) - 2G_e}{(G_e\theta)^2 + (G_e{}^2 + 1) + 2G_e}} \quad (135)$$

There are some notable differences between this expression for SBS in Equation (135) and the carrier suppression expression in Equation (133). There is no dominating term in front of the radical and it is independent of the magnitude of the baseband input signals. This should make SBS much more sensitive to quadrature phase error and amplitude mismatch errors. The third term in the numerator and denominator in Equation (135) are both a factor of amplitude mismatch, but are of opposite polarity. Thus, SBS should be much more sensitive to amplitude mismatch variation than the case for CS. Indeed, the graph in Figure 26 shows this to be true. Equations (69) and (94) tell us that the SA1630 SBS specification can be met with as much as 2 degrees of quadrature phase error or 0.3 dB of amplitude mismatch, but not both. How much of one can be traded off for the other while still meeting the SA1630 –35 dBc SBS specification can be easily determined from Equation (135) and/or by following the –35 dBc contour curve on the graph in Figure 26.

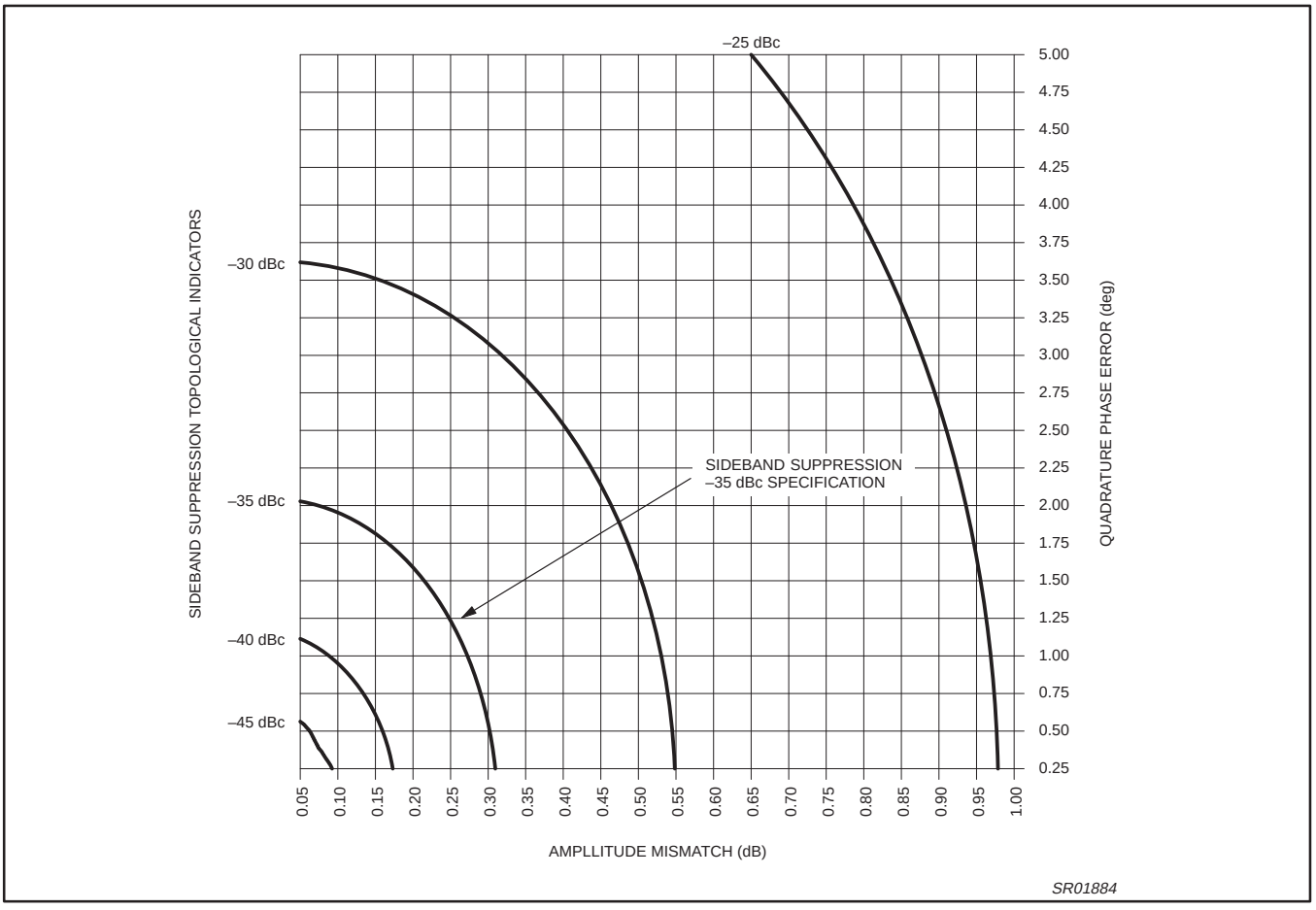

Figure 26. Sideband suppression vs. amplitude mismatch and quadrature phase error

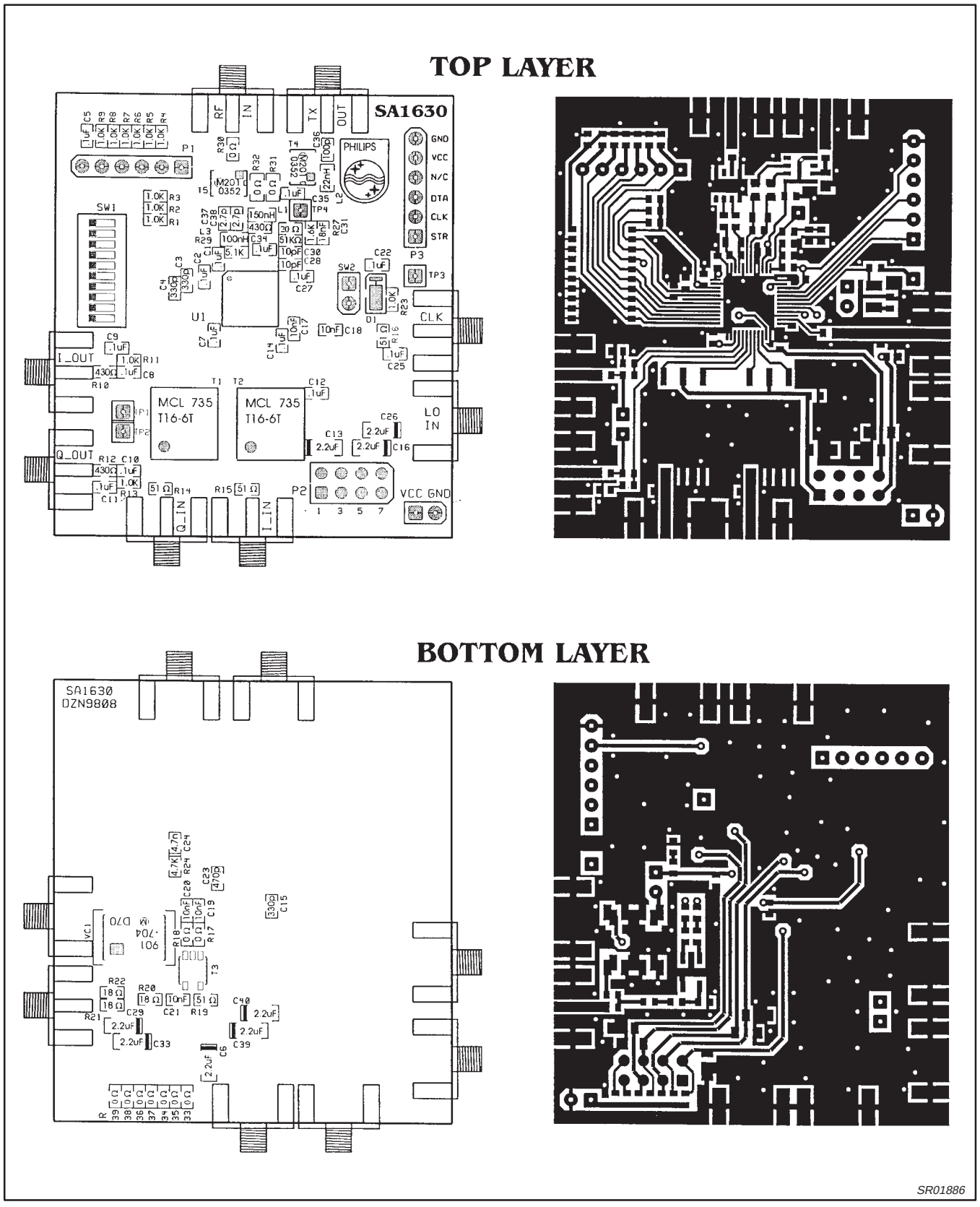

Figure 27. SA1630 application board

Table 3. Component list for SA1630 application board

Qty.	Part Value	Part Reference	Part Description	Vendor Part Number	Manufacturer Part Number
Surface mount capacitors					
2	2.7 pF	C37, C38	NPO Ceramic 0603 ±0.25pF, 50V	Garrett CE2R7C1NO	MMC
2	10 pF	C28, C30	NPO Ceramic 0603 ±0.5pF, 50V	Garrett CE100D1NO	MMC
1	100 pF	C36	NPO Ceramic 0603 ±5%, 50V	Garrett CE101J1NO	MMC
3	330 pF	C3, C4, C15	X7R Ceramic 0603 ±10%, 50V	Garrett CE331K1NR	MMC
1	470 pF	C23	X7R Ceramic 0603 ±10%, 50V	Garrett CE471K1NR	MMC
1	4.7 nF	C24	X7R Ceramic 0603 ±10%, 50V	Garrett CE472K1NR	MMC
5	10 nF	C17, C18, C19, C20, C21	X7R Ceramic 0603 ±10%, 50V	Garrett CE103K1NR	MMC
1	18 nF	C31	X7R Ceramic 0603 ±10%, 25V	Garrett MCH182C183KK	Rohm Electronics
15	0.1 µF	C1, C2, C5, C7, C8, C9, C10, C11, C12, C14, C22, C25, C27, C32, C34, C35	Z5U Ceramic 0603 ±20%, 25V	Garrett CC104M1NU	MMC
8	2.2 µF	C6, C13, C16, C26, C29, C33, C39, C40	Tant Chip Cap 10V A 3216 ±10%	Garrett 267M1002225K-533	Matsuo Electronics
Surface mount resistors					
12	0	R17, R18, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39	Chip Res 0603 1/16W ±5%	Garrett MCR10JW000	Rohm Electronics
3	18	R20, R21, R22	Chip Res 0603 1/16W ±5%	Garrett MCR10JW180	Rohm Electronics
1	20	R26	Chip Res 0603 1/16W ±5%	Garrett MCR10JW200	Rohm Electronics
4	51	R14, R15, R16, R19	Chip Res 0603 1/16W ±5%	Garrett MCR10JW510	Rohm Electronics
3	430	R10, R12, R28	Chip Res 0603 1/16W ±5%	Garrett MCR10JW431	Rohm Electronics
12	1 K	R1, R2, R3, R4, R5, R6, R7, R8, R9, R11, R13, R23	Chip Res 0603 1/16W ±5%	Garrett MCR10JW102	Rohm Electronics
1	1.6 K	R27	Chip Res 0603 1/16W ±5%	Garrett MCR10JW162	Rohm Electronics
1	4.7 K	R24	Chip Res 0603 1/16W ±5%	Garrett MCR10JW472	Rohm Electronics
1	5.1 K	R29	Chip Res 0603 1/16W ±5%	Garrett MCR10JW512	Rohm Electronics
1	51 K	R25	Chip Res 0603 1/16W ±5%	Garrett MCR10JW513	Rohm Electronics
Inductors					
1	22 nH	L2	Chip Inductor 1008 ±10%	Coilcraft 1008CS–220 ±10%	Coilcraft 1008CS–220 ±10%
1	100 nH	L3	Chip Inductor 1008 ±10%	Coilcraft 1008CS–101 ±10%	Coilcraft 1008CS–101 ±10%
1	150 nH	L1	Chip Inductor 1008 ±10%	Coilcraft 1008CS–151 ±10%	Coilcraft 1008CS–151 ±10%
Transformer					
2	16:1	T1, T2	RF transformer – Ratio: 16:1	Mini-Circuits T16-6T-KK81	Mini-Circuits T16-6T-KK81
1	4:1	T3	RF transformer – Ratio: 4:1	Mini-Circuits TC4-14	Mini-Circuits TC4-14
2	LBD30	T4, T5	Balun	Murata LDB30 (50-209)	Murata LDB30 (50-209)
Integrated circuit					
1	SA1630	U1	IF quadrature transceiver	SA1630BE	Philips SA1630
Miscellaneous					
1	704 MHz	VC1	704 MHz VCO	Murata 901-704 D70	Murata 901-704 D70
8			SMA edge connector	Digikey J502-ND	EF Johnson 142-0701-801
8		P1, P2, P3, TP1, TP2, TP3, TP4, SW2	Single row straight header	Digikey S1011-36-ND	Sullins
1		D1	SMT LED, red	Digikey P500CT-ND	Panasonic: LN1251C-TR
1		SW1	SMT switch, 10 pos.	Digikey CKN3062-ND	C 7K: SD10H0SK

SA1630 IF transceiver demonstration board AN2003

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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