APPLICATION NOTE

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An FM/IF system for DECT and other high speed GFSK applications

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An FM/IF system for DECT and other high speed GFSK applications: SA639

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ABSTRACT

A Philips low voltage high performance monolithic FM/IF system, the SA639 is introduced to meet the increasing demand for high speed digital wireless PCS applications. In order to assist the system design, a SA639-based performance evaluation board has been developed according to the Digital European Cordless Telephone (DECT) specifications. This application note presents a detailed description of the SA639 FM/IF system, the evaluation board, and design information including circuit diagram, component list, and the board layout. The experimental performance evaluation procedures, measured bit error rate (BER), sensitivity to frequency off-set, and sensitivity to FM deviation variation of this system are also presented. Results indicate that the low voltage SA639 FM/IF system provides superior performance for high speed digital wireless applications.

I. INTRODUCTION

To achieve the goal of wireless personal communications, allowing users access to the capabilities of the global communications network at any time without regard to location and mobility, cellular and cordless telephony have been taken as two major approaches. Cellular systems are evolving towards smaller cells (microcells) and lower power levels to provide higher overall capacity. Cordless telephones have evolved from home appliances towards wide spread “universal” low power personal communications systems. With the advent of digital cordless telephony, cordless systems with enhanced functionality have been developed that can support higher data rates and more sophisticated applications such as wireless private branch exchanges (WPBX) and public-access Telepoint systems. One of the first digital cordless standards is the Digital European Cordless Telecommunications (DECT) system, a pan-European standard designed to connect all of Europe with a common digital cordless system. DECT is also a flexible standard for providing a wide range of services in small cells.

In this application note, the SA639, a Philips low voltage FM/IF system with several important features such as post filter amplifier and active data switch, is proposed for DECT and other high speed digital wireless applications. A SA639-based DECT receiver evaluation board has been developed. Detailed description of the SA639 FM/IF system, structure of the evaluation board, design information, and experimental evaluation results are presented.

II. REVIEW OF DECT STANDARD

DECT is designed as a flexible interface to provide cost-effective communications services to high user densities in small cells. This standard is intended for the applications such as domestic cordless telephony, Telepoint, cordless PBXs, and Radio Local Loop (RLL). It supports multiple bearer channels for speech and data transmission (which can be set up and release during a call), hand over, location registration, and paging. Functionally, DECT is closer to a cellular system than to a classical cordless telephone. However, the interface to PSTN or ISDN remains the same as for a PBX or corded telephone. Table 1 is a summary of the key specifications of DECT and other digital cordless telephone systems.

DECT is based on Time Division Duplex (TDD) and Time Division Multiple Access (TDMA) with 10 carriers in the 1880 - 1900MHz band. Figure 1 illustrates the DECT TDD/TDMA frame structure. The completed frame is 10ms in duration with 24 time slots. The first 12 slots are allocated for the transmission from base station to handsets, and the other 12 slots are for the transmission from hand sets to base station. Each slot is 417μs long with 480 bits. The first 32 bits is a “1010...” sequence for synchronization. The 32kb/s ADPCM CODEC is used for speech coding in DECT, which provides 320 bits during each 10ms frame. When a call is made, two slots (one is in the first 12 slots, the other is in the last 12 slots) are assigned to the user for transmit and receive.

Gaussian filtered FSK (GFSK) modulation scheme is employed in DECT. GFSK is a premodulation Gaussian filtered digital FM scheme. Figure 2 shows the block diagram of a GFSK modulator. The advantages of GFSK can be summarized as follows.

i) Constant envelope nature: this allows GFSK modulated signal to be operated with class-C power amplifier without introducing spectrum regeneration. Therefore, lower power consumption and higher power efficiency can be achieved.

ii) Narrow power spectrum: narrow mainlobe and low spectral tails keep the adjacent channel interference to low levels and achieve higher spectral efficiency.

iii) Non-coherent detection: GFSK modulated signal can be demodulated by the limiter/discriminator receiver as shown in Figure 3. This simple structure leads to low cost GFSK receivers.

III. THE SA639 FM/IF SYSTEM

The SA639 is a low-voltage high performance monolithic FM/IF system with high speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, fast RSSI op amps, post detection filter amplifier, and a data switch. The block diagram of SA639 is presented in Figure 4. The SA639 was designed specially for high data rate portable communications applications and will function down to 2.7V. The data output provides a minimum bandwidth of 1MHz to demodulate high speed data, such as in DECT applications. Figure 5 presents the quad tank S-curve of SA639, which indicates the linear range to be about 2MHz. The measured RSSI characteristics of SA639 is presented in Figure 6. With more than 75dB dynamic range, the SA639 RSSI rise/fall time is 0.8/2.0ms at -45dBm RF level.

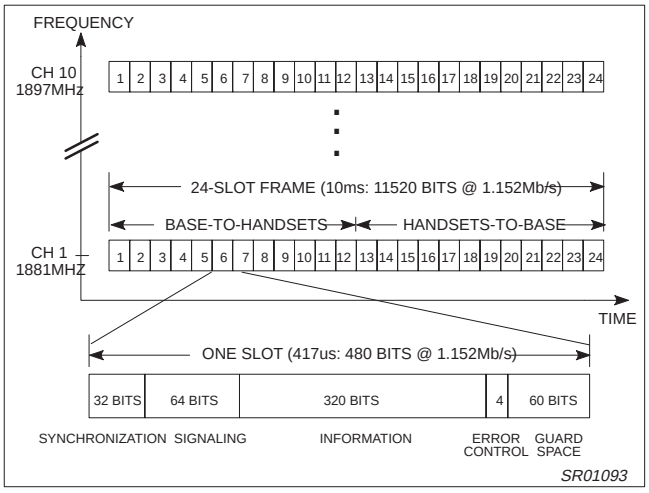

Figure 1. DECT TDD/TDMA Frame Structure

An FM/IF system for DECT and other high speed GFSK applications: SA639

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Table 1. Summary of Digital Cordless Standards

Standard	CT2/CT2+	DECT	PHS	PACS
Region	Europe/Canada	Europe	Japan	USA
Frequency Band (MHz)	CT2: 864–868 CT2+: 944–948	1880–1900	1895–1918	Tx: 1850-1910 Rx: 1930-1990
Duplex	TDD	TDD	TDD	FDD
Multiple Access	TDMA	TDMA	TDMA	TDMA
Number of Channels	40	10	77	16 pairs
Channel Spacing (kHz)	100	1728	300	300
Users/Channel	1	12	4	8/pair
Modulation	GFSK (FM dev. 14-25kHz)	GFSK (FM dev. 288kHz)	π/4-DQPSK	π/4-DQPSK
Bit Rate	72kb/s	1.152Mb/s	384kb/s	384kb/s
Speech Coding	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM
Frame Duration	2ms	10ms	5ms	2.5ms
Peak Power	10mW	250mW	80mW	200mW

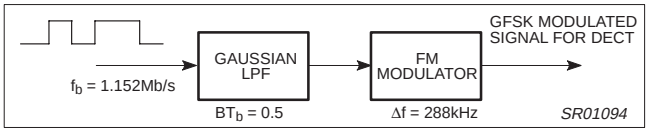

Figure 2. Block Diagram of GFSK Modulator

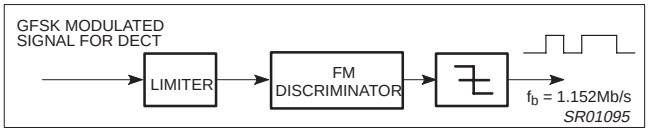

Figure 3. Block Diagram of GFSK Demodulator

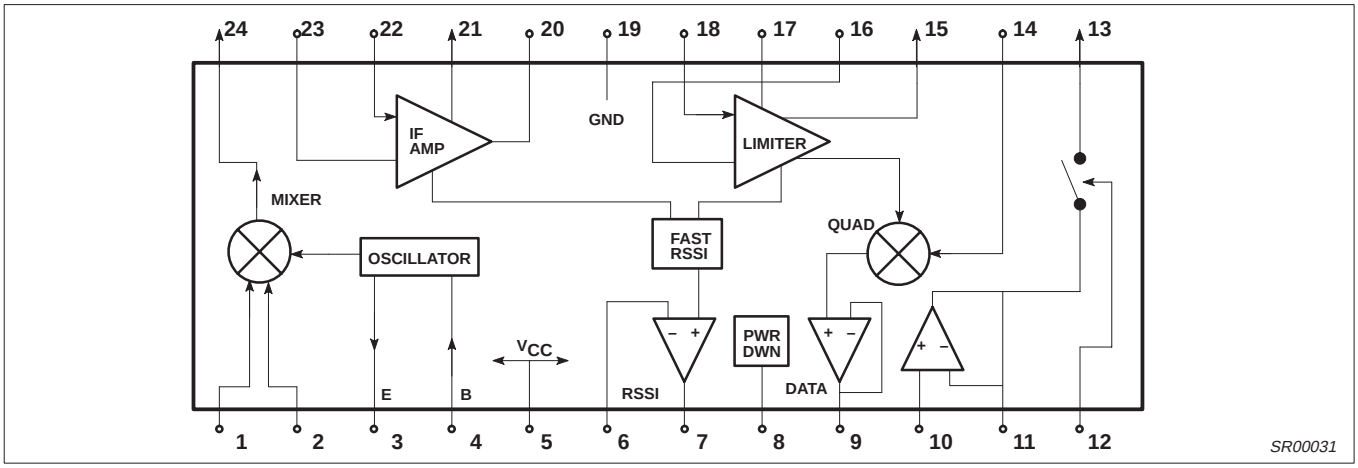

Figure 4. Block Diagram of the SA639 FM/IF System

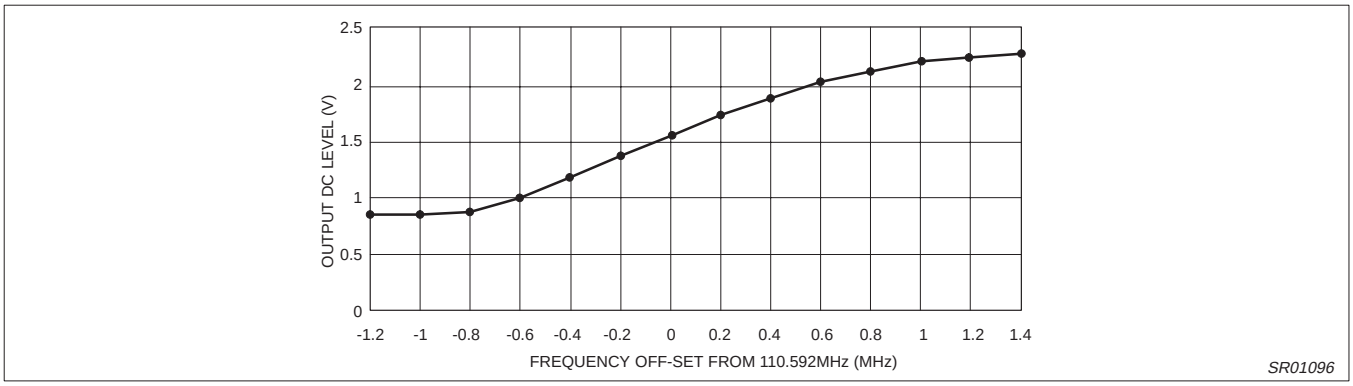

Figure 5. Quad Tank S-Curve of SA639 Board

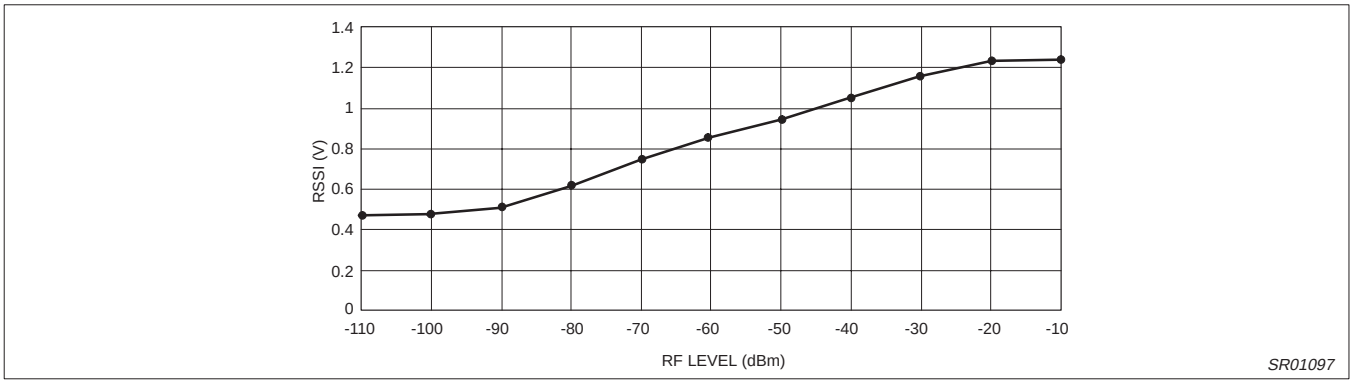

Figure 6. Measured RSSI Characteristics of SA639

The post-detection amplifier may be used to realize a group delay optimized low pass filter. The filter amplifier provides 0dB gain and has a 3dB bandwidth of at least 4MHz in order to keep its frequency response influence on the filter group delay characteristics at a minimum. It can be configured for Sallen & Key low pass with Bessel characteristic and a 3dB cut frequency of about 800kHz.

The SA639 incorporates an active data switch to derive the data comparator reference voltage by means of routing a portion of data signal to an external integration circuit. The data switch is typically closed for 10ms in the course of 32 bit synchronization sequence, and is open otherwise. The time constant of the external integration circuit is about 5 to 10ms. This active switch provides excellent tracking behavior over a DC input range of 1.2 - 2.0V. The slew rate is better than 1V/ms. When the switch is opened, the output is in a tri-state mode with a leakage current of less than 100nA. This reduces the discharge of the external integration circuit. As compared to other similar FM/IF chips, another advantage of SA639 is that during power down mode (between data bursts) the data switch will output a reference of about 1.6V to maintain a charge on the external RC circuit. This idea helps extract the reference voltage for the external capacitor in a shorter time and improves the accuracy of the voltage on the capacitor. The overall system is well suited for battery operated high quality products in digital wireless personal communications. Detailed specifications of SA639 can be found in [3].

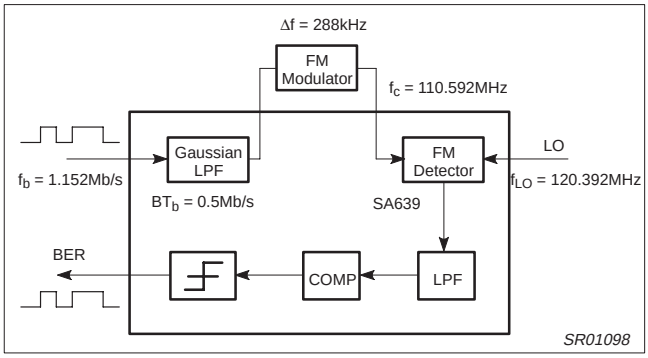

Figure 7. Structure of the SA639 GFSK Evaluation Board

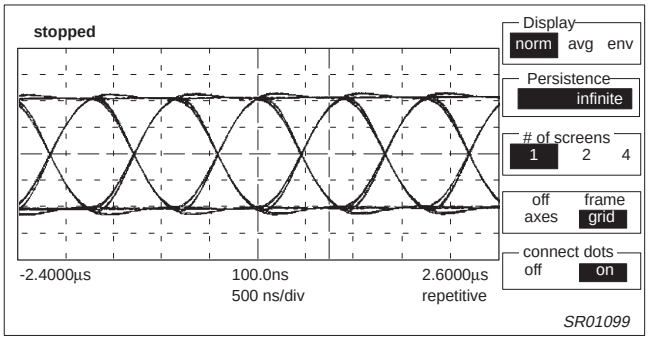

Figure 8. Measured Eye-Diagram at the Output of Tx Gaussian LPF

IV. STRUCTURE OF THE SA639 EVALUATION BOARD

A SA639-based evaluation board has been developed based on DECT specifications. The structure of this board is illustrated in Figure 7 together with a VCO/FM discriminator based GFSK modem (modulator/demodulator). The demo board contains the entire demodulator as well as the Gaussian low-pass filter (LPF) for the modulator. The DECT modulated signal, therefore, can be generated either by a standard DECT signal generator, or by sending a 1.152Mb/s data stream to the on-board Gaussian LPF (BTb = 0.5), then applying the filtered base band wave form to a FM signal generator with a modulation index of 0.5. The output is then the GFSK modulated signal (DECT). The schematic of the Gaussian LPF can be found in Figure 14. Baseband eye-diagram at the output of the Gaussian LPF is presented in Figure 8.

At the output of the limit/frequency discriminator, the post-detection amplifier is configured as a Sallen & Key LPF to eliminate noise. For the convenience of operation, the evaluation board is designed in such a way that the reference voltage for the data comparator can be obtained either from the switch controlled DC extraction circuit, or directly from the power supply. If the DECT Burst Mode Control circuit is available, the active data switch can be used to extract and track DC level during the synchronization sequence. Otherwise the DC reference can be obtained from the power supply and manually adjusted for the comparator operation.

A 2-level threshold detector with sampling time adjustment circuit is implemented on the board for data regeneration. The phase of data clock can be adjusted manually through a monostable multivibrator (74HC123) to achieve the optimal sampling time. The demo board is initially adjusted for a bit rate of 1.152Mb/s. If a different data rate

is used, the sampling time has to be re-adjusted. The output of the threshold detector is the regenerated binary data, which can be sent to a data error analyzer to evaluate the BER performance.

The symbol timing recovery (STR) circuit is not implemented on this evaluation board. Transmit data clock either hard-wire connected from the transmitter or from a separate STR circuit is required for the operation. The performance measurements presented in this application note were conducted with hard-wire connected data clock. However, BER degradation caused by STR should not be more than 1dB [6].

This SA639-based GFSK demo board is designed with DECT specifications at RF frequency of 110.592MHz, LO frequency of 120.392MHz, and intermediate frequency of 9.8MHz. For different frequency plan applications, the step-by-step matching circuit design procedure can be found in [1]. Tables 2 and 3 present the SA639 RF/LO input impedance and Mixer/Limiter output impedance over frequency, respectively.

Table 2. SA639 RF/LO Input Impedance Over Freq.

Frequency	RF Input	LO Input
50MHz	846Ω // 4.52pF	6900Ω // 4.07pF
110MHz	687Ω // 3.84pF	4900Ω // 4.09pF
240MHz	510Ω // 3.69pF	1900Ω // 4.22pF
500MHz	190Ω // 4.21pF	245Ω // 4.98pF

Table 3. SA639 Mixer/Limiter Output Impedance Over Freq.

Frequency	RF Input	LO Input
0.5MHz	395Ω // 20.2pF	438Ω // 14.5pF
10MHz	350Ω // 6.67pF	383Ω // 3.5pF
21MHz	339Ω // 4.58pF	393Ω // 2.04pF
50MHz	326Ω // 3.44pF	391Ω // 1.35pF

V. PERFORMANCE EVALUATION

Performance of this SA639 based DECT GFSK system including BER and sensitivity to frequency off-set and FM deviation variation is experimentally evaluated. Measurement procedures and the measured results are presented in this section.

Figure 9 illustrates the measurement set-up with the SA639 DECT evaluation board. A data error analyzer is employed to generate a pseudo random binary sequence (PRBS) with length of 10^9-1 at a data rate of 1.152Mb/s. This data sequence is sent to a DECT signal generator to generate a standard DECT modulated signal at 110.592MHz. Another signal generator is employed to provide an LO signal at 120.392MHz for the FM/IF system detection. The reference DC voltage for the data comparator is obtained from power supply for this evaluation. Data clock signal is directly from the data error analyzer. The sampling time is manually adjusted at the center of baseband eye diagram. Recovered data sequence is fed back to the Data Error Analyzer for BER measurement.

The BER measurement procedures can be summarized as follows.

- Build the measurement set-up as shown in Figure 9.
- Measure SINAD at the data output of SA639: RF = 110.592MHz, fm = 1kHz, Df = 288kHz; LO = 120.392MHz, -10dBm; the typical sensitivity for 12dB SINAD should be about -97dBm.
- Check SA639 output level: tune the quad tank circuit to have the least distorted eye-diagrams at the post-op. amp. output. The DC level should be about 1.4 - 1.7v.
- Check the DC reference for the comparator: set the reference voltage at the DC level of the op. amp. output by adjusting VR1 in Figure 14.
- Adjust sampling position: set the up edge of the clock at pin 11 of 74HC74 to be at the center of the eye-diagram at pin 2 of LM311B by adjusting VR2 in Figure 14.
- Measure BER with high RF level: set RF input signal level at -60 dBm; LO signal level at -10 dBm: error free.
- Measure BER vs. RF input level curve: RF level: -76 ~ -86 dBm, LO level: -10 dBm, at each point, at least 100 errors have to be measured.

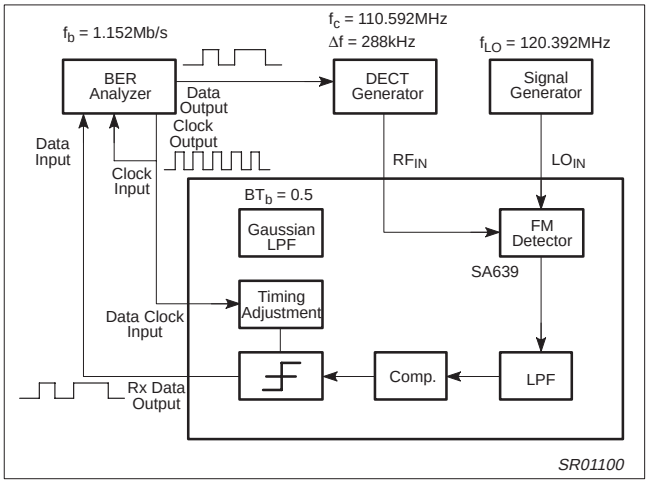

Figure 9. Block Diagram of the BER Evaluation Set-up

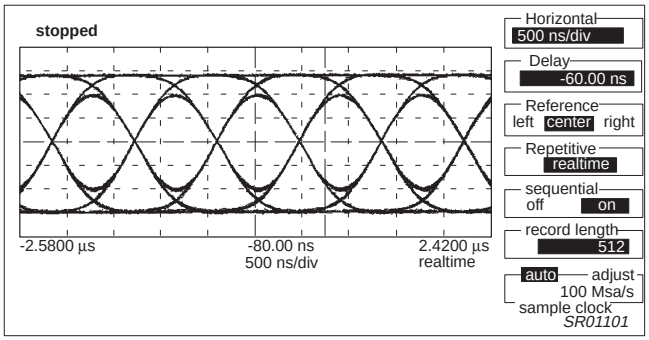

Figure 10. Recovered Eye-Diagram at the Output of SA639

The recovered baseband eye-diagram is shown in Figure 10, and the measured BER vs. RF input level is presented in Figure 11. It can be seen that about -83dBm RF power is needed to achieve the bit error rate of 10^{-3}. Since a typical front-end circuit has a better noise figure than FM/IF system, it is common to achieve more than 5dB signal-to-noise ratio gain by the front-end circuit. Therefore, with the SA639 FM/IF the overall system sensitivity could be better than -88dBm for the BER of 10^{-3}. Based on our measurements, by applying the Philips UAA2077AM 2GHz image rejecting front-end to the SA639 FM/IF system the overall system sensitivity is -91dBm for the BER of 10^{-3}. This performance compares very well to the DECT specifications for public access equipment (-86dBm for 10^{-3} BER).

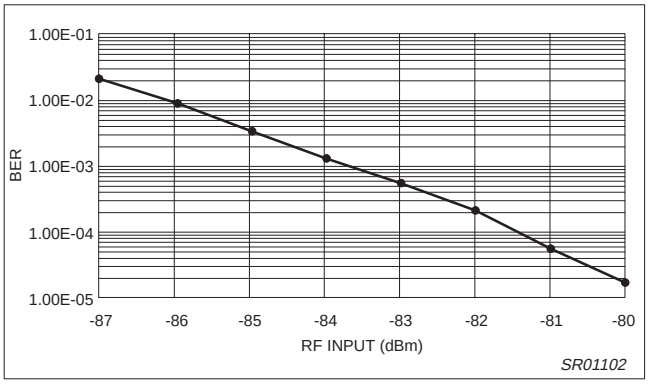

Figure 11. BER of the SA639 DECT Demoboard (RF: 110.592 MHz; LO: 120.392 MHz; fb: 1.152 Mb/s)

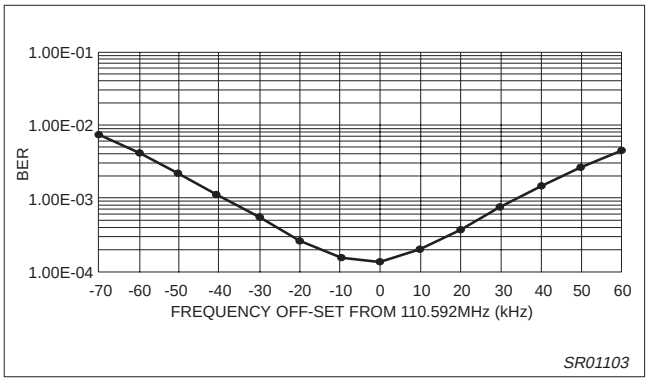

Figure 12. BER Degradation Caused by Frequency Off-Set (RF: -82dBm)

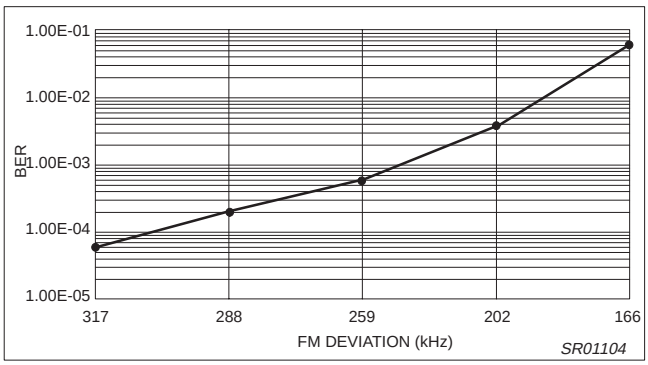

Figure 13. BER vs. FM Deviation (RF: 110.592 MHz, -82 dBm; fb: 1.152 Mb/s)

The performance degradation caused by frequency off-set and the sensitivity to FM deviation variation of this system are also evaluated. Figure 12 presents the measured BER vs. frequency off-set. Even with 50 kHz off-set, only minor degradation can be observed, and -82dBm RF level is enough for 10^{-3} BER. The sensitivity of this system to FM deviation variation is illustrated in Figure 13. Even with 10% deviation reduction (259kHz), less than -82dBm RF signal is needed to achieve the BER of 10^{-3}. These results indicate that the Philips SA639 FM/IF system provides superior performance for DECT and other high data rate GFSK applications.

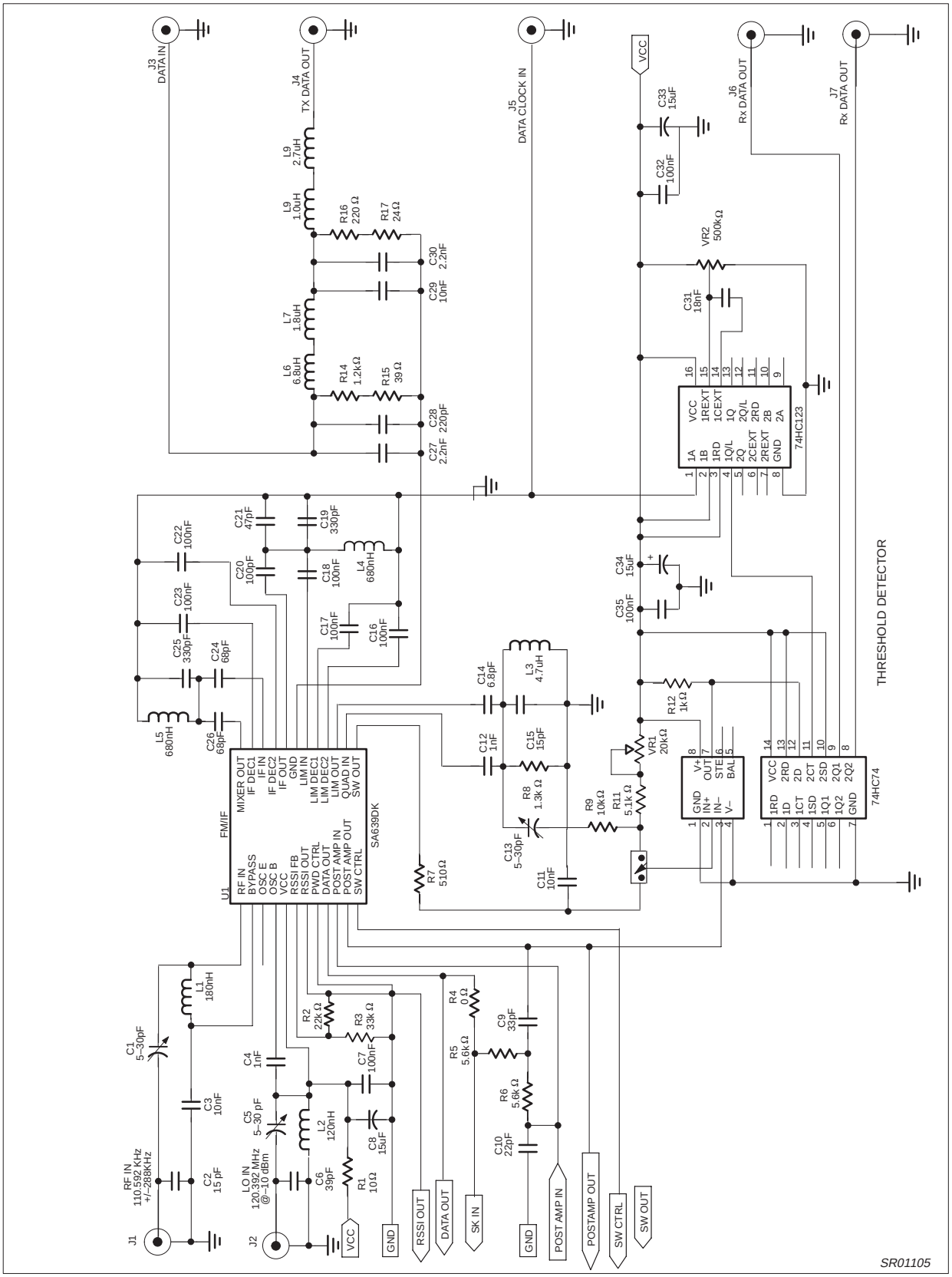

Figure 14. Schematic

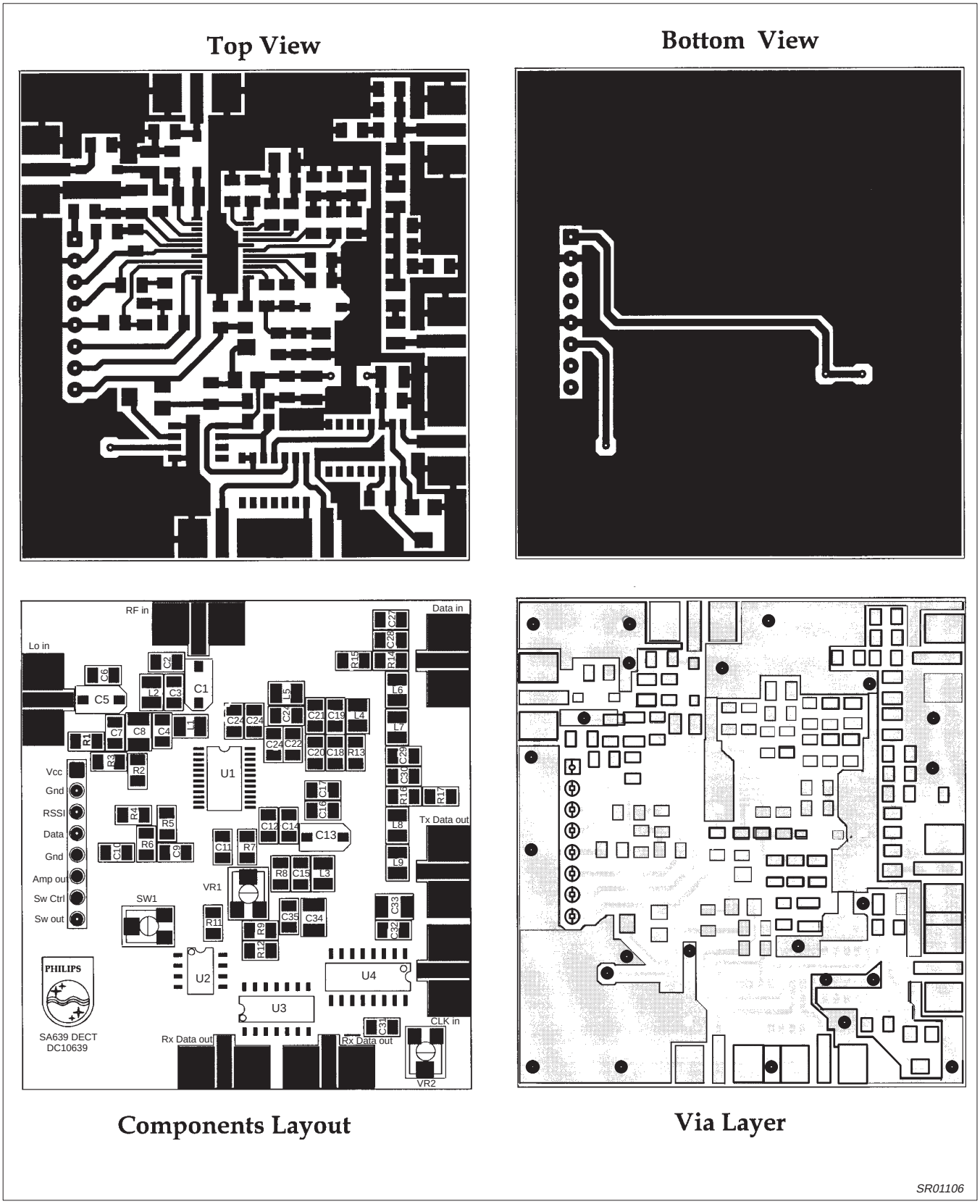

Figure 15. Board Layout

VI. CONCLUSIONS

A Philips low voltage high performance FM/IF system (SA639) based GFSK modem evaluation board is presented. Experimental performance evaluation including bit error rate (BER), sensitivity to frequency off-set, and sensitivity to FM deviation variation of this system has been conducted based on DECT specifications. Results indicate that a superior performance can be achieved with the Philips FM/IF systems for high speed digital wireless applications.

Table 4. Customer Application Component List for GMSK/GFSK Demoboard

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	6.8pF	50V	C14	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG689C9BB2
1	15pF	50V	C2, C15	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG150J9BB2
1	18pF	50V	C31	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG180J9BB2
1	22pF	50V	C10	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG220J9BB2
1	33pF	50V	C9	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG330J9BB2
1	39pF	50V	C6	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG390J9BB2
1	47pF	50V	C21	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG470J9BB2
2	68pF	50V	C24, C26	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG680J9BB2
2	100pF	50V	C18, C20	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG101J9BB2
1	220pF	50V	C28	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG221J9BB2
1	330pF	50V	C19, C25	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG331J9BB2
3	1000pF	50V	C4, C12	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG102J9BB2
2	2200pF	50V	C27, C30	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG222J9BB2
3	0.01µF	50V	C3, C11, C29	Cer Cap 1206 X7R ±10%	Garrett	Philips	12062R103K9BB2
7	0.1µF	50V	C7, C16, C17, C22, C23, C32, C35	Cer Cap 1206 X7R ±10%	Garrett	Philips	12062R104K9BB2
3	15µF	10V	C8, C33, C34	Tantalum Capacitor Chips	Garrett	Philips	49MC106C006KOAS
Surface Mount Variable Capacitors							
3	5-30pF		C1, C5, C13	Trimmer capacitor	Kent Elect	Kyocera	CTZ3S-30C-W1
Surface Mount Resistors							
1	0Ω	50V	R4	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW000E
1	10Ω	50V	R1	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW100E
1	24Ω	50V	R17	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW240E
1	39Ω	50V	R15	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW390
1	220Ω	50V	R16	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW221E
1	510Ω	50V	R7	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW511E
1	560Ω	50V	R13	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW561E
1	1kΩ	50V	R12	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW102E
1	1.2kΩ	50V	R14	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW122E
1	1.3kΩ	50V	R8	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW132E
1	5.1kΩ	50V	R11	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW512E
2	5.6kΩ	50V	R5, R6	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW562E
1	10kΩ	50V	R9	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW223E
1	22kΩ	50V	R2	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW223E
3	33kΩ	50V	R3	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW333E
Surface Mount Variable Resistors							
1	20kΩ	50V	VR1	Trimmer Resistor .25W ±20%	Garrett	Philips	ST-4TA203
1	500kΩ	50V	VR2	Trimmer Resistor .25W ±20%	Garrett	Philips	ST-4TA504
Surface Mount Switch							
1	SPDT		SW1	4mm Selector Switch	Garrett	Philips	CS-412YTA
Surface Mount Inductors							
1	120nH		L2	Chip Inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-331XKBB
1	180nH		L1	Chip Inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-331XKBB
2	680nH		L4, L5	Chip Inductor 1008 ±10%	Digikey	TOKO	380NB-R68M
1	1.8µH		L7	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-1R8K
1	2.7µH		L9	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-2R7K
1	4.7µH		L3	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-4R7K
1	6.8µH		L6	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-6R8K
1	10µH		L8	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-100K

Table 4. Continued

Surface Mount Integrated Circuits							
1		5V	U1	FM IF with filter switch	Philips	Philips	SA639
1		5V	U2	Voltage comparator	Philips	Philips	LM311B
1		5V	U3	Dual D-type flip-flop	Philips	Philips	74HC74
1		5V	U4	Dual re-triggerable multivibrator	Philips	Philips	74HC123
Miscellaneous							
7			J1, J2, J3, J4, J5, J6, J7	SMA gold connector	Newark	EF Johnson	142-0701-801
1			JP1	8-pins header straight	Mouser	Molex	538-22-03-2081
1				Printed circuit board	Excel	Philips	DC10639
78 Total Parts							

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