APPLICATION NOTE

ABSTRACT
The SA8026 is a low voltage, low phase noise, fractional-N frequency synthesizer. It is targeted for wireless systems where good phase noise performance and fast switching time is crucial.

AN1893

SA8026/7026/8016/7016 Low voltage Fractional-N dual frequency synthesizers

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SA8026/7026/8016/7016
Low voltage fractional-N dual frequency synthesizer

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SA8026/7026/8016/7016 Low voltage fractional-N dual frequency synthesizer

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1. INTRODUCTION TO THE SA8026

1.1. Description

The SA8026 is a low voltage, low phase noise, TSSOP packaged, fractional-N frequency synthesizer. It is targeted for wireless systems where good phase noise performance and fast switching time is crucial. Designed in the QUBiC2 BiCMOS process, the main synthesizer operates at VCO input frequency up to 2.5 GHz. The auxiliary synthesizer can operate up to 550 MHz, and the phase detector up to 4 MHz. The design is based on the previous SA8025 family. There is also a 1 GHz version, SA7026, which operates up to 1.3 GHz. The SA8026 and SA7026 also have single derivatives, the SA8016 and SA7016, respectively, where there are no auxiliary synthesizers.

1.2. Features

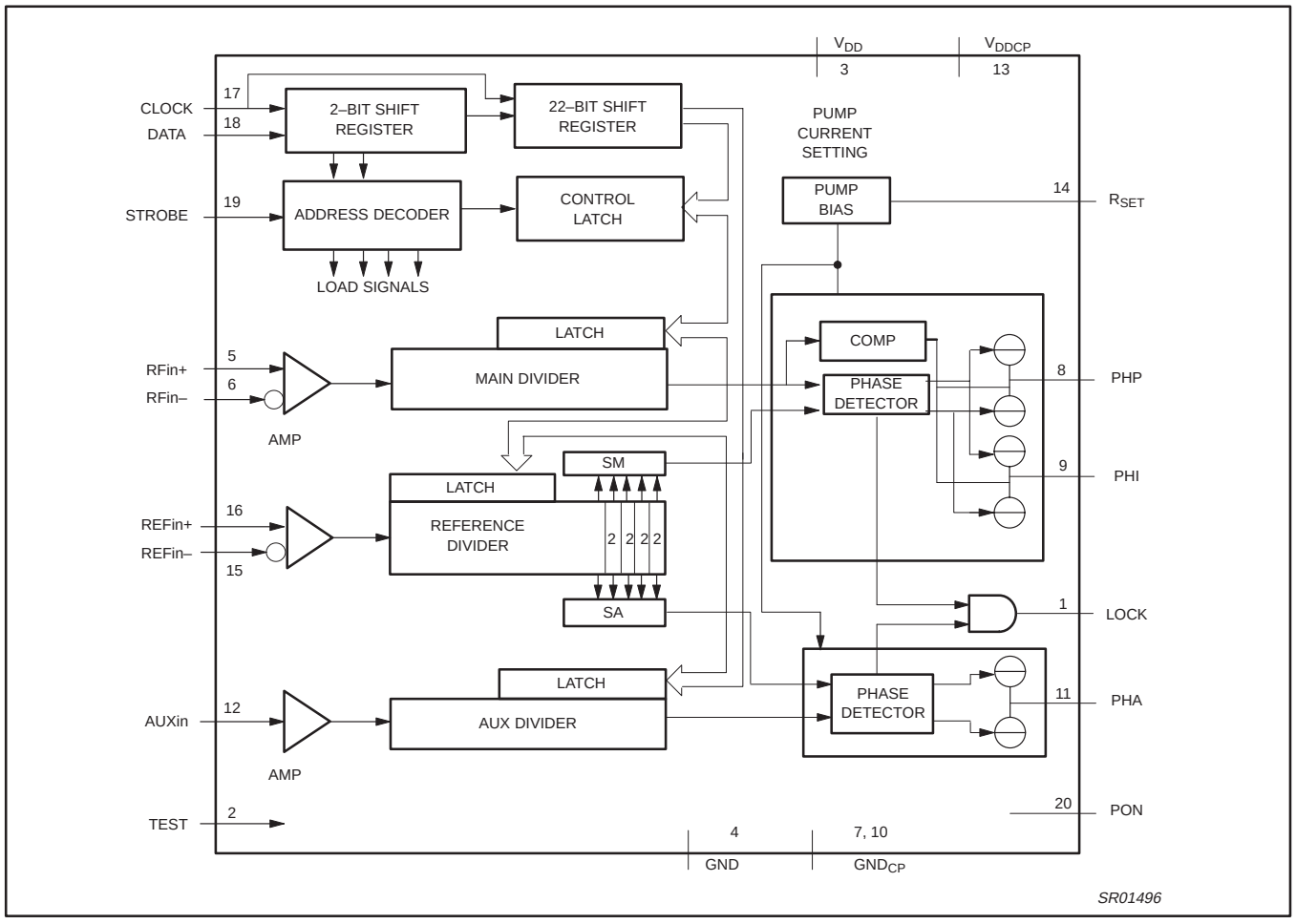


Figure 1. SA8026 block diagram

Table 1. SA8026 features

Typical performance:	
RF	
Main frequency range	2.5 GHz (max.)
Auxiliary frequency range	550 MHz (max.)
Reference frequency range	40 MHz (max.)
Phase comparison frequency	4 MHz (max.)
RF input sensitivity	–18 dBm (min.)
DC	
Supply voltage	2.7 V – 5.5 V
I_{CC} powered up	10 mA typical @ +3 V
I_{CC} powered down	1 μA @ +3 V
Features	
Low noise performance	
Fully programmable via 10 Mb/s 3-wire serial interface	
Hardware or software power-downs	
Package	TSSOP-20
Applications	
2 GHz PCS mobile telephones	
Portable battery-powered equipment	

2. FUNCTIONAL DESCRIPTION OF SA8026

2.1. Phase detector and charge pumps

The phase detector drives the two charge pumps, PHP and PHI. The output charge pump currents are set via software per Table 2.

Table 2. Charge pump current setting for the SA8026

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}	I_{PHI}
0	0	$1.5 \times I_{SET}$	$3 \times I_{SET}$	$15 \times I_{SET}$	$36 \times I_{SET}$
0	1	$0.5 \times I_{SET}$	$1 \times I_{SET}$	$5 \times I_{SET}$	$12 \times I_{SET}$
1	0	$1.5 \times I_{SET}$	$3 \times I_{SET}$	$15 \times I_{SET}$	0
1	1	$0.5 \times I_{SET}$	$1 \times I_{SET}$	$5 \times I_{SET}$	0

The reference current I_{SET} is set by an external resistor R_{SET} at Pin 14. R_{SET} should be between 6 kΩ and 15 kΩ, giving an I_{SET} of approximately 208 μA and 83 μA, respectively.

$$I_{SET} = \frac{V_{SET}}{R_{SET}}$$

where V_{SET} is a regulated 1.25 V reference voltage.

There are three ways to connect the charge pump outputs to the loop filter:

- Connect only PHP to the loop filter
- Tie PHP and PHI together for higher charge pump output and connect to the loop filter
- Use the adaptive mode.

2.1.1. Speedup mode

As seen in the block diagram (Figure 1), there are two independent charge pumps, PHP and PHI. The charge pumps will enter the speedup mode at the rising edge of the strobe after the last bit of WORD A is sent. The charge pumps will get out of speedup mode when the strobe goes back low. Speedup mode can also be activated via software by programming the T_{spu} bit in Word E.

If CP = 00, the output current of PHP = 15 × I_{SET}, and PHI = 36 × I_{SET}

If CP = 01, the output current of PHP = 5 × I_{SET}, and PHI = 12 × I_{SET}

If CP = 10, the output current of PHP = 15 × I_{SET}, and PHI = 0

If CP = 11, the output current of PHP = 5 × I_{SET}, and PHI = 0

One drawback of the speedup mode is that there is a secondary glitch that occurs when the charge pumps go from speedup to normal mode. This switching causes a difference in final phase error due to different current gains which results in frequency instability or glitch in the frequency domain. It will, in effect, cause the switching time to be longer depending on the loop bandwidth. One way to combat this problem is to experiment with the strobe pulse width to optimize the duration that the charge pumps remain in speedup mode.

The following graphs show typical measurements of the sink and source currents of the charge pumps for different CP settings.

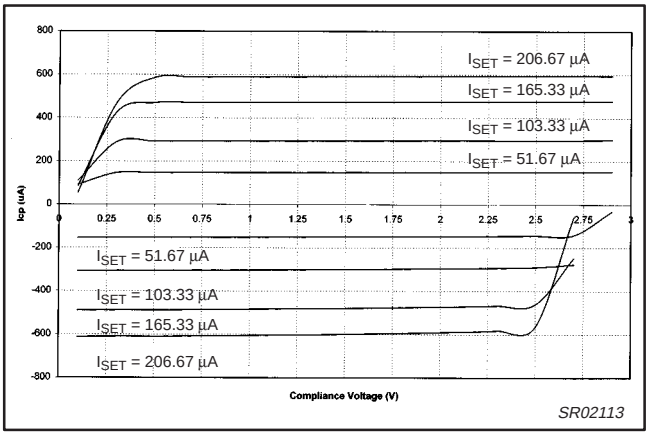


Figure 2. PHP charge pump vs. I_{SET} with CP=10; Temp=25°C

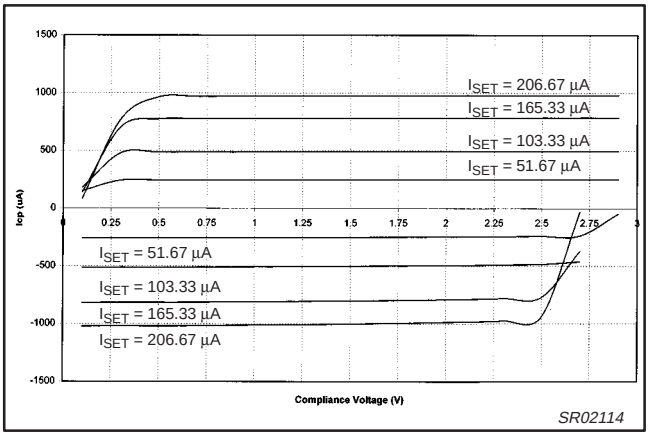


Figure 3. PHP charge pump vs. I_{SET} with CP=11; Temp=25°C

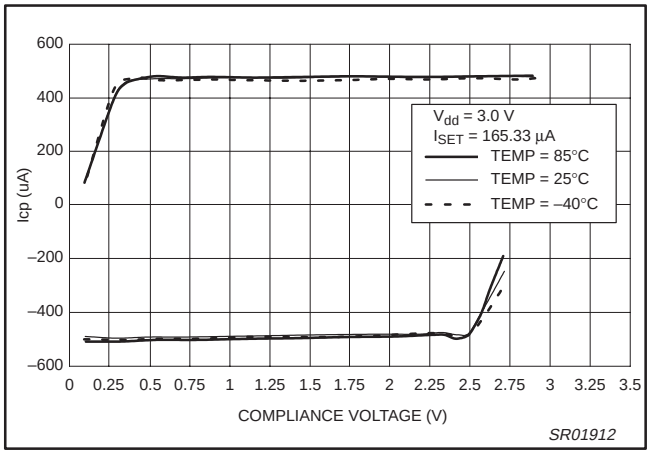


Figure 4. PHP charge pump vs. temperature with CP=10

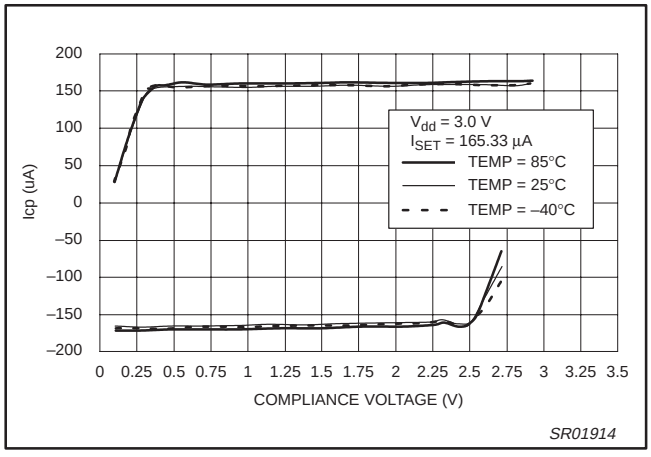


Figure 5. PHP charge pump vs. temperature with CP=11

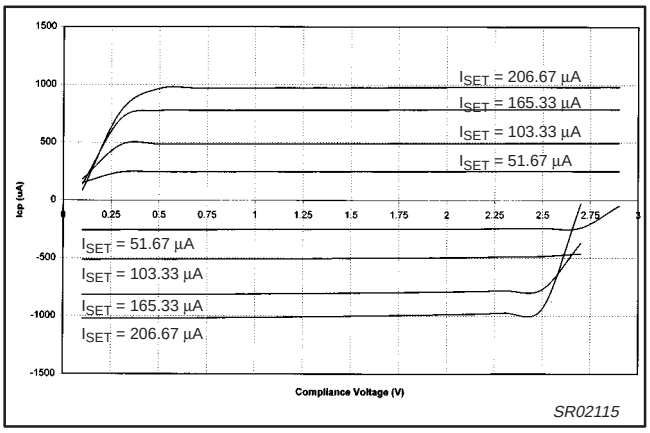


Figure 6. PHP-SU charge pump vs. I_{SET} with CP=01; Temp=25°C

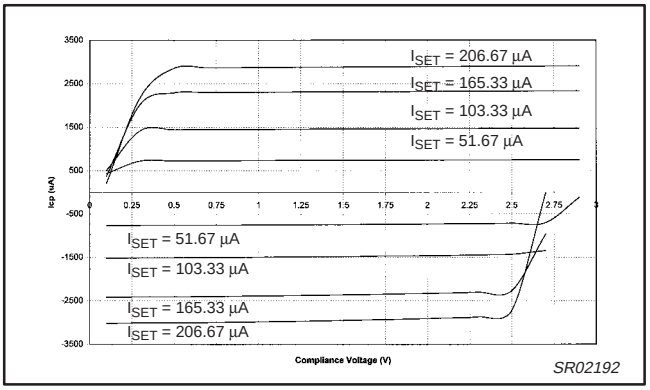


Figure 7. PHP-SU charge pump vs. temperature with CP=00; Temp=25°C

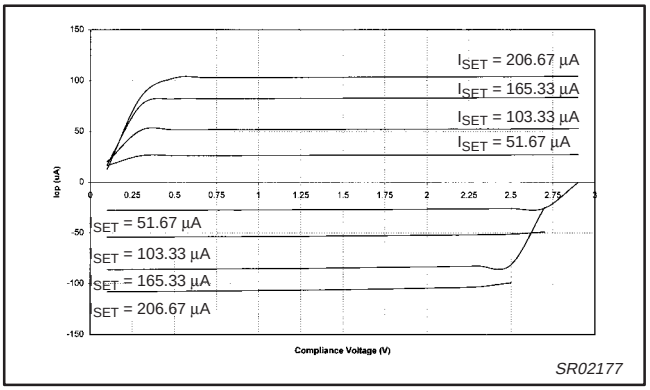


Figure 8. PHA charge pump vs. I_{SET} with CP=11; Temp=25°C

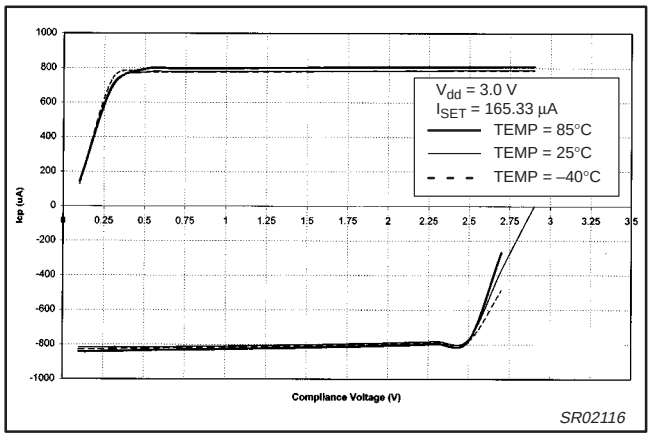


Figure 9. PHP-SU charge pump vs. temperature with CP=01

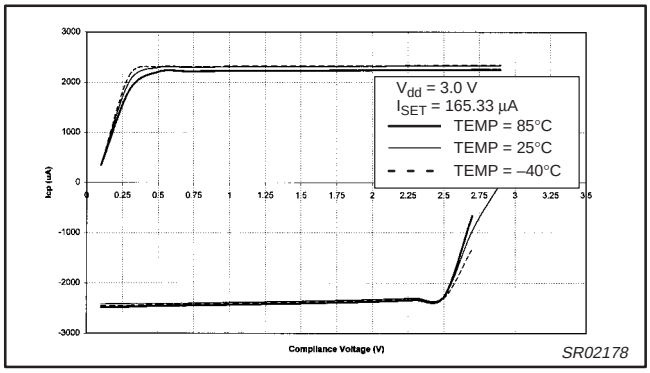


Figure 10. PHP-SU charge pump vs. I_{SET} with CP=00

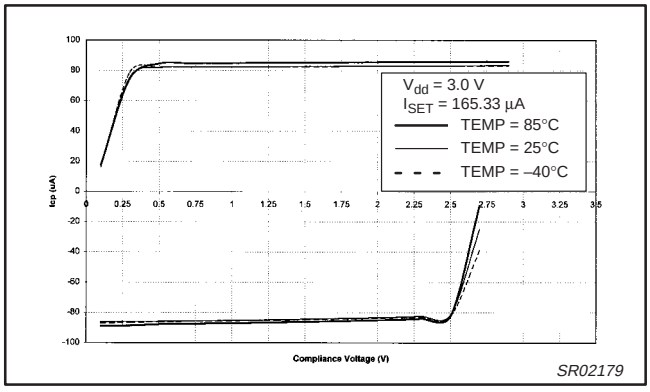


Figure 11. PHA charge pump vs. temperature with CP=11

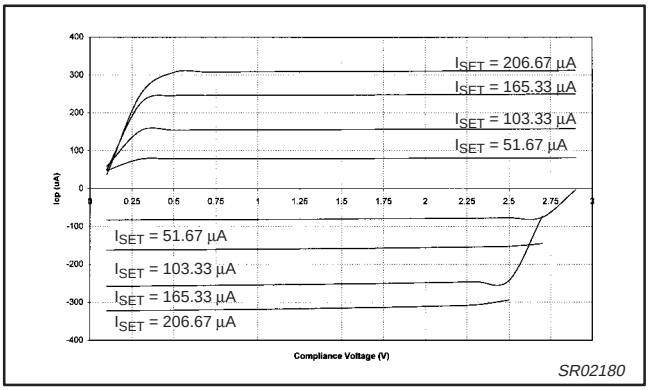


Figure 12. PHA charge pump vs. I_{SET} with CP=10; Temp=25°C

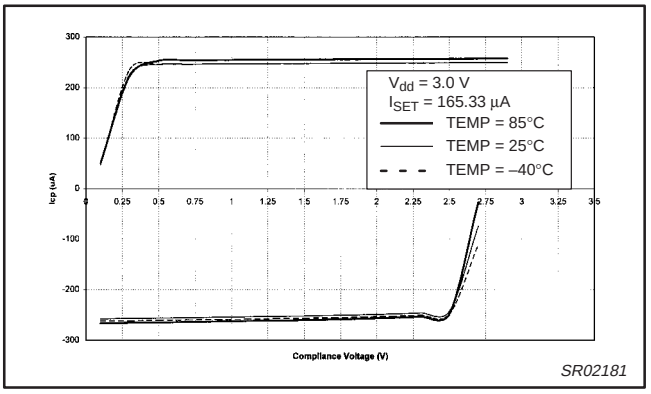


Figure 15. PHA charge pump vs. temperature with CP=10

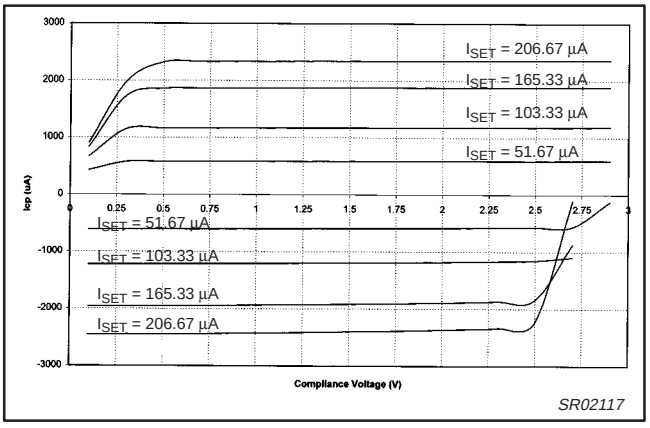


Figure 13. PHI charge pump vs. I_{SET} with CP=01; Temp=25°C

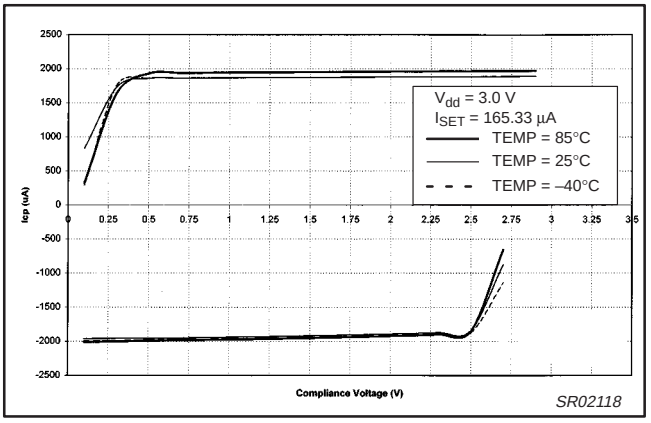


Figure 16. PHI charge pump vs. temperature with CP=01

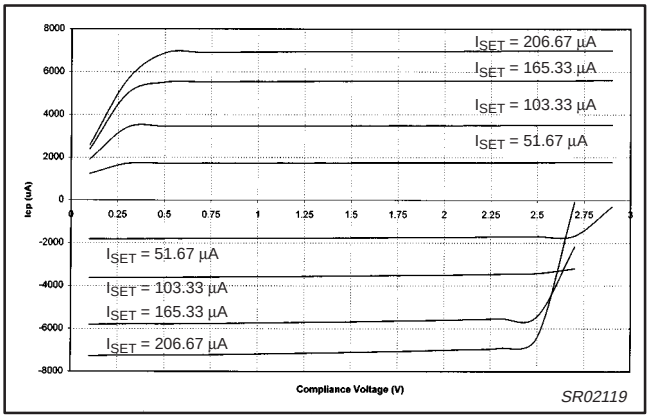


Figure 14. PHI charge pump vs. I_{SET} with CP=00; Temp=25°C

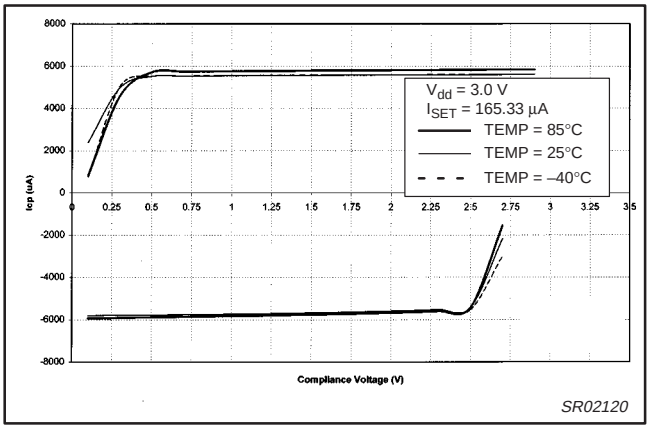


Figure 17. PHI charge pump vs. temperature with CP=00

2.1.2. Charge pump-phase detector characteristics

The following setup is used to obtain the phase detector gain curve.

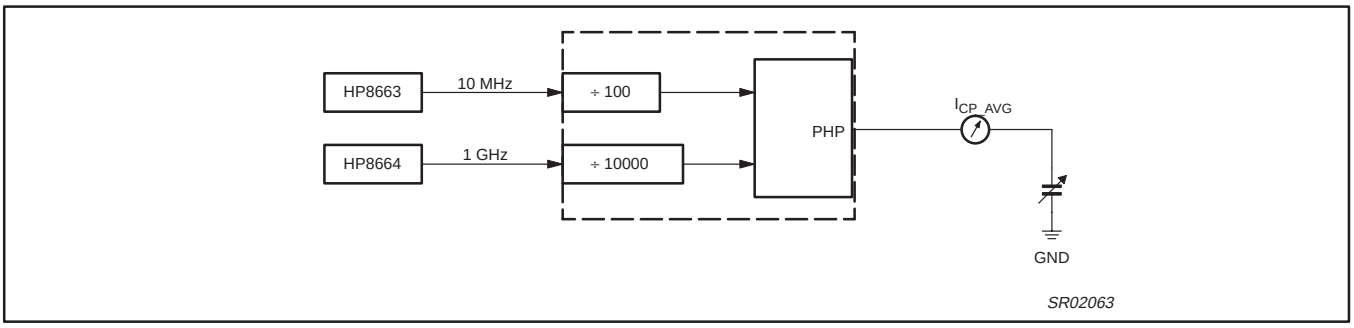


Figure 18. Phase detector gain measurement

The HP8663 supplies the reference input, and the HP8664 supplies the RF input. The two frequencies are divided down to obtain a comparison frequency of 100 kHz. The phase of the HP8664 is varied and I_{CP_AVG} is measured as a function of the phase error.

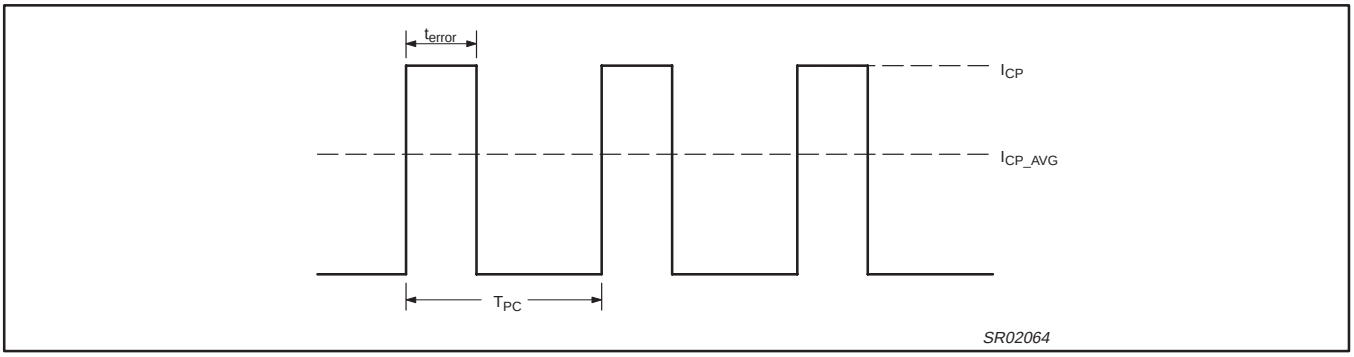


Figure 19.

$$I_{CP\_AVG} = \left(\frac{t_{error}}{T_{PC}}\right) \times I_{CP} \quad (1)$$

$$\text{Phase Detector Gain} = I_{CP\_AVG} \times \left(\frac{T_{PC}}{t_{error}}\right) \quad (2)$$

Phase error values are taken in the region of ±10 ns. The loop spends most of its time in this region when it is locked or near locked. Figures 21 and 23 show the source and sink gains of the phase detector.

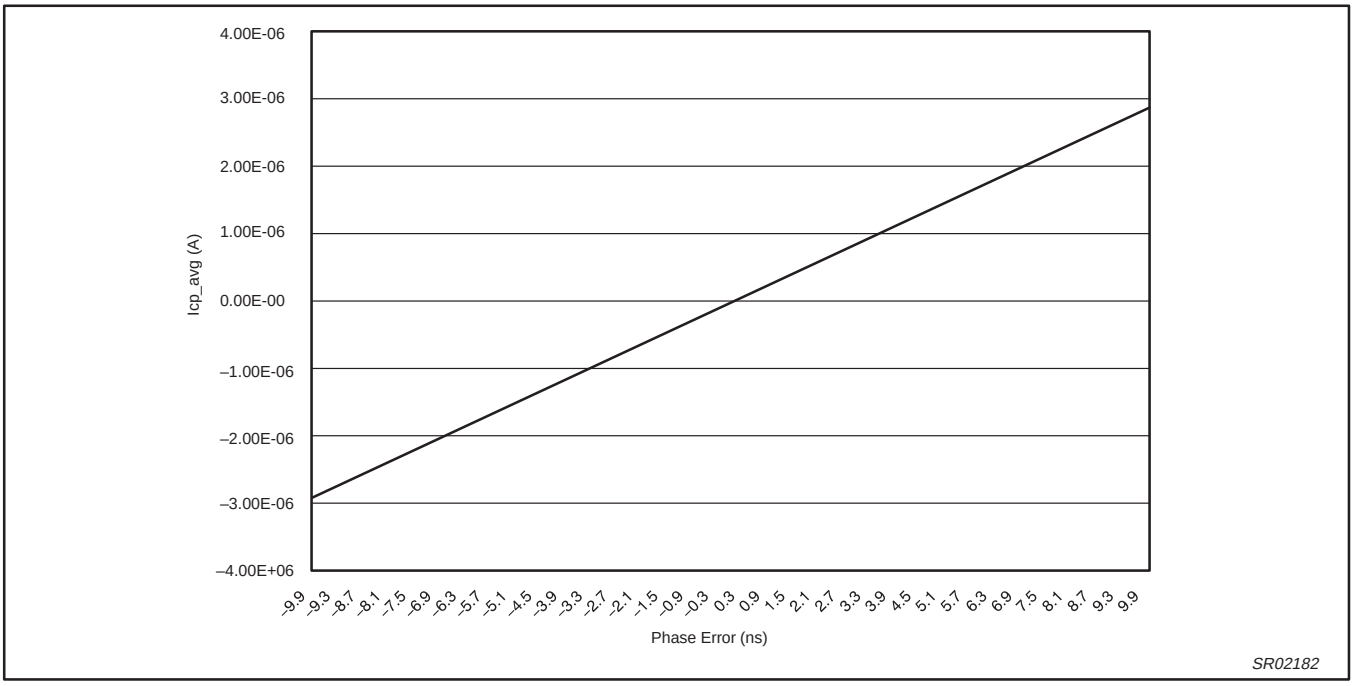
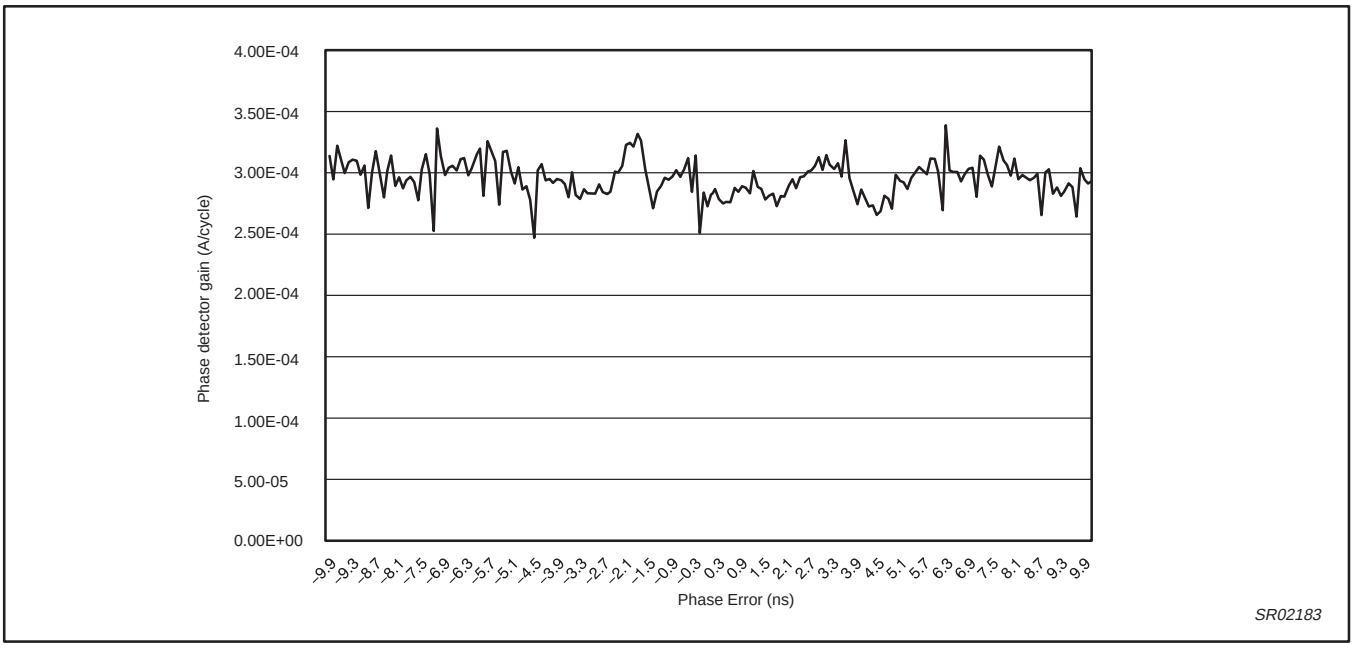


Figure 20. Charge pump current vs. phase error



Conditions: R_{SET} = 12 kΩ, CP = 00; I_{CP} = 306 μA, V_{CC} = 3.0 V

Figure 21. Phase detector gain

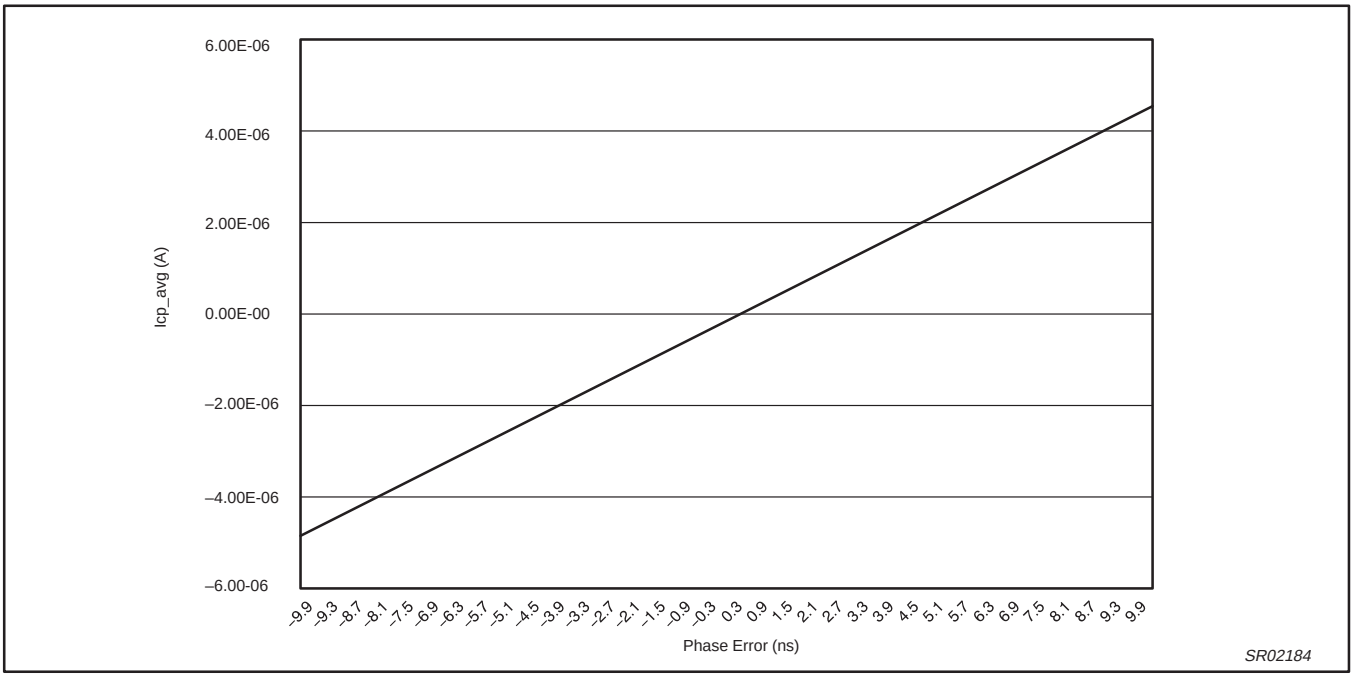
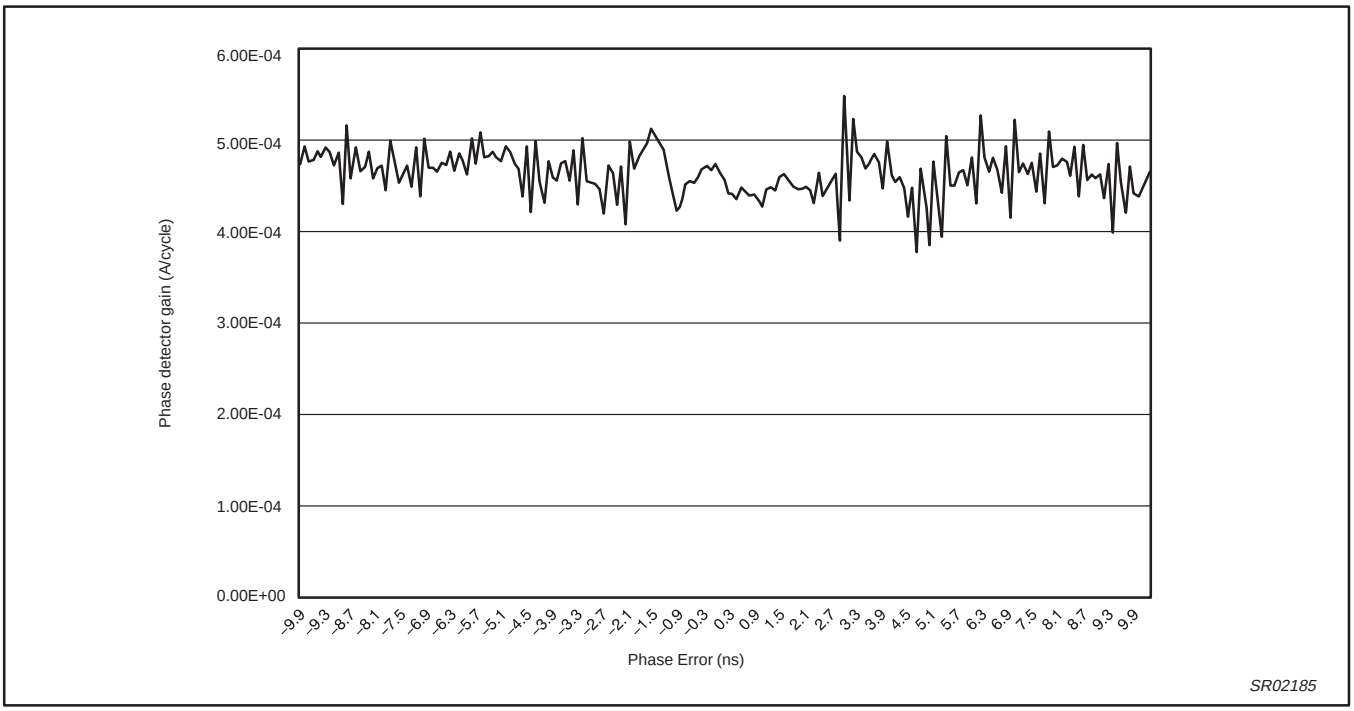


Figure 22. Charge pump current vs. phase error



Conditions: R_{SET} = 7.5 kΩ, CP = 00; I_{CP} = 492 µA, V_{CC} = 3.0 V

Figure 23. Phase detector gain

2.2. Fractional compensation

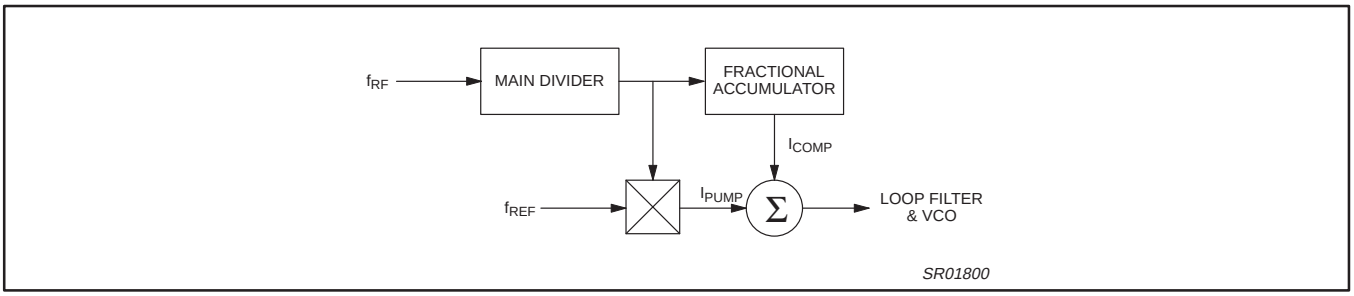


Figure 24. SA8026 fractional compensation method: current injection

SA8026 fractional compensation current is added to I_{PHP} and I_{PHI} via an 8-bit DAC (FDAC) to reduce the fractional spurs. Design target is for at least 15 dB of compensation with FDAC values of 80 for FMOD = 8 or 128 for FMOD = 5. The optimum FDAC value may be dependent on board layout and may vary up to 10%. The designer can get better fractional spur rejection by further tweeking the FDAC value.
The compensation current generated is:

$$I_{COMP} = \frac{I_{PUMP}}{128} \times \frac{FDAC}{5 \times 128} \times FRD \quad (3)$$

If FDAC is fixed, the compensation current is then directly proportional to the value contained in the fractional accumulator (FRD).

2.2.1. Find FDAC

At every cycle, the VCO advances on the reference by FRD/FMOD of the VCO cycle. The instantaneous phase error is then:

$$\frac{FRD}{FMOD} \times \frac{1}{VCO} \quad (4)$$

where FMOD is the modulus used. Therefore, the extra charge taken from the filter is given by:

$$Q_N = \frac{FRD \times I_{PUMP}}{FMOD \times VCO} \quad (5)$$

To compensate for this charge, we add an equal amount of charge to the filter.

$$Q_{COMP} = \frac{I_{PUMP}}{128} \times \frac{FDAC}{5 \times 128} \times FRD \times \frac{128}{VCO} \quad (6)$$

$$= \frac{I_{PUMP} \times FDAC \times FRD}{640 \times VCO} \quad (7)$$

Setting $Q_N = Q_{COMP}$ and solving for FDAC

$$\frac{FRD \times I_{PUMP}}{FMOD \times VCO} = \frac{I_{PUMP} \times FDAC \times FRD}{640 \times VCO} \quad (8)$$

$$\Longrightarrow \quad FDAC = \frac{640}{FMOD} \quad (9)$$

From Equation (9) above, the optimal theoretical FDAC value for FMOD = 8 is 80, and 128 for FMOD = 5.
Note that FDAC is:

- Independent of the reference frequency
- Independent of VCO frequency
- Independent of charge pump current.

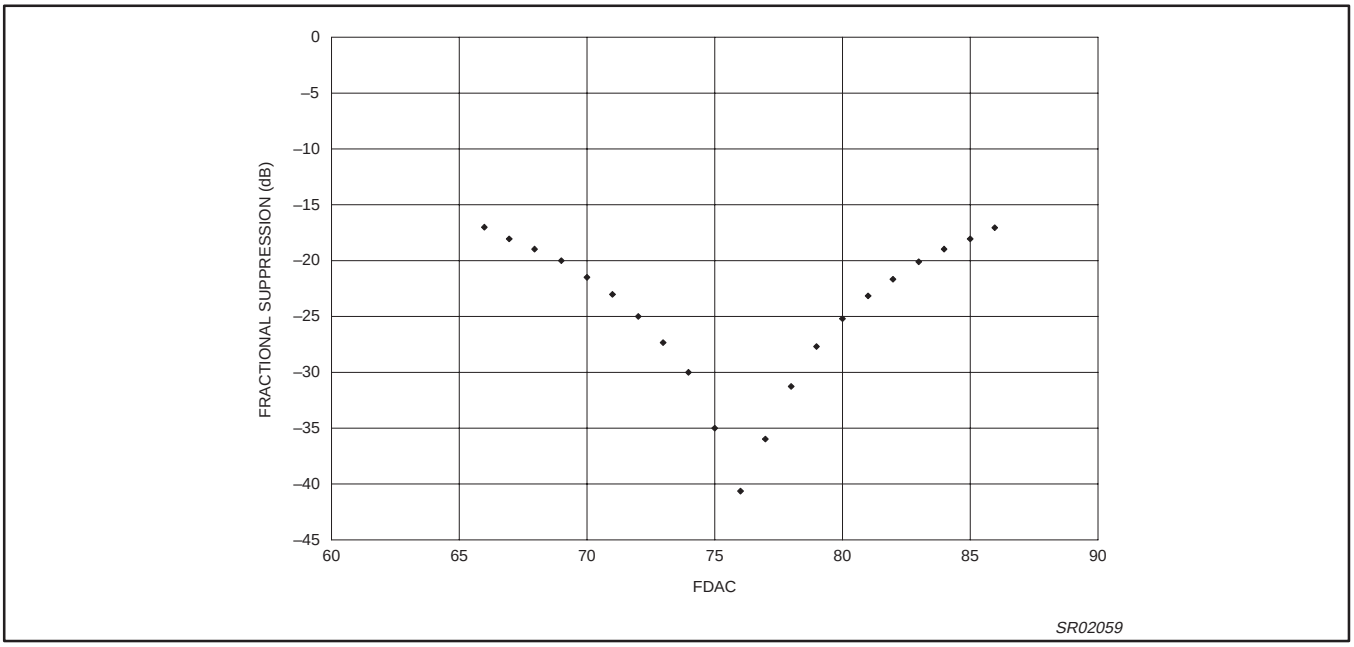


Figure 25. Fractional compensation for FMOD = 8

From Figure 25, the measured optimal FDAC value is 76. Note that the theoretical or expected optimal FDAC value is 80. Near the optimal value, minor variation of the FDAC value can result in large degradation of fractional suppression. FDAC can vary as much as 10–15 dB for ±2 counts. The characteristics of this curve will be the same from device to device but might be shifted by ±2 FDAC counts.

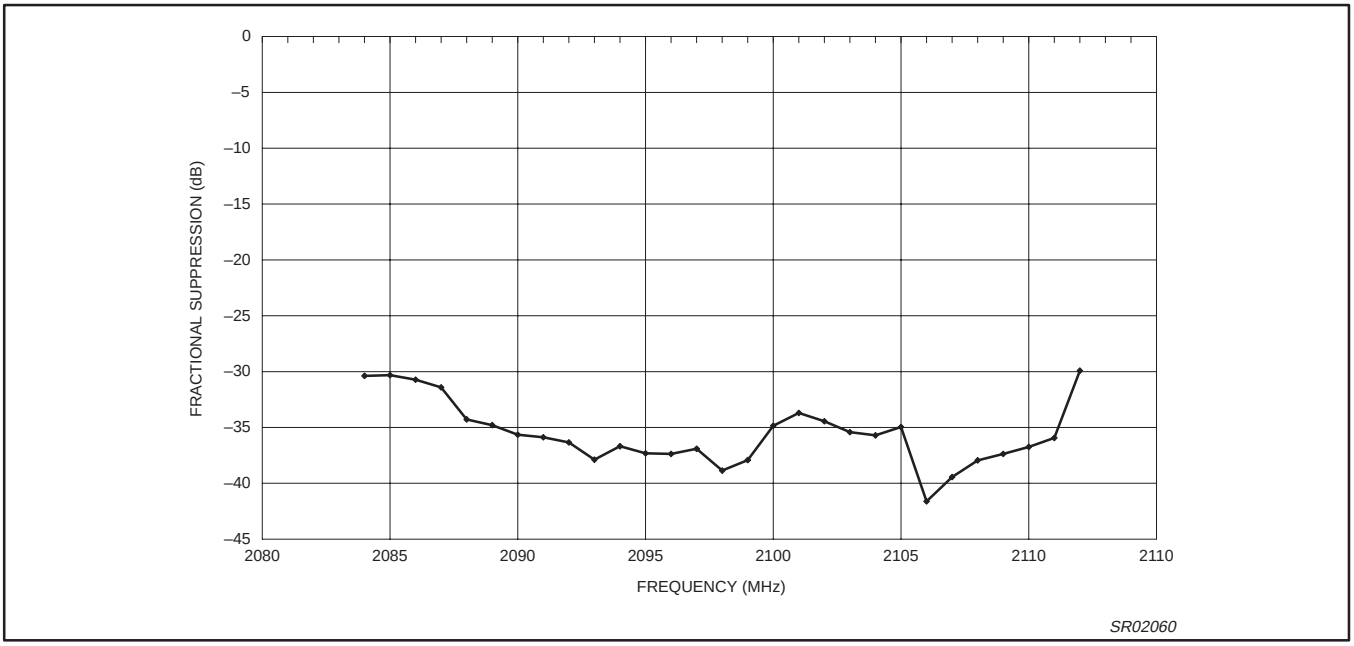
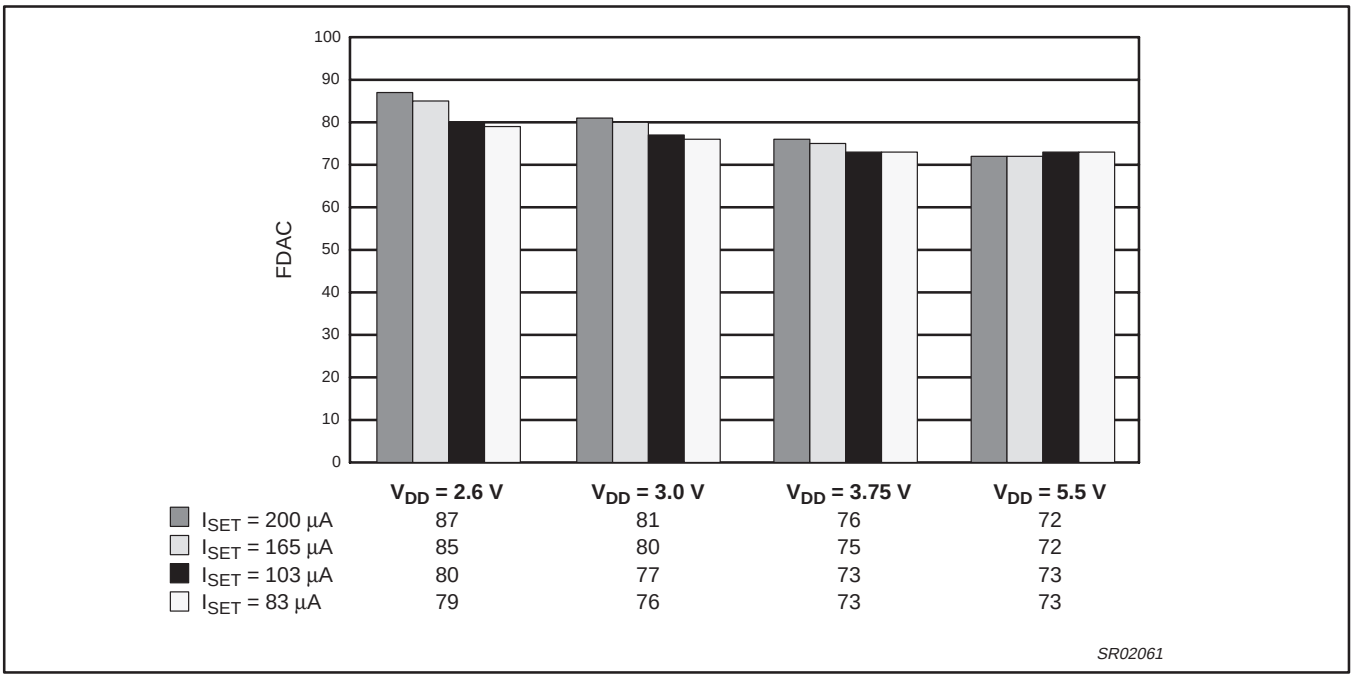


Figure 26. Fractional compensation across frequency, I_{SET} = 165 mA, V_{CC} = 3 V, FDAC = 76

Although it is desirable to have the fractional compensation constant across frequency, Figure 26 shows that it can vary as much as 10–15 dB. This is equivalent to ±2 counts as stated. If this variation is a problem, the designer can reprogram the FDAC to get back to the optimal compensation.

Figure 27 shows the average optimal FDAC for different I_{SET} and supply voltages. One way to predict the behavior of the fractional compensation is to look at the phase detector gain plot. Since the optimal FDAC value is also dependent on the board layout, the phase detector gain curve has that information. Ideally, the curve should be flat. If the curve is above or below the expected phase detector gain near the zero phase error, the FDAC value will have to adjust for it. This adjustment is based on the theoretical optimal FDAC value. Another plot that could help designers is Figure 28, which shows the performance of the fractional compensation with different I_{SET}. The designer can trade-off between I_{SET} and the amount of fractional compensation.



	V_{DD} = 2.6 V	V_{DD} = 3.0 V	V_{DD} = 3.75 V	V_{DD} = 5.5 V
I_{SET} = 200 µA	87	81	76	72
I_{SET} = 165 µA	85	80	75	72
I_{SET} = 103 µA	80	77	73	73
I_{SET} = 83 µA	79	76	73	73

Figure 27. SA8026 optimal FDAC value for FMOD = 8

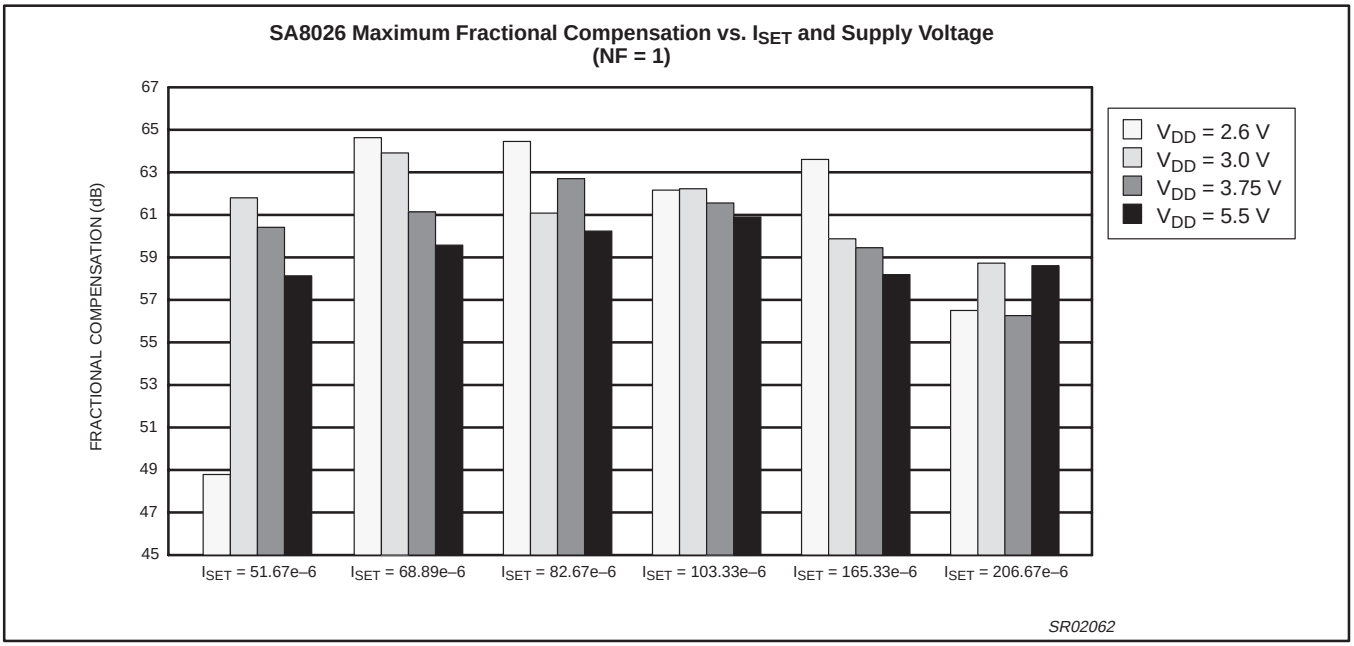


Figure 28. Fractional compensation vs. I_{SET}

2.3. Reference divider

The reference oscillator drives a preamplifier to provide the clock for the reference divider. The maximum frequency allowed is 40 MHz. For better noise performance, it is recommended that a TCXO be used. The reference divider is programmable with values between 4 and 1023 and followed by a three bit binary counter. The 3 bit SM (SA) determines which of the 5 output pulses are selected as the main (auxiliary) phase detector input. To avoid cross-talk between the main and auxiliary divider, the phase detector signals generated by the reference divider for the main phase detector occur at different time as the phase detector signal for the auxiliary divider.

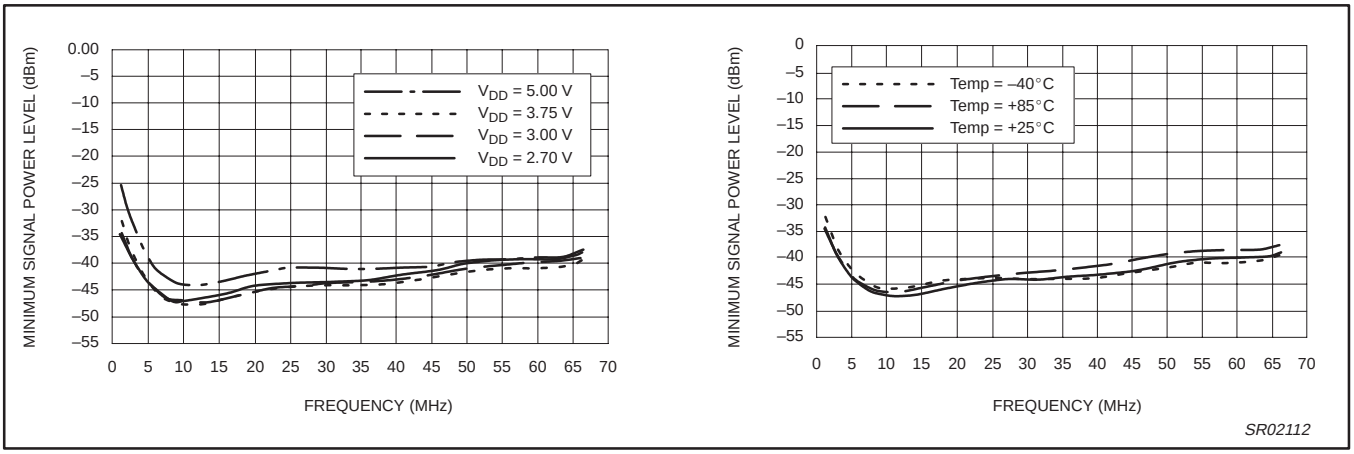


Figure 29. Reference input sensitivity

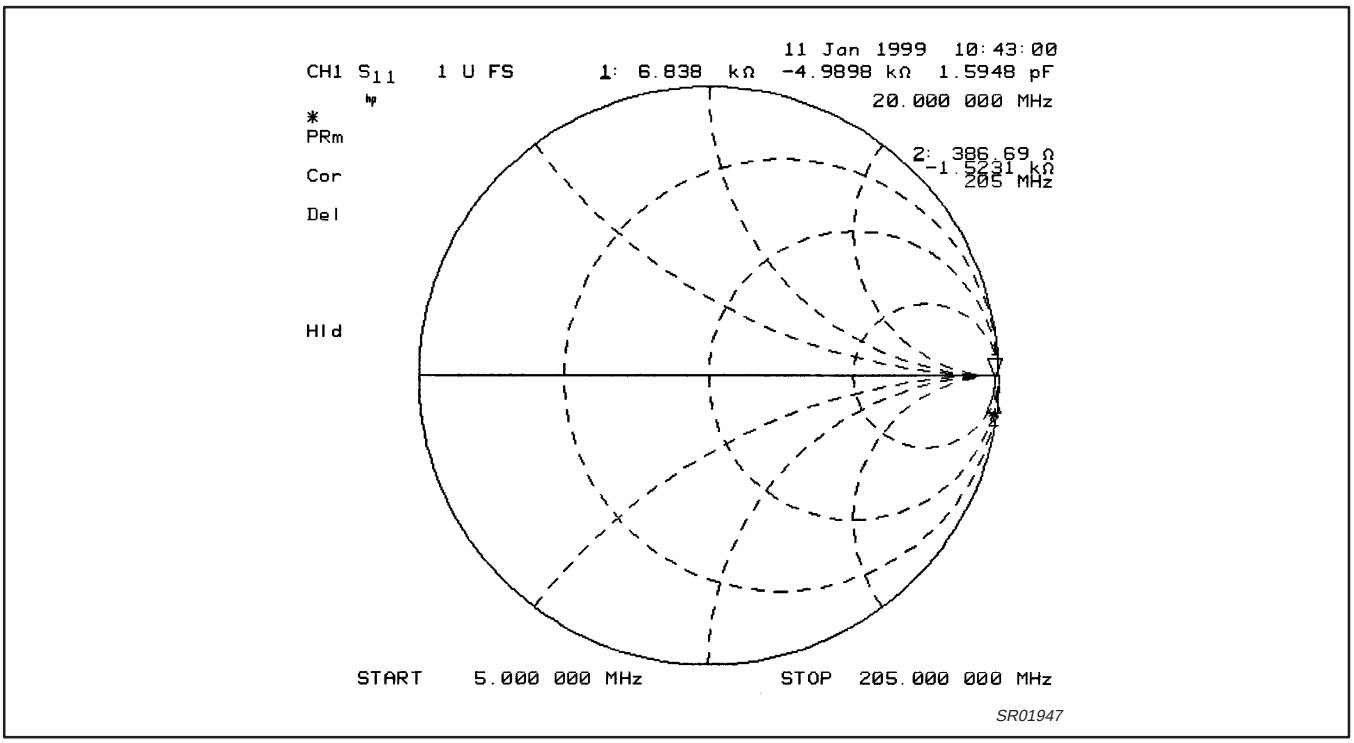


Figure 30. Reference input impedance

Table 3. Reference input impedance
Typical input impedance of the REF_{in} port at V_{DD} = 3.0 V

Frequency (MHz)	R_e (ms)	I_m (ms)	Resistance (kΩ)	Capacitance (pF)
5	0.09	0.02	10.91	0.50
13	0.10	0.05	10.50	0.65
21	0.10	0.07	10.48	0.55
29	0.10	0.10	10.05	0.53
37	0.11	0.12	8.86	0.52
45	0.10	0.14	9.64	0.48
53	0.11	0.16	8.93	0.49
61	0.11	0.20	9.27	0.52
69	0.11	0.20	9.12	0.47
77	0.11	0.24	8.97	0.49
85	0.11	0.26	9.31	0.49
93	0.11	0.29	9.30	0.50
101	0.11	0.31	8.74	0.49
109	0.10	0.33	9.61	0.49
117	0.13	0.35	7.76	0.48
125	0.12	0.38	8.30	0.49
133	0.12	0.41	8.01	0.49
141	0.11	0.44	8.74	0.50
149	0.14	0.45	7.37	0.48
157	0.15	0.48	6.83	0.49
165	0.14	0.51	7.22	0.49
173	0.14	0.53	6.95	0.49
181	0.15	0.56	6.70	0.49
189	0.16	0.57	6.20	0.48
197	0.17	0.59	5.98	0.48
205	0.16	0.62	6.36	0.48

2.4. Main divider

The RF_{in} differential inputs drive a pre-amplifier to provide the clock for the main divider. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. For single-ended operation, the input signal should be fed to one of the inputs while the other one is AC grounded. The divider consists of a fully programmable bipolar prescaler (first 7 LSBs) followed by a CMOS counter. Total divide ratios range from 512 to 65536.

At the completion of the main cycle, a main divider output pulse is generated which will drive the main phase comparator and the fractional accumulator is also incremented by the value of NF. When the accumulator overflows, the overall division ratio N will be increased by 1 to N+1, the average division ratio over FMOD (either 5 or 8 will be:

$$N_{frac} = N + \frac{NF}{FMOD} \quad (10)$$

The output of the main divider will be modulated with fractional jitter. The phase jitter is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

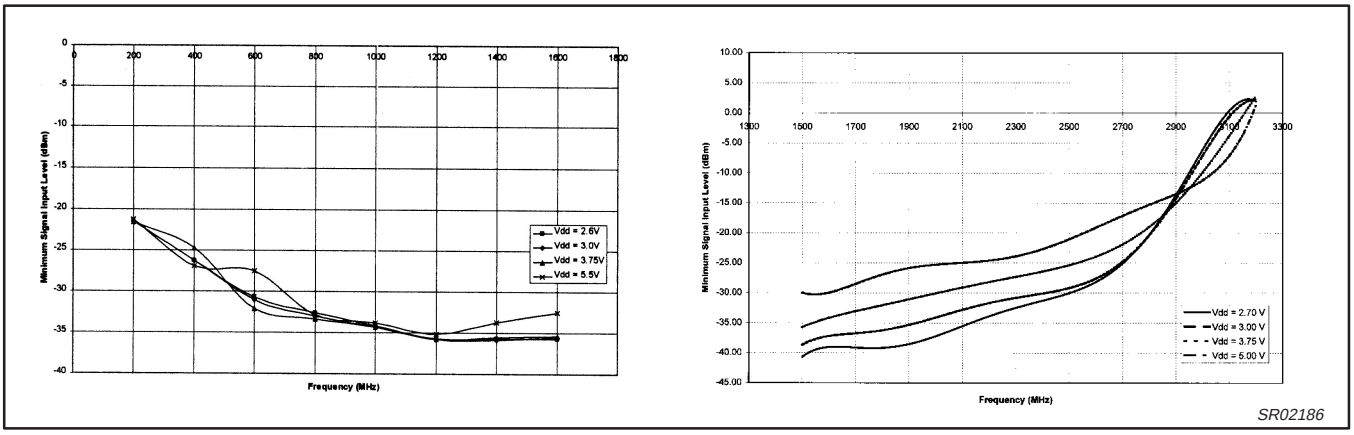


Figure 31. Main divider input sensitivity versus frequency and supply voltage (Temp = 25°C)

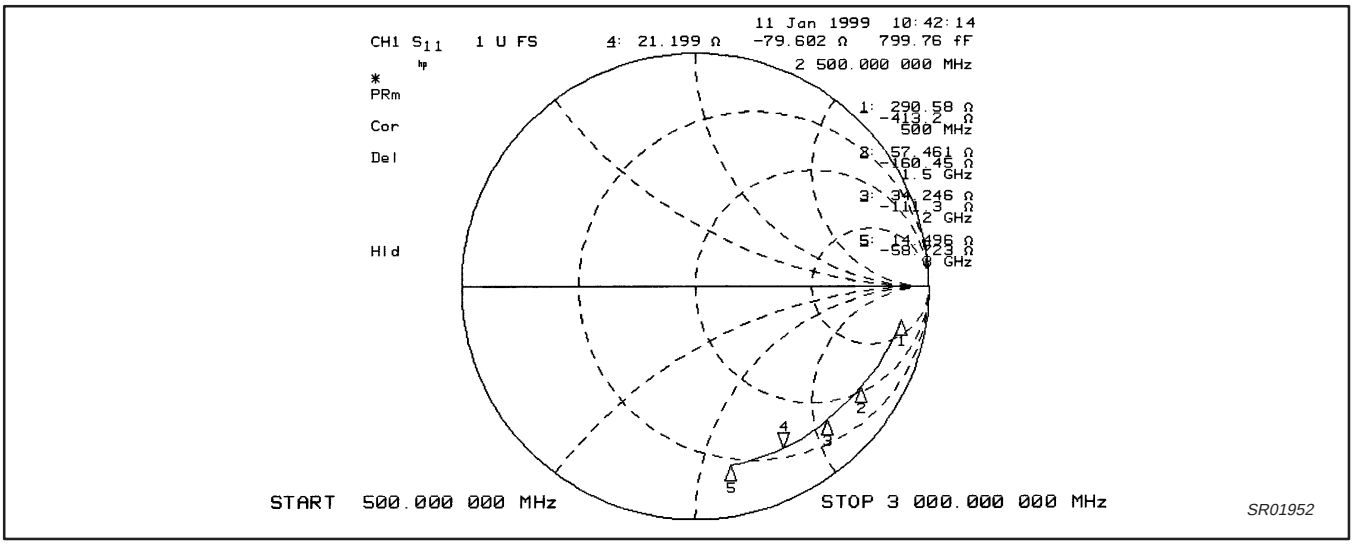


Figure 32. Main input impedance

Table 4. Main input impedance

Typical input impedance of the RF_{in} port at V_{DD} = 3.0 V

Frequency (MHz)	R_e (ms)	I_m (ms)	Resistance (kΩ)	Capacitance (pF)
500	1.15	1.64	0.87	0.52
600	1.22	1.97	0.82	0.52
700	1.28	2.30	0.78	0.52
800	1.37	2.50	0.73	0.53
900	1.47	2.80	0.68	0.55
1000	1.58	3.20	0.63	0.56
1100	1.69	3.60	0.59	0.58
1200	1.70	4.00	0.56	0.60
1300	1.80	4.60	0.52	0.62
1400	1.90	5.10	0.48	0.64
1500	2.00	5.50	0.45	0.67
1600	2.10	6.10	0.41	0.70
1700	2.20	6.80	0.38	0.73
1800	2.30	7.20	0.35	0.77
1900	2.40	7.60	0.33	0.80
2000	2.50	8.20	0.30	0.85
2100	2.60	9.10	0.28	0.91
2200	2.70	9.80	0.26	0.98
2300	2.80	10.40	0.23	1.06
2400	2.90	11.10	0.21	1.15
2500	3.10	11.70	0.19	1.26
2600	3.30	12.40	0.17	1.38
2700	3.50	13.40	0.15	1.52
2800	3.70	14.30	0.13	1.71
2900	3.90	15.30	0.11	1.93
3000	4.00	16.00	0.10	2.24

2.5. Auxiliary divider

The Auxiliary divider structure is the same as the main, except that there is no fractional capability and it is only a 14-bit divider. Permissible divide ratios range from 128 to 16384.

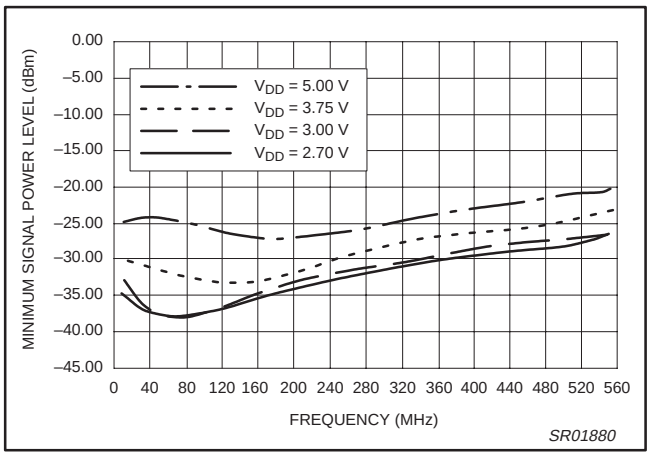


Figure 33. Auxiliary input sensitivity

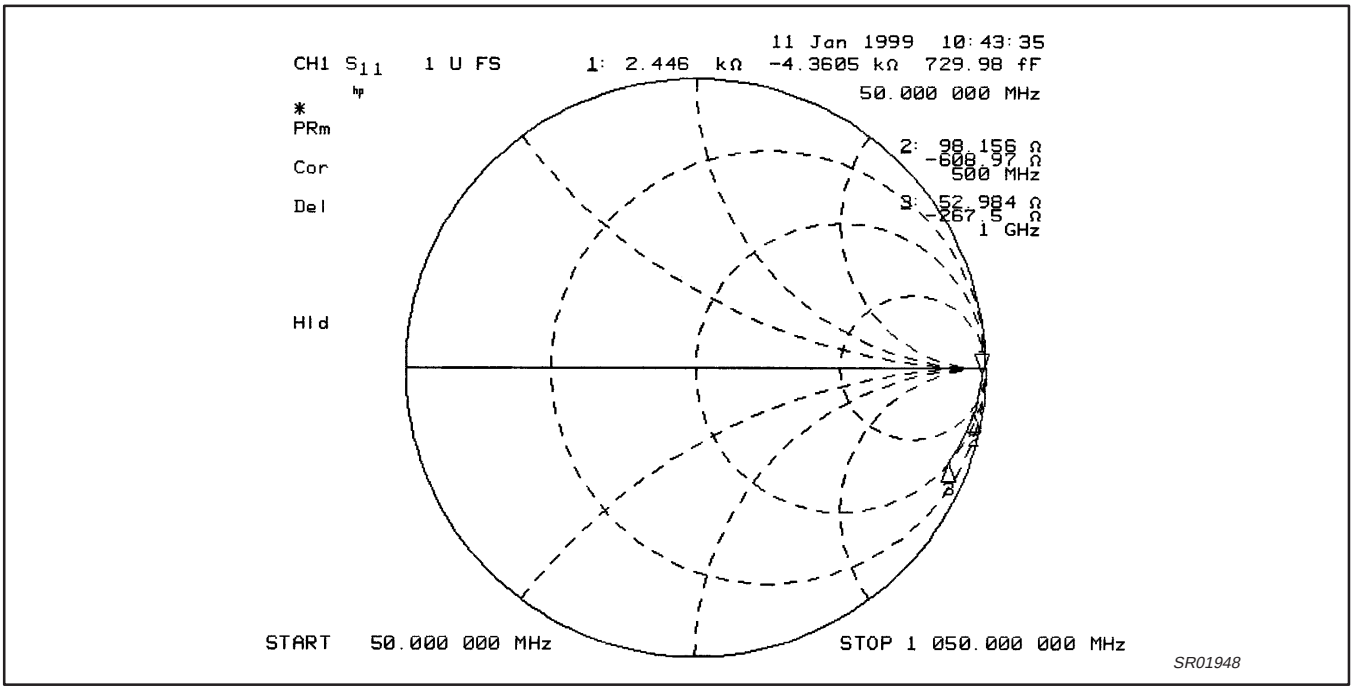


Figure 34. Auxiliary input impedance

Table 5. Auxiliary input impedance
Typical input impedance of the AUX_{in} port at V_{DD} = 3.0 V

Frequency (MHz)	R_e (ms)	I_m (ms)	Resistance (kΩ)	Capacitance (pF)
50	0.10	0.17	10.22	0.56
90	0.12	0.29	8.49	0.51
130	0.11	0.41	9.19	0.51
170	0.13	0.54	7.45	0.51
210	0.15	0.67	6.77	0.51
250	0.16	0.80	6.30	0.51
290	0.17	0.92	5.78	0.51
330	0.19	1.05	5.30	0.51
370	0.19	1.19	5.18	0.51
410	0.23	1.32	4.44	0.51
450	0.24	1.44	4.20	0.51
490	0.26	1.59	3.92	0.52
530	0.28	1.72	3.60	0.52
570	0.32	1.84	3.10	0.51
610	0.36	2.00	2.82	0.52
650	0.39	2.15	2.57	0.53
690	0.40	2.28	2.48	0.53
730	0.43	2.45	2.31	0.53
770	0.47	2.62	2.14	0.54
810	0.50	2.77	1.99	0.54
850	0.55	2.98	1.81	0.56
890	0.59	3.19	1.69	0.57
930	0.65	3.40	1.53	0.58
970	0.71	3.62	1.42	0.59
1010	0.77	3.89	1.29	0.61
1050	0.86	4.13	1.17	0.63

2.6. Lock detect

The output LOCK maintains a logic ‘1’ when the auxiliary phase detector is ANDed with the main phase detector. The lock condition for the main and the auxiliary synthesizers is defined as a phase difference of less than ± 1 period of the reference frequency.

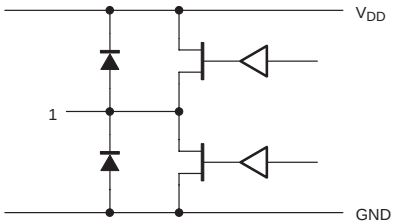
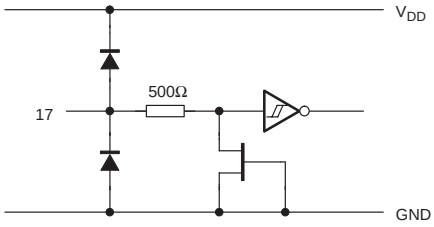
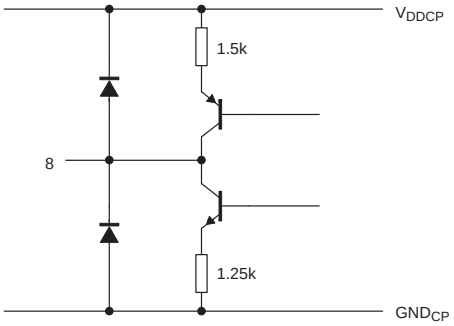
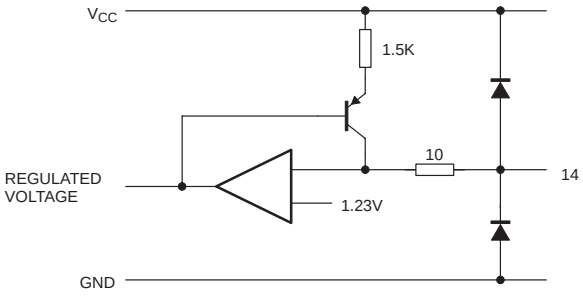
2.7. Power down

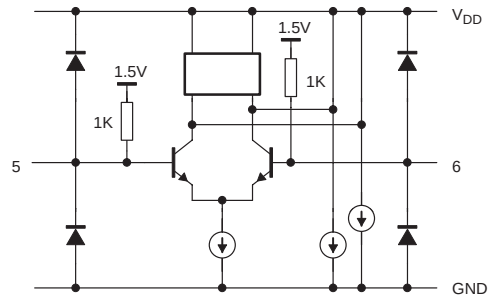
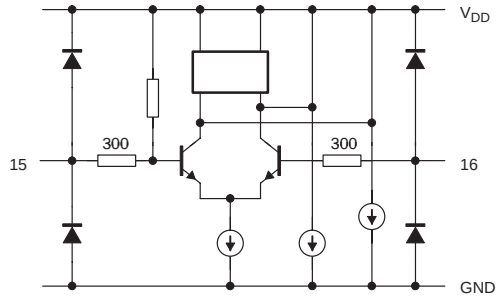
The SA8026 can be powered down either by hardware or software. The PON (hardware) signal is exclusively ORed with the PD (software) bits in the B-Word. If PON = 0, then the part is powered up when PD = 1. When the synthesizer is reactivated from power-down, the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

2.8. Test pin

The Test pin (Pin 2) is used as an input pin for the test mode. For normal operation of the synthesizer, this pin should be either grounded or connected to V_{DD}.

2.9. Pin functions

PIN NUMBER	PIN MNEMONIC	EQUIVALENT CIRCUIT
1	LOCK	
2	Test	
20	PON	
19	STROBE	
18	DATA	
17	CLOCK	
8	PHP	
9	PHI	
11	PHA	
14	R_{SET}	

PIN NUMBER	PIN MNEMONIC	EQUIVALENT CIRCUIT
5	RF_{in+}	
6	RF_{in-}	
12	AUX_{in}	
16	REF_{in+}	
15	REF_{in-}	

3. LOOP FILTER DESIGN

3.1. Normal design equations

δ : Final frequency resolution after settling

$$\delta = \frac{\text{frequency error after settling}}{\text{switching step}} \quad (11)$$

t_{sw} : Switching time (sec)

f_n : Natural frequency

ω_n : $2\pi f_n$ (rad/sec)

N : Divide ratio

ζ : Damping factor

K_{VCO} : VCO gain (Hz/V) or $2\pi \cdot$ VCO gain (rad/V)

K_Φ : Phase detector gain = Icp/2π (A/rad)

$$\omega_n = \frac{-1n\left(\delta \cdot \sqrt{1-\zeta^2}\right)}{\zeta \cdot t_{sw}} \quad (12)$$

$$C_1 = \frac{K_\phi \cdot K_{VCO}}{N \cdot {\omega_n}^2} \quad (13)$$

$$R_1 = 2 \cdot \zeta \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C_1}\right)^{0.5} \quad (14)$$

$$C_2 \leq \frac{C_1}{10} \quad (15)$$

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_n \quad (16)$$

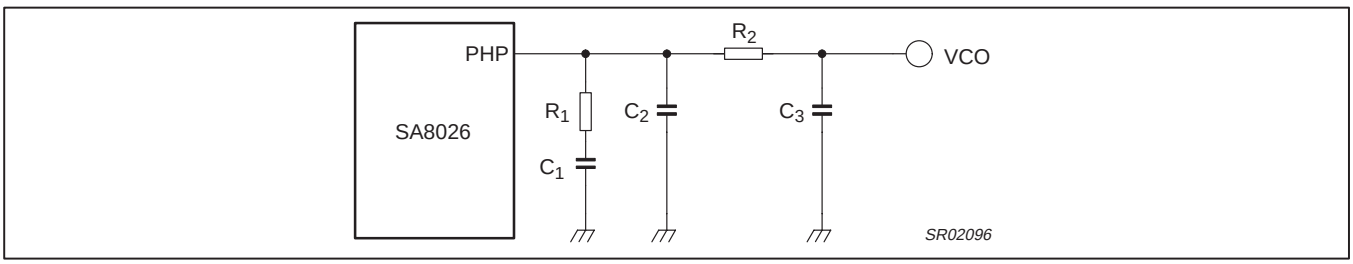


Figure 35. Loop filter

$$BW_{3dB} = \frac{\omega_n}{2\pi}\left[\ 2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2+1}\ \right]^{1/2} \quad (17)$$

3.2. Design example

This design example will give the user an idea of the performance of all parameters: phase noise, fractional spurs compensation, comparison spurs, and switching time. The resulting components are used on the demo board. For a quick AC verification of the demo board, the user can refer to the measured plots in this application note.

VCO frequency (f_{VCO}) = 2083 to 2108 MHz

Channel spacing (f_{chan}) = 30 kHz

Comparison frequency (f_{comp}) = 8 · 30 kHz = 240 kHz

Switching time (t_{sw}) = 400 μsec

Switching step = 25 MHz

Frequency error = within 1 kHz

VCO gain (K_{VCO}) = 40 MHz/V Murata MQG101-2098

Reference crystal (f_{ref}) = KSS VCTCXO 19.44 MHz

Determine R_{SET}:

Choose I_{CP} = 500 μA ; CP = 00 (Table 2 on Page 5)

$$I_{CP} = 3 \cdot I_{SET} = \frac{3 \cdot V_{SET}}{R_{SET}} = \frac{3 \cdot 1.25}{R_{SET}} = 500\ \mu A$$

R_{SET} = 7.5 kΩ

Determine N:

To ensure the same switching time from both directions, we use the worst case,

$$N = \frac{2108MHz}{240kHz} = 8783$$

Determine ω_n:

From Equation (11)

$$\delta = \frac{1000}{25e6} = 0.04e{-}3$$

Pick ζ = 0.707 … critically damped

From Equation (12)

$$\omega_n = \frac{-\ln\left(0.04e{-}3 \cdot \sqrt{1-0.707^2}\right)}{0.707 \cdot 400e{-}6} = 37034 rad/s$$

Determine R_1, C_1, C_2:

Using Equation (13) with 2π from K_{VCO} (rad/V) and $^1/_2\pi$ from K_Φ (A/rad) canceled out,

$$C_1 = \frac{500e{-}6 \cdot 40e6}{8783 \cdot 37034^2} = 1.67nF \qquad \Rightarrow \text{use } 1.8\ nF$$

Using Equation (14)

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{8783}{500e{-}6 \cdot 40e6 \cdot 1.8e{-}9}\right)^{0.5} = 22.086k\Omega \qquad \Rightarrow \text{use } 22\ k\Omega$$

Using Equation (15)

$$C_2 = \frac{1.8e{-}9}{10} = 180pF$$

Determine R_2, C_3:

Using Equation (16)

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_n$$

For the Auxiliary Synthesizer, follow the same procedure as described above.

VCO frequency (f_{VCO}) = 492.9 to 500.9 MHz
Comparison frequency (f_{comp}) = 240 kHz
Switching time (t_{sw}) = 1.8 ms
VCO gain (K_{VCO}) = 6 MHz/V

Determine N:

$$N = \frac{500MHz}{240kHz} = 2083$$

Determine ω_n:

$$\delta = \frac{1000}{25e6} = 0.04e{-}3$$

Pick $\xi = 0.707$

$$\omega_n = \frac{-\ln\left(0.04e{-}3 \cdot \sqrt{1-0.707^2}\right)}{0.707 \cdot 1800e{-}6} = 8230 rad/s$$

Determine R_1, C_1, C_2:

$$C_1 = \left(\frac{250e{-}6 \cdot 6e6}{2083 \cdot 8230^2}\right) = 10.63nF \quad \Rightarrow \text{use } 10\ nF$$

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{2083}{250e{-}6 \cdot 6e6 \cdot 10e{-}9}\right)^{0.5} = 16.67k\Omega \quad \Rightarrow \text{use } 18\ k\Omega$$

$$C_2 = \frac{10e{-}9}{10} = 1\ nF$$

3.3. Performance measurements

The following parameters are measured for performance verification:

- Close-in phase noise/integrated phase jitter
- Fractional spurs compensation
- Comparison spurs
- Switching time

Close-in phase noise is measured using the marker noise option on a HP8563 spectrum analyzer. If this option does not exist, a common way of measuring the phase noise is by reading the level at a particular offset (usually 1 kHz) with respect to the carrier (dBc). Use the equation below to calculate the phase noise.

Phase noise (dBc/Hz) = dBc – 10log(RBW), where RBW is the resolution bandwidth of the spectrum analyzer.

Note that using the equation above will yield a phase noise result approximately 2 dB better than with the marker noise option. This is because the marker noise option already adds a correction factor of 2.5 dB to the measurement in consideration of the actual noise power bandwidth and equipment accuracy (see Phase Noise Setup).

Switching time is measured using a HP53310A Modulation Domain Analyzer. Use external trigger with the 3-wire bus strobe as the trigger source (see Switching Time Setup).

Integrated phase jitter and residual FM are measured using a Rohde and Schwarz Modulation Domain Analyzer or by using the formulae below with the single sideband phase noise plot.

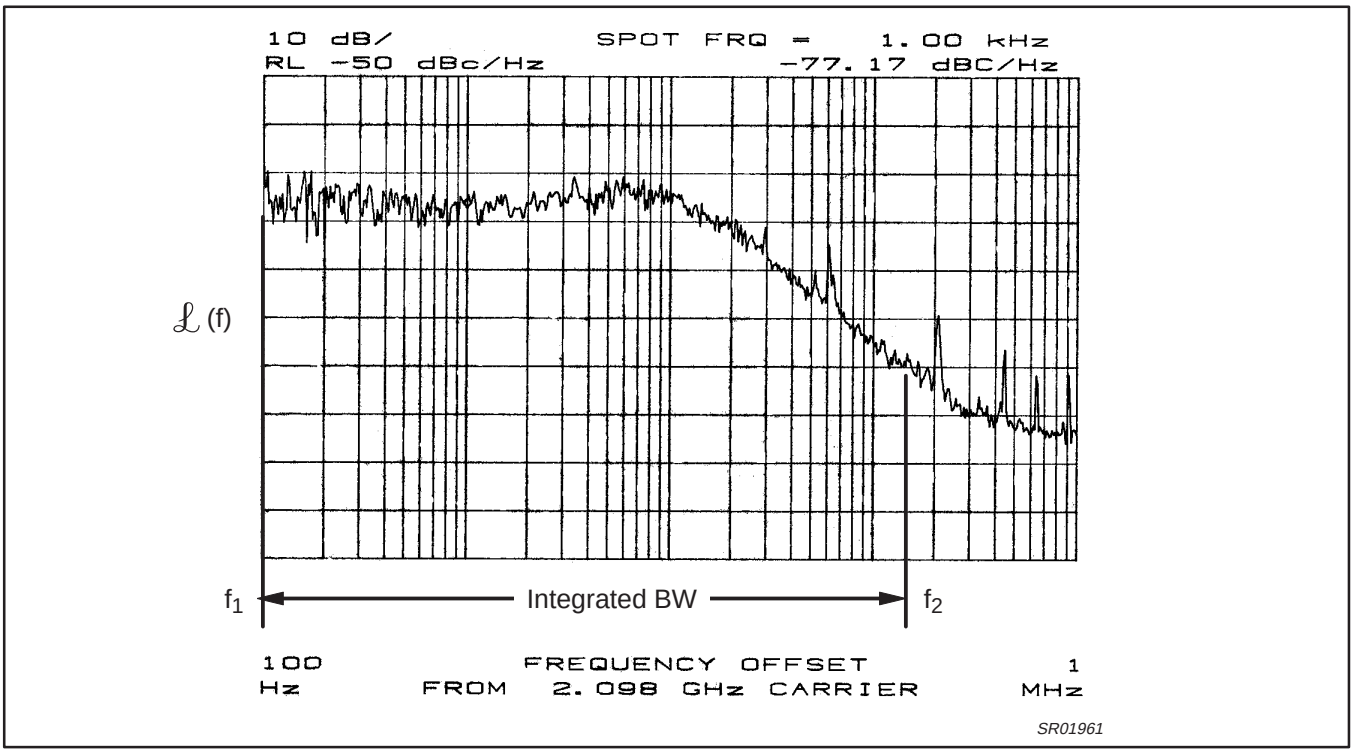


Figure 36.

Integrated phase jitter:

$$\sigma_\phi = \sqrt{\int_{f_1}^{f_2} S_\phi\,(f)df} \qquad (18)$$

Where f_1 is normally taken from 0.001R to 0.05R and f_2 is normally taken to be equal to R. R is the symbol rate in hertz for digital communications systems. $S_\phi(f) = 2\mathcal{L}(f)$.

Integrated residual FM:

$$\sigma_f = \sqrt{\int_{f_1}^{f_2} f^2 S_\phi\,(f)df} \qquad (19)$$

Where f_1 and f_2 are offset frequencies for which the quantity applies. $S_\phi(f) = 2\mathcal{L}(f)$.

3.4. Performance results

3.4.1. Simulated results of design example

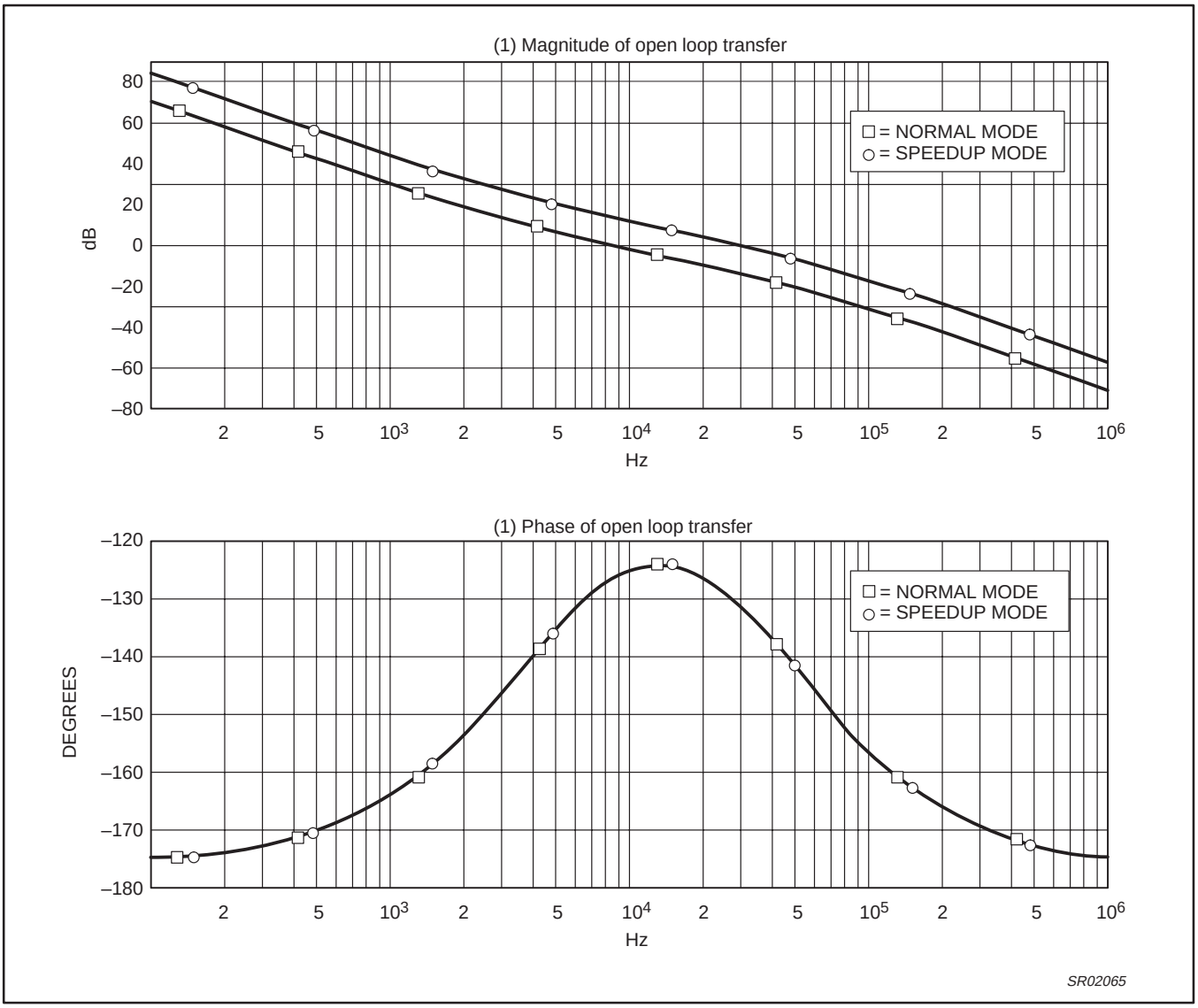


Figure 37. Open loop response for design example.

The phase margin is around 53° in normal mode, and 48° in speedup mode. If PHI charge pump were connected to PHP for an I_{CP} of 8.5 mA in speedup mode, the phase margin would have reduced to 29°. Thus there would be peaking in the response as loop becomes less stable. A better way is to connect the PHI output to the integrating capacitor for two different loop responses. This approach is described in the “adaptive mode” section.

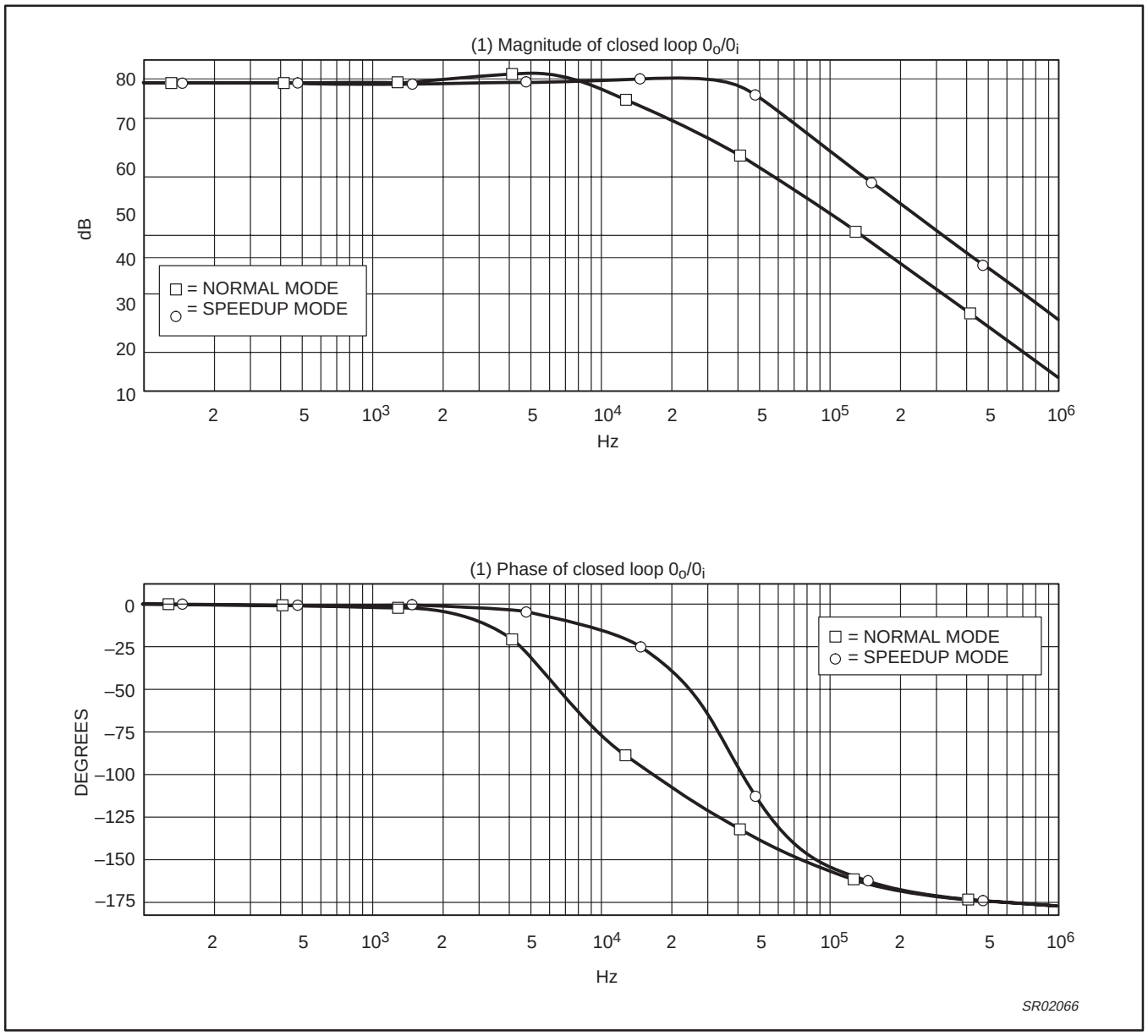


Figure 38. Closed loop response for design example.

3.4.2. Loop bandwidth measurement

Loop BW calculated from Equation (17) in Section 3.1. “Loop Filter Design” is 12.13 kHz. Figures 39 and 40 show the actual loop bandwidth which correlates well with the design equations and simulated results of Figure 38.

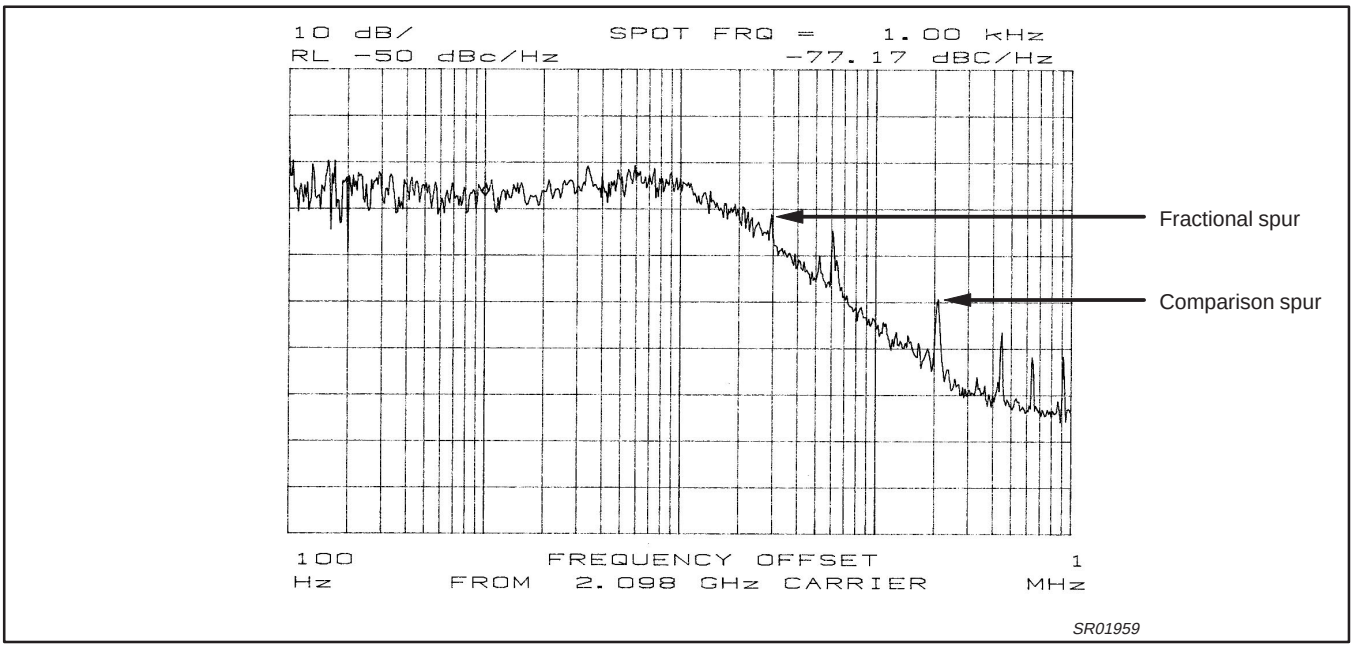


Figure 39. Loop bandwidth normal mode: CP = 10

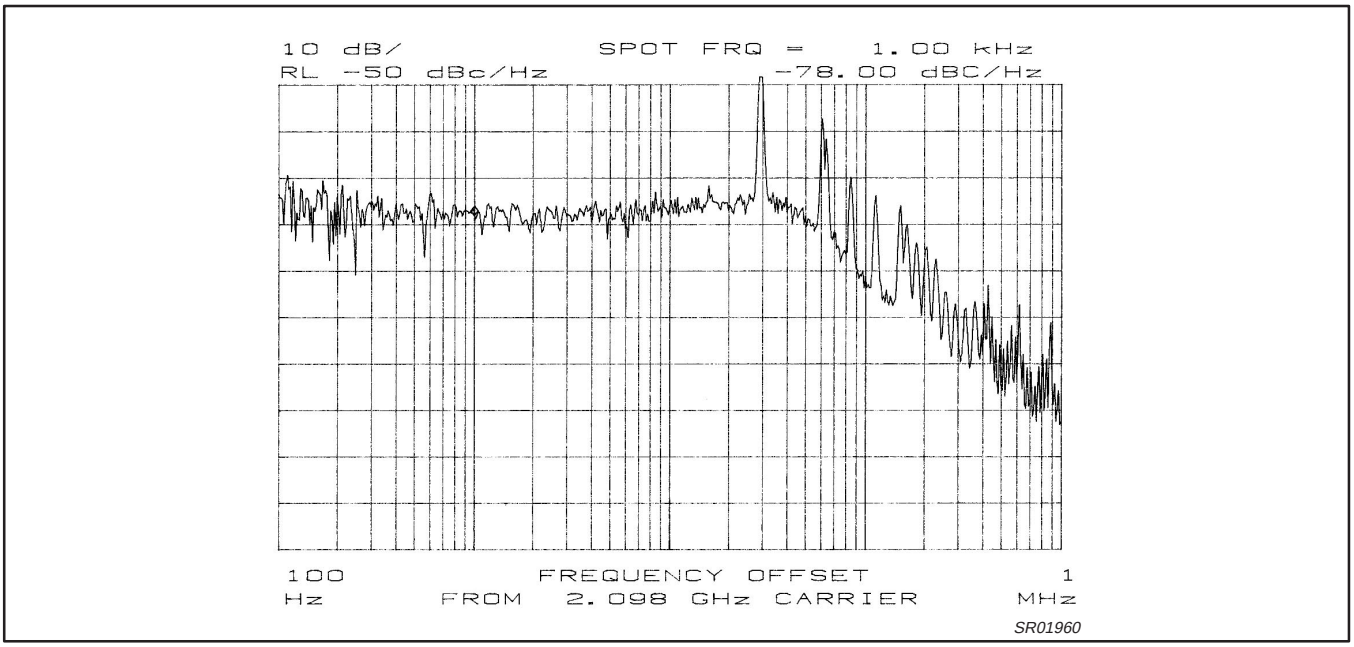


Figure 40. Loop bandwidth speedup mode: CP = 10

With the same FDAC value as in normal mode, spurs are enhanced during speedup mode. The designer needs to adjust the FDAC value if speedup mode is used all the time.

3.4.3. Main phase noise

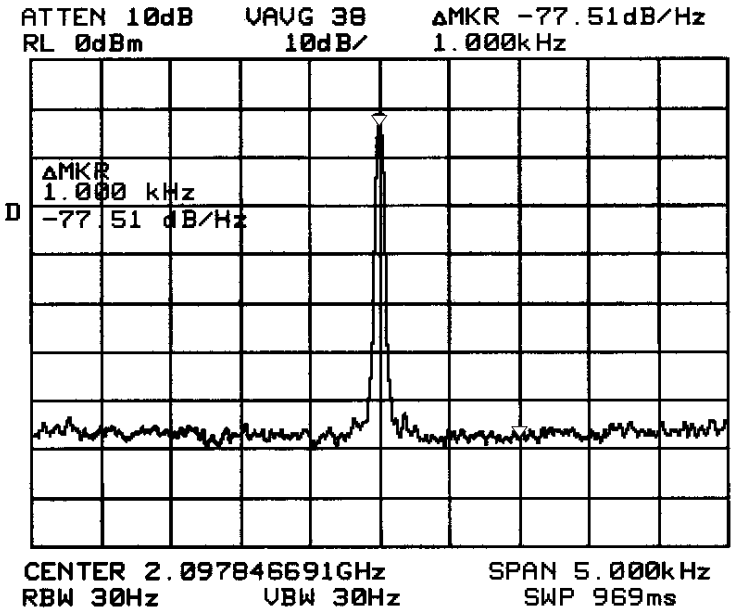


Figure 41. Main phase noise (@ 1 kHz offset = –77.51 dBc/Hz)

3.4.4. Noise floor

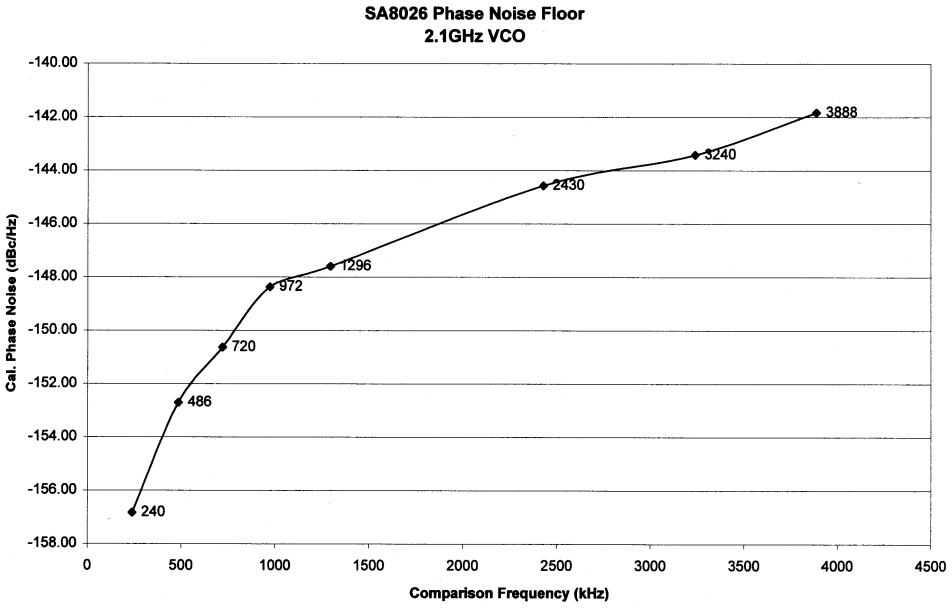


Figure 42. Noise floor

Figure 42 shows the noise floor for different comparison frequencies. This plot is obtained by measuring the close-in phase noise at 1 kHz offset and then subtracting 20log(N), where N is the main divider ratio.

3.4.5. Comparison spurs

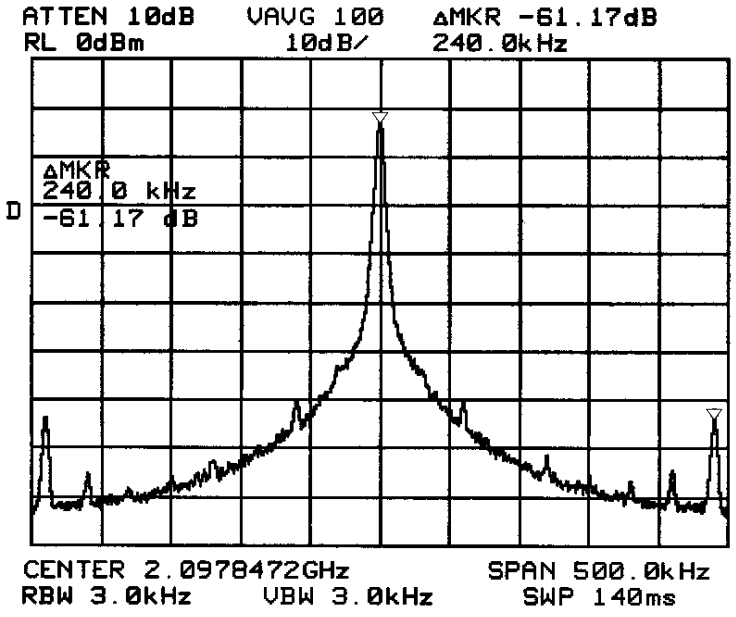


Figure 43. Comparison spur (@ 240 kHz = –61.17 dBc)

Comparison spurs are mainly caused by the mismatch of the charge pumps. However, leaky external components, such as loop filter capacitors and VCO, will also contribute to this spur.

3.4.6. Fractional compensation performance

The quickest way to check for fractional compensation performance is to set FDAC = 0, then increase FDAC until optimal compensation is found. Figure 44 shows the fractional spur with the FDAC set to 0. Note, there is some attenuation from the loop filter. Note that this value may vary by a few counts from device to device. This variation is also board layout, V_{CC}, and I_{SET} dependent.

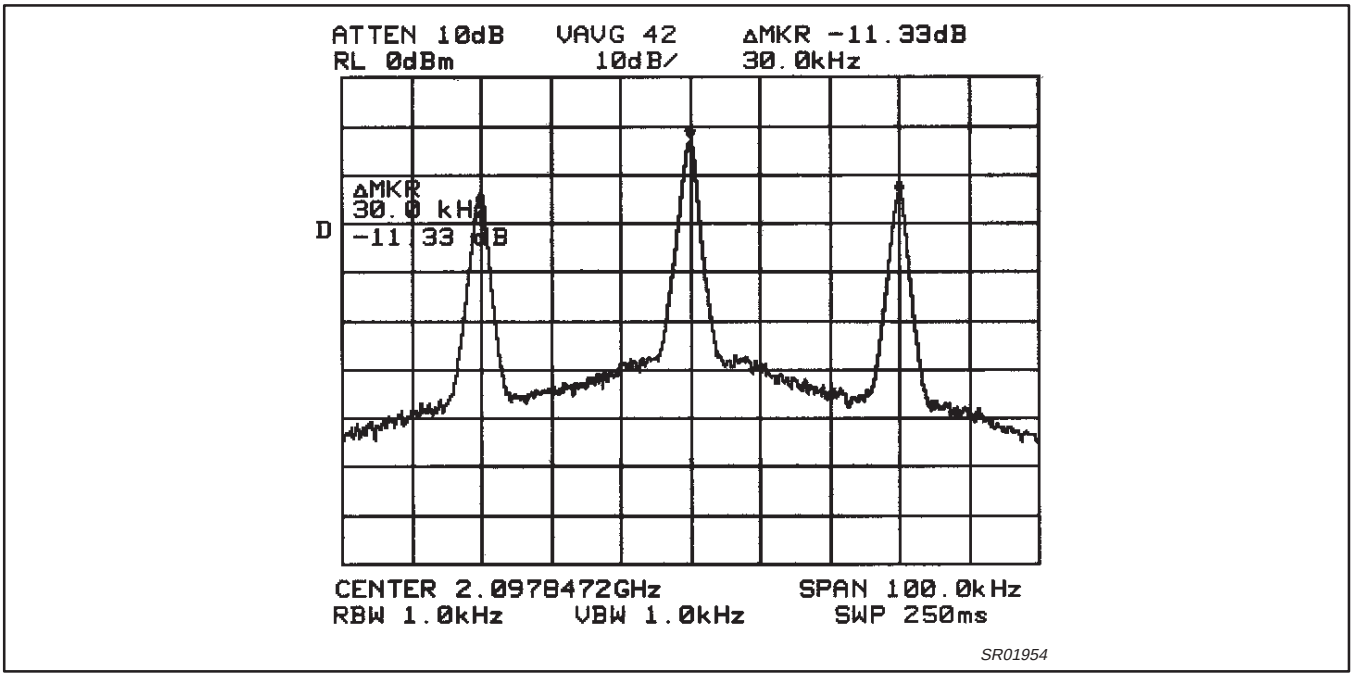


Figure 44. Fractional spur @ 30 kHz = –11.33 dBc, FDAC = 0 (uncompensated)

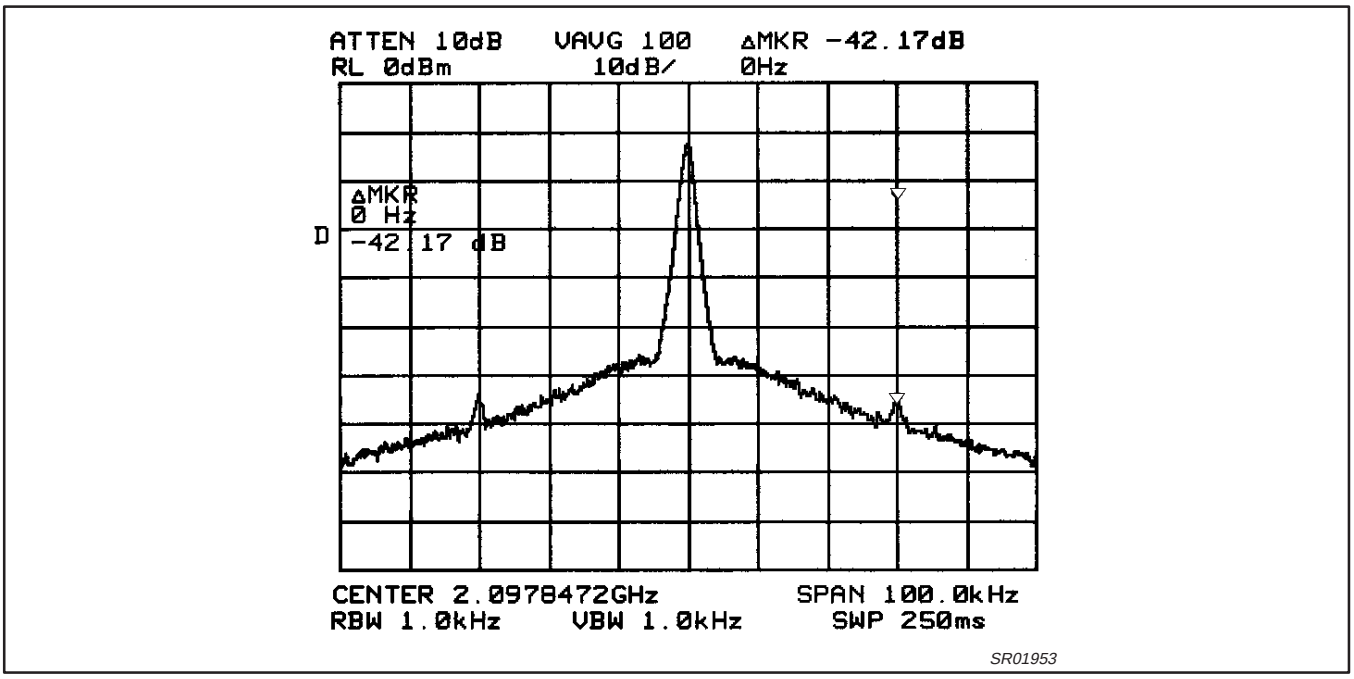


Figure 45. Fractional spur @ 30 kHz = –53.5 dBc, FDAC = 76 (compensated)

3.4.7. Switching time measurement

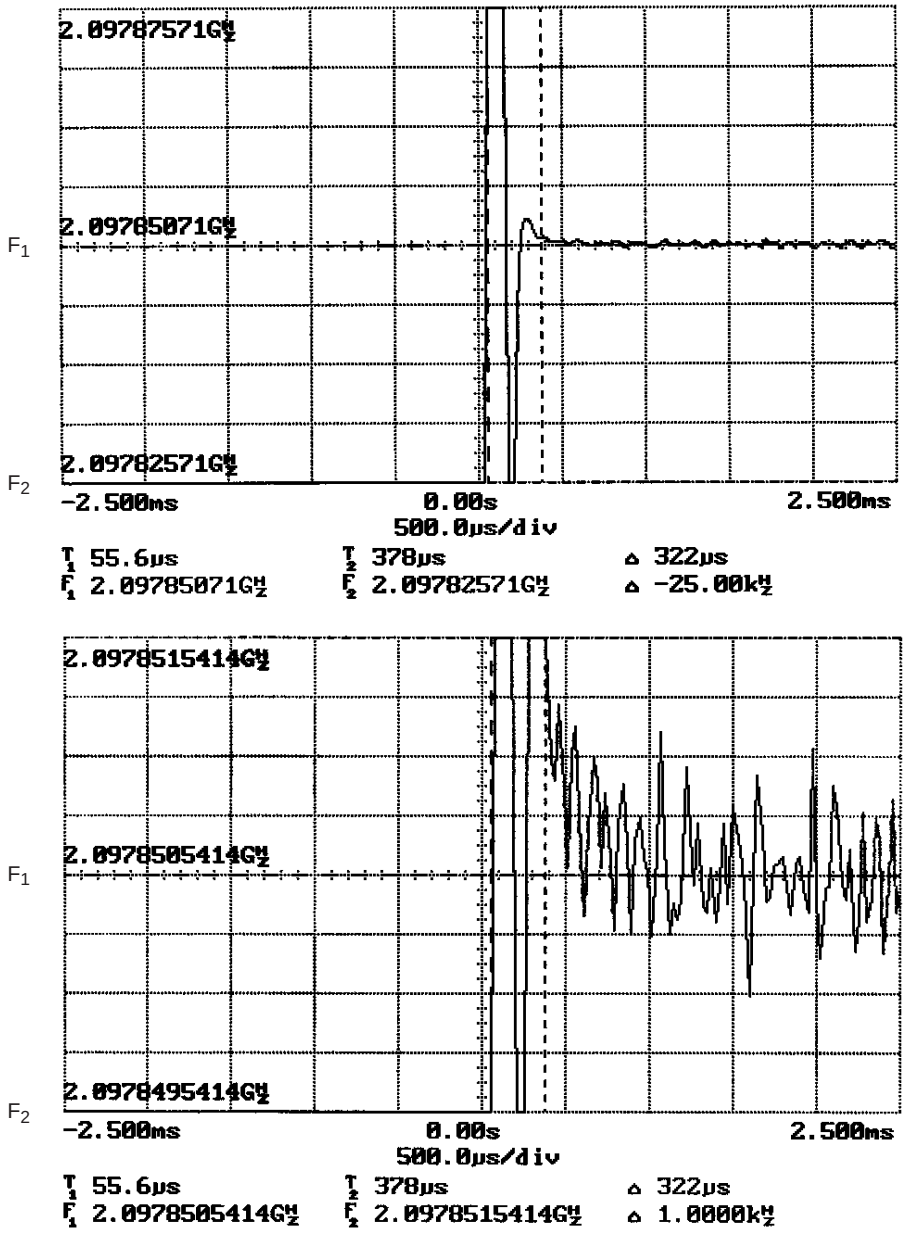
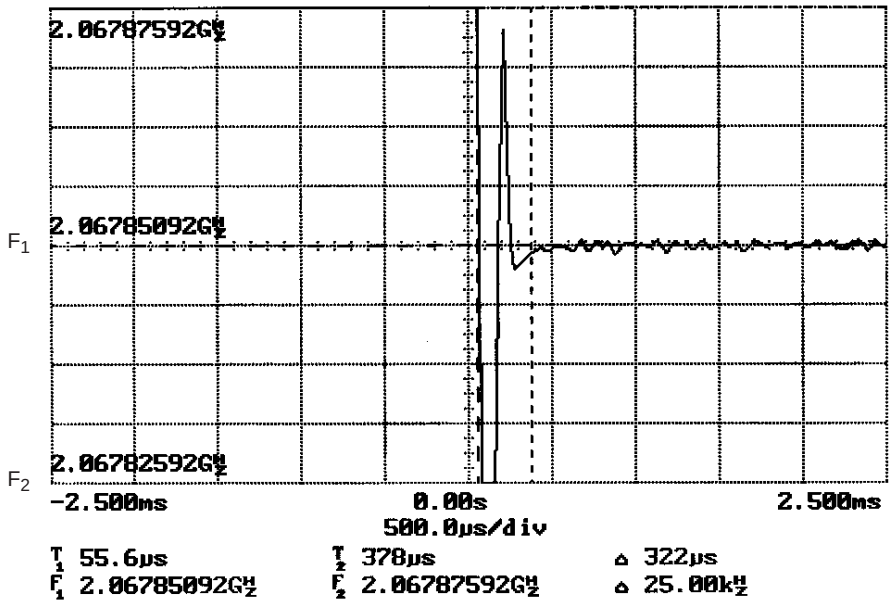


Figure 46. Low-to-High switching to within 1 kHz (30 MHz jump)



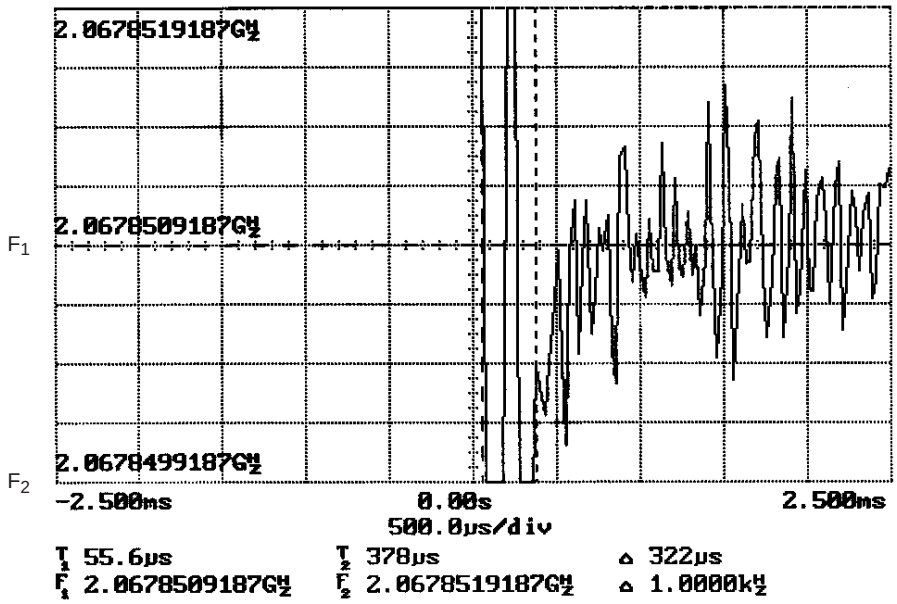


Figure 47. High-to-Low switching to within 1 kHz (30 MHz jump)

3.4.8. Secondary glitch

A secondary glitch occurs when the charge pumps go from speedup to normal mode. This switching causes a difference in final phase error due to different current gains which results in frequency instability or glitch in the frequency domain. It will, in effect, cause the switching time to be longer depending on the loop bandwidth. One way to combat this problem is to experiment with the strobe pulse width to optimize the duration that the charge pumps remain in speedup mode.

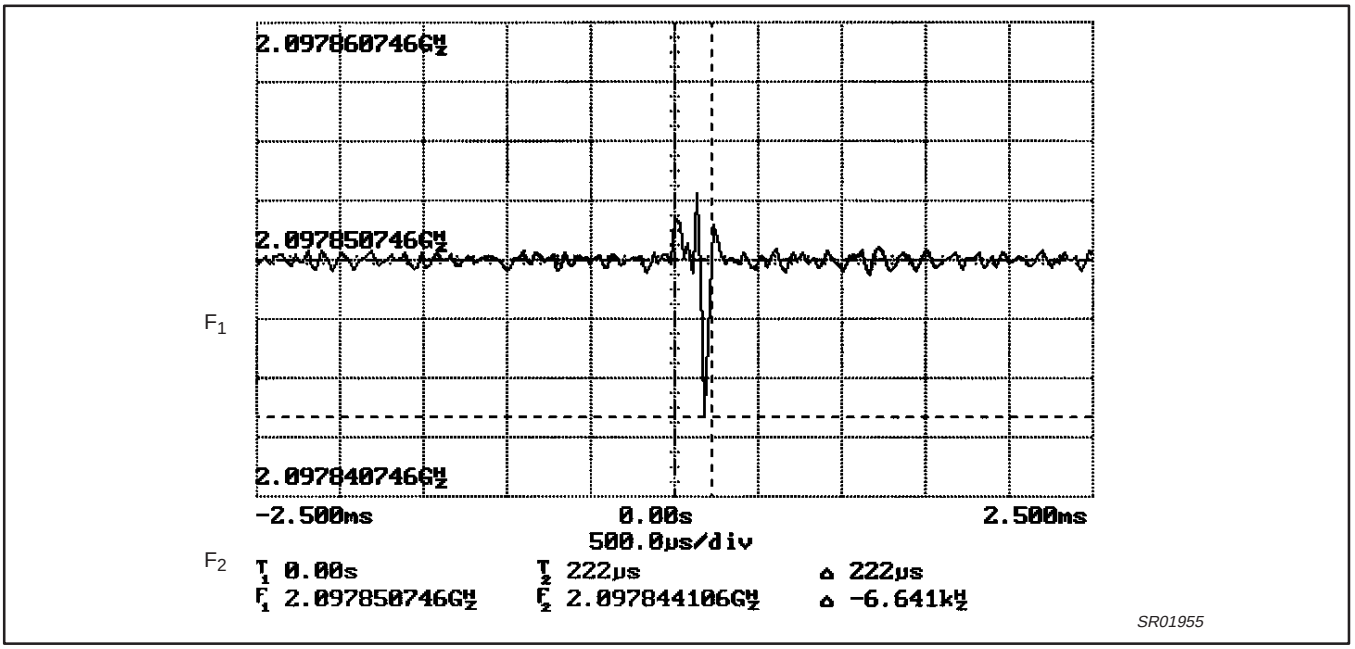


Figure 48. Strobe pulse width = 200 µs in software (WINSYNTH); frequency pull = 6.6 kHz

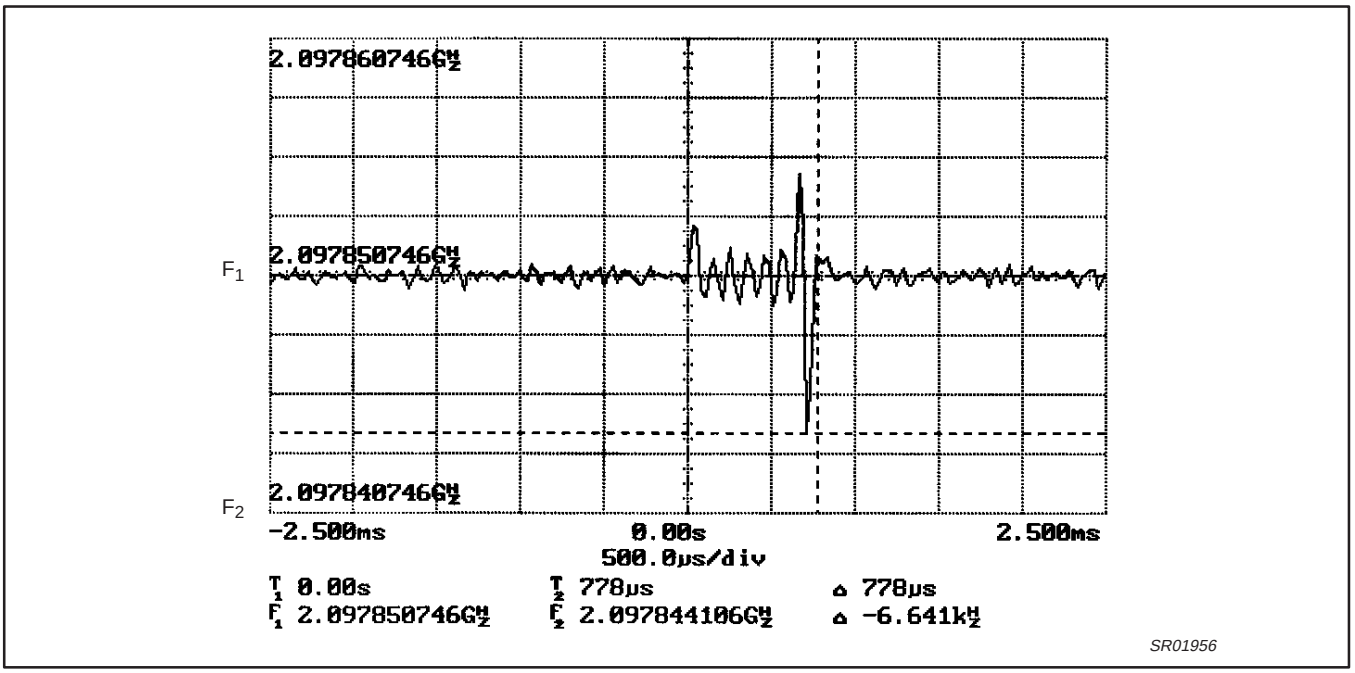


Figure 49. Strobe pulse width = 900 µs in software (WINSYNTH); frequency pull = 6.6 kHz

3.4.9. Auxiliary phase noise

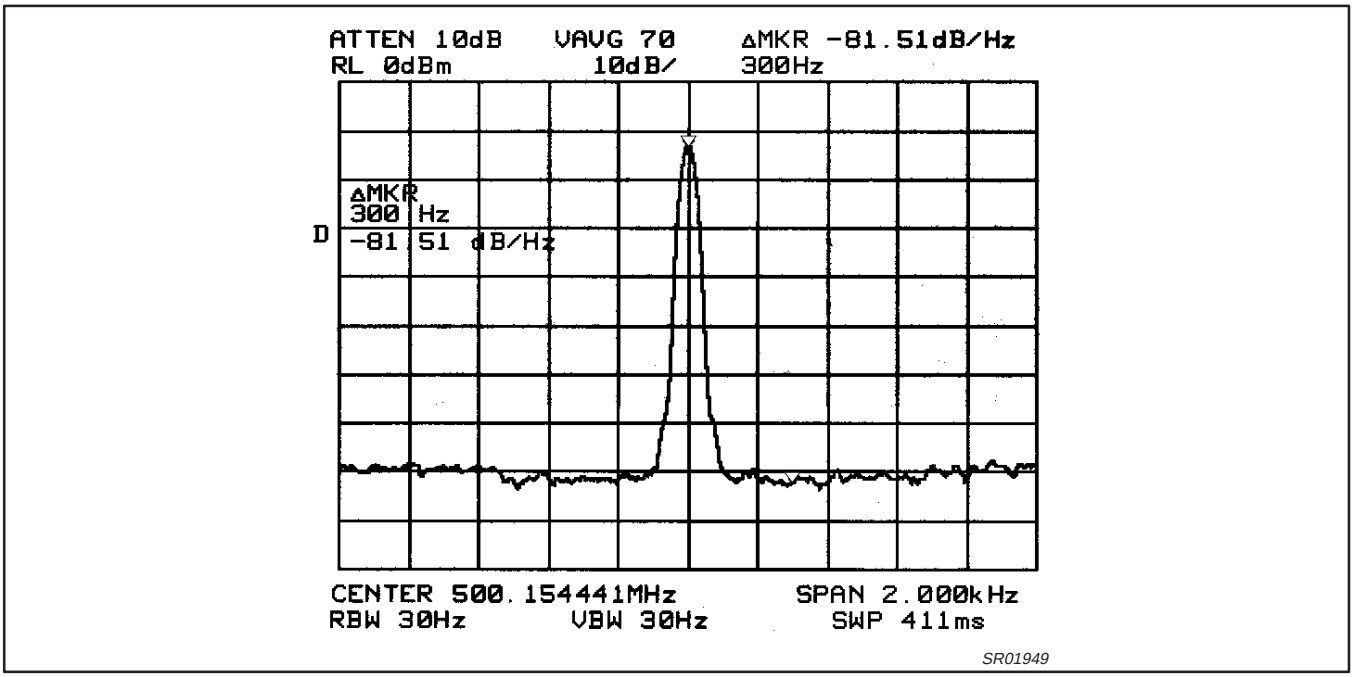


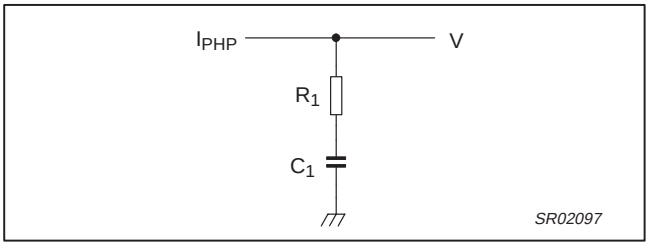
Figure 50. AUX phase noise (@ 1 kHz offset = –81.51 dBc/Hz)

3.5. Adaptive mode

To take advantage of having two charge pumps, designers can implement the loop filter in adaptive mode where two different loop responses are realized. When the synthesizer switches from channel to channel, a wider loop bandwidth is desired. Once the synthesizer is locked to the correct frequency, a narrow filter bandwidth is required for lower noise performance. This mode can be implemented by connecting the PHI charge pump to the integrating capacitor C_1, controlling the width of the STROBE (amount of time in speedup), and selecting CP0,1 in Table 2.

Derivation for Conventional Filter with 1 charge pump

Assuming there is no spurs attenuation pole,



$$V = I_{PHP}R_1 + \frac{I_{PHP}}{sC_1}$$

$$= I_{PHP}\left(\frac{sR_1C_1 + 1}{sC_1}\right)$$

Since the charge pumps are in speedup mode, $I_{PHP} = X \cdot I_{NORMAL}$, where X is the current factor set by CP in Table 2.

Then,

$$V = X \cdot I_{NORMAL}\left(\frac{sR_1C_1 + 1}{sC_1}\right)$$

Thus, the transfer function becomes:

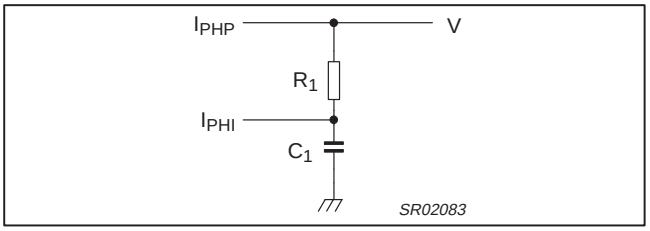
$$F_N(s) = \frac{V}{I_{NORMAL}} = X\left(\frac{sR_1C_1 + 1}{sC_1}\right)$$

$$\text{Pole} = 0\text{Hz} \qquad \text{Zero} = \frac{1}{2\pi R_1C_1}$$

$$\text{Gain} = X$$

Derivation for Adaptive Filter with 2 charge pumps

Assuming there is no spurs attenuation pole,



$$V = \left(R_1 + \frac{1}{sC_1}\right)I_{PHP} + \frac{1}{sC_1}I_{PHI}$$

$$= \left(\frac{sR_1C_1 + 1}{sC_1}\right)I_{PHP} + \frac{I_{PHI}}{sC_1}$$

Since the charge pumps are in speedup mode,

$$I_{PHP} = X \cdot I_{NORMAL} \qquad \text{and} \qquad I_{PHI} = Y \cdot I_{NORMAL}$$

where X and Y are the current factors set by CP in Table 2.

Then,

$$V = \frac{(sR_1C_1 + 1)X \cdot I_{NORMAL} + Y \cdot I_{NORMAL}}{sC_1}$$

Thus, the transfer function becomes:

$$F_A(s) = \frac{V}{I_{NORMAL}} = \frac{(sR_1C_1 + 1)X + Y}{sC_1}$$

$$= \frac{sR_1C_1X + (X + Y)}{sC_1}$$

$$= \frac{(X + Y)\left(\frac{sR_1C_1X}{X+Y} + 1\right)}{sC_1}$$

$$\text{Pole} = 0\text{Hz} \qquad \text{Zero} = \frac{X + Y}{2\pi R_1C_1 \cdot X} \qquad \text{Gain} = X + Y$$

The gain is increased by a factor of X+Y and the zero is shifted by (X+Y)/X

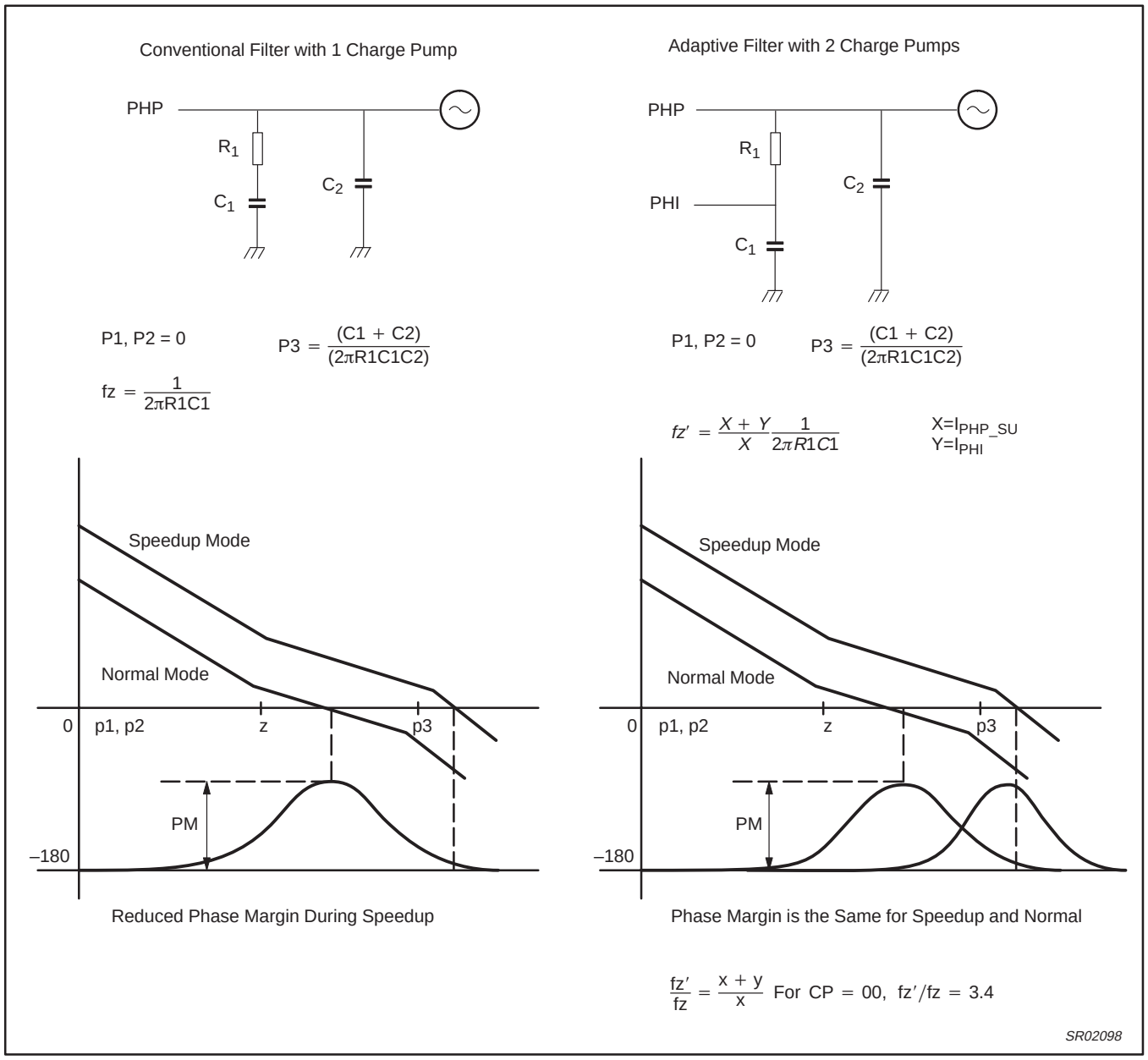


Figure 51. Filter response for different modes

4. PERFORMANCE OF THE SA8026 IN DIFFERENT APPLICATIONS

4.1. IS-136

Table 6. Measurement results for IS-136 Application
NP = Not Populated

Parameters	**IS-136 Application**		
Loop Components		C_1 = 10 nF C_2 = 1 nF C_3 = NP	R_1 = 9.1 kΩ R_2 = NP
VCO Murata	VCO Gain K_{VCO} VCO Frequency f_{VCO} Frequency Range	40 MHz/V 2098 MHz 2058 – 2138 MHz	
Channel Spacing		30 kHz	
Comparison Frequency		240 kHz FMOD = 8	
Reference Frequency: VCTCXO KSS		19.44 MHz	
Charge Pump	Current Gain I_{CP} R_{SET} CP0, CP1	492 µA/cycle 7.5 kΩ CP0 = 0, CP = 0	
Results			
Loop Bandwidth		5 kHz	
Close-in Phase Noise @ 1 kHz		–74.2 dBc/Hz	
Integrated Phase Jitter; 10 Hz – 100 kHz Residual FM; CCITT Filter	2100 MHz	2.9 mrad rms 30 Hz rms	
Fractional Spurs		–64 dBc	
Comparison Spurs		–71 dBc	
Switching Time to within 1 kHz	2078 to 2108 MHz	744 µs	

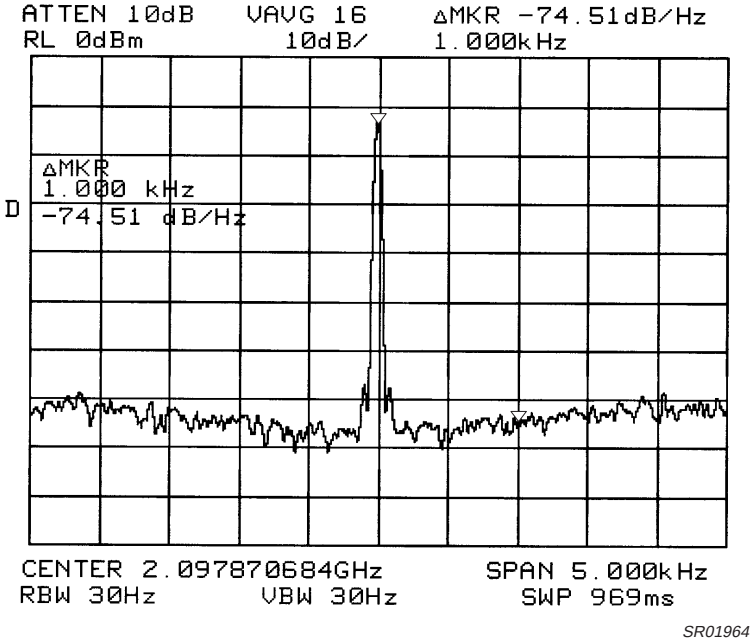


Figure 52. IS-136 phase noise

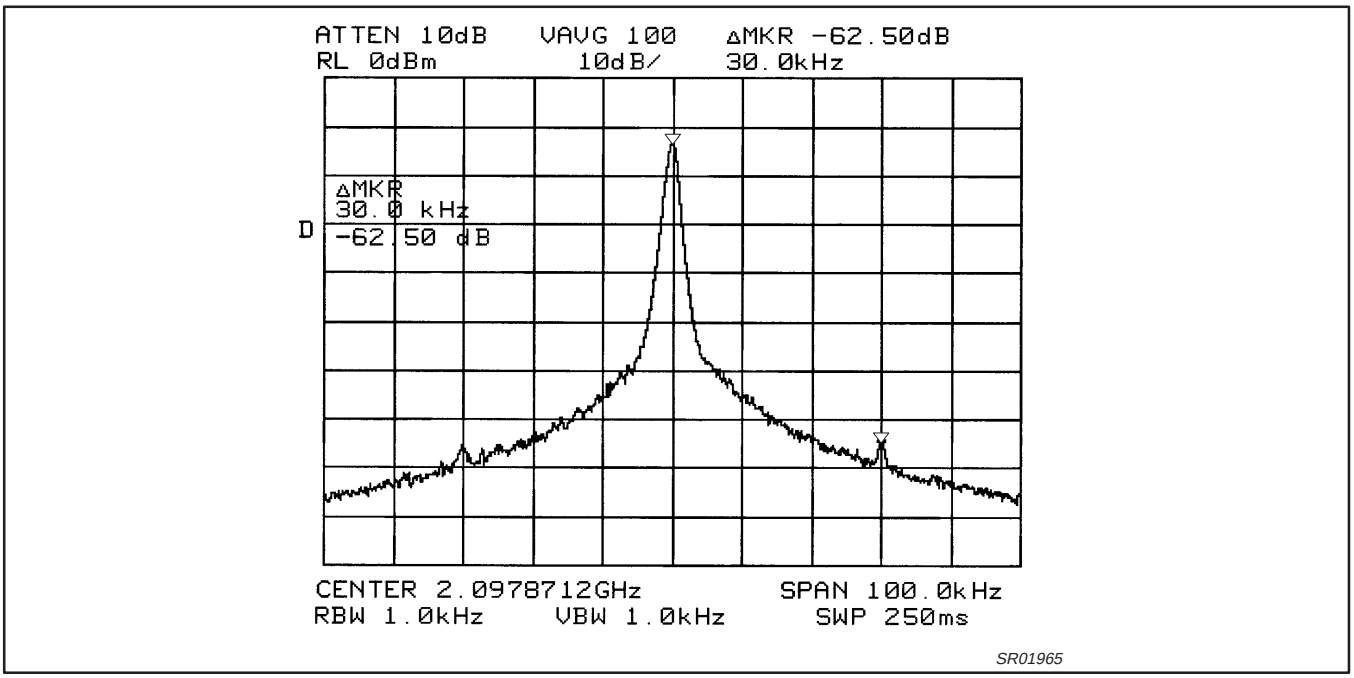


Figure 53. IS-136 fractional spur

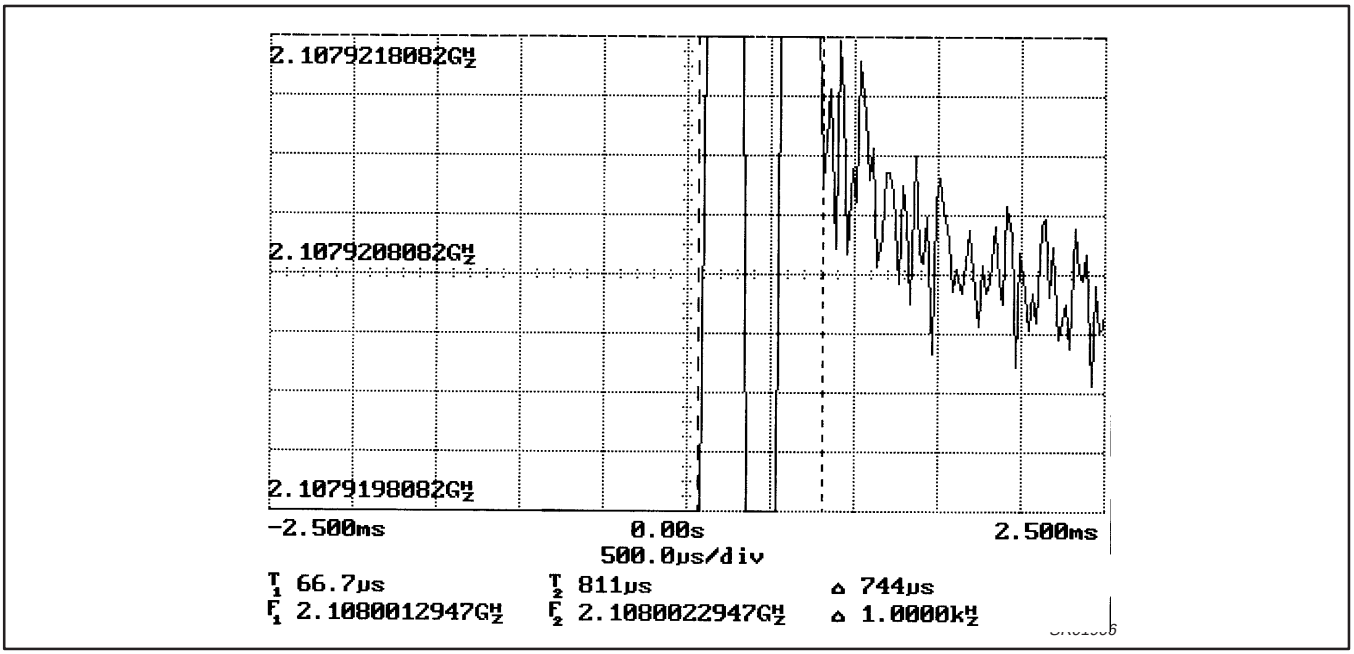


Figure 54. IS-136 switching time

4.2. DCS1800

Table 7. Measurement results for DCS1800
NP = Not Populated

Parameters	**DCS1800 Application**		
Loop Components		C_1 = 15 nF C_2 = 1.5 nF C_3 = 560 pF	R_1 = 3.6 kΩ R_2 = 7.5 kΩ
VCO Murata	VCO Gain K_{VCO} VCO Frequency f_{VCO} Frequency Range	40 MHz/V 2098 MHz 2058 – 2138 MHz	
Channel Spacing		200 kHz	
Comparison Frequency		1000 kHz FMOD = 5	
Reference Frequency: VCTCXO KSS		13 MHz	
Charge Pump	Current Gain I_{CP} R_{SET} CP0, CP1	492 µA/cycle 7.5 kΩ CP0 = 0, CP = 0	
Results			
Loop Bandwidth		8 kHz	
Close-in Phase Noise @ 1 kHz		–81 dBc/Hz	
Integrated Phase Jitter; 10 Hz – 100 kHz @ 2100 MHz		20.6 mrad rms	
Fractional Spurs		–76 dBc	
Comparison Spurs		–80 dBc	
Switching Time to within 1 kHz	2078 to 2108 MHz	467 µs	

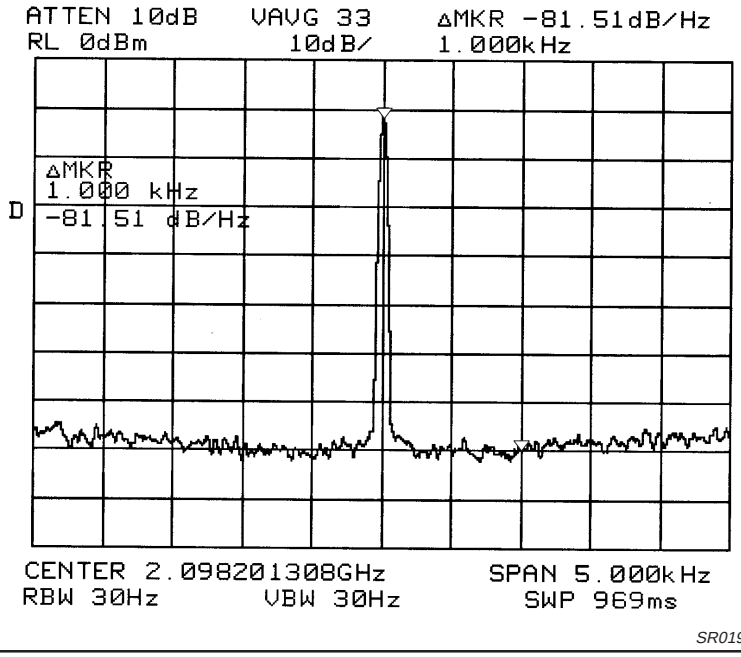


Figure 55. DCS1800 phase noise

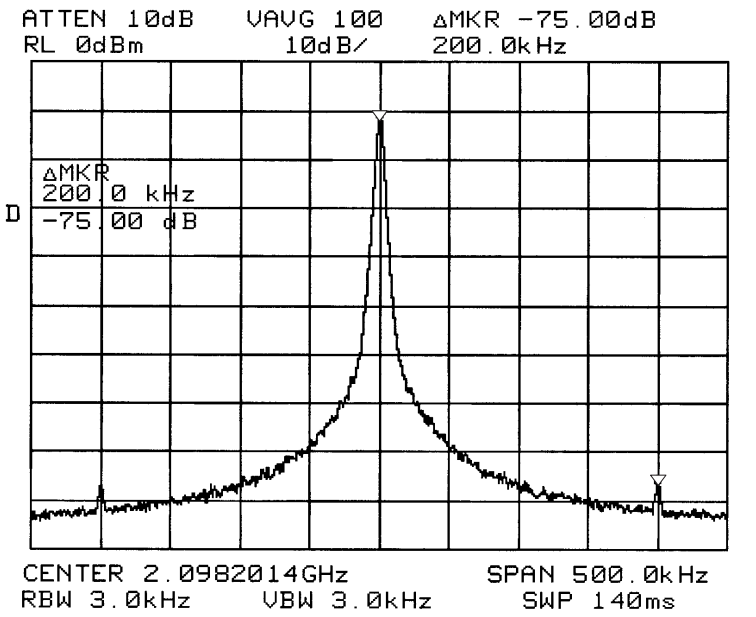


Figure 56. DCS1800 fractional spur

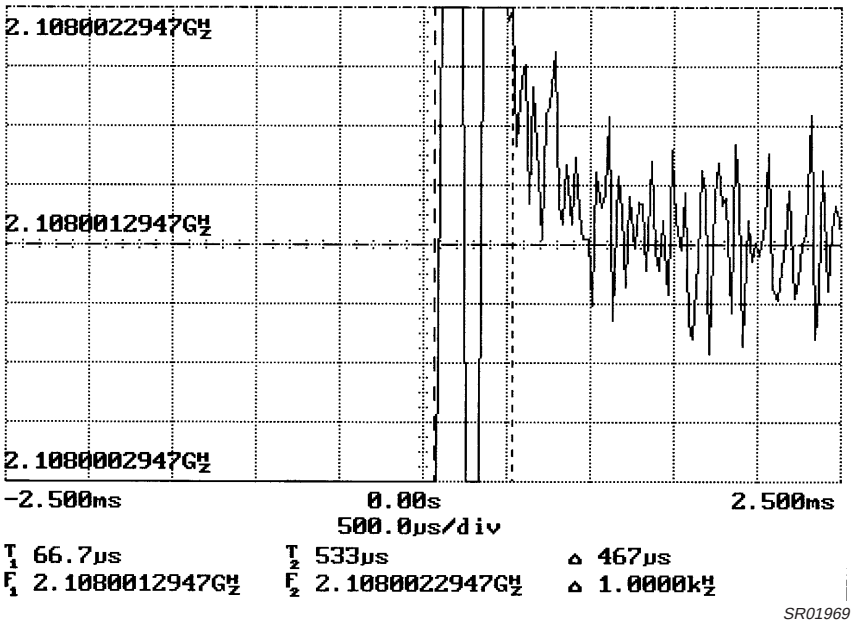


Figure 57. DCS1800 switching time

4.3. PHS

Table 8. Measurement results for PHS Application
NP = Not Populated

Parameters	**PHS Application**		
Loop Components		C_1 = 10 nF C_2 = 1 nF C_3 = NP	R_1 = 4.3 kΩ R_2 = NP
VCO Murata	VCO Gain K_{VCO} VCO Frequency f_{VCO} Frequency Range	18 MHz/V 1662 MHz 1651 – 1674 MHz	
Channel Spacing		300 kHz	
Comparison Frequency		2400 kHz FMOD = 8	
Reference Frequency: VCTCXO KSS		19.2 MHz	
Charge Pump	Current Gain I_{CP} R_{SET} CP0, CP1	492 µA/cycle 7.5 kΩ CP0 = 0, CP = 0	
Results			
Loop Bandwidth		12 kHz	
Close-in Phase Noise @ 1 kHz		–83 dBc/Hz	
Integrated Phase Jitter; 10 Hz – 100 kHz @ 1.663 GHz		13.2 mrad rms	
Fractional Spurs		–76 dBc	
Comparison Spurs		–80 dBc	
Switching Time to within 1 kHz	1649 to 1677 MHz	344 µs	

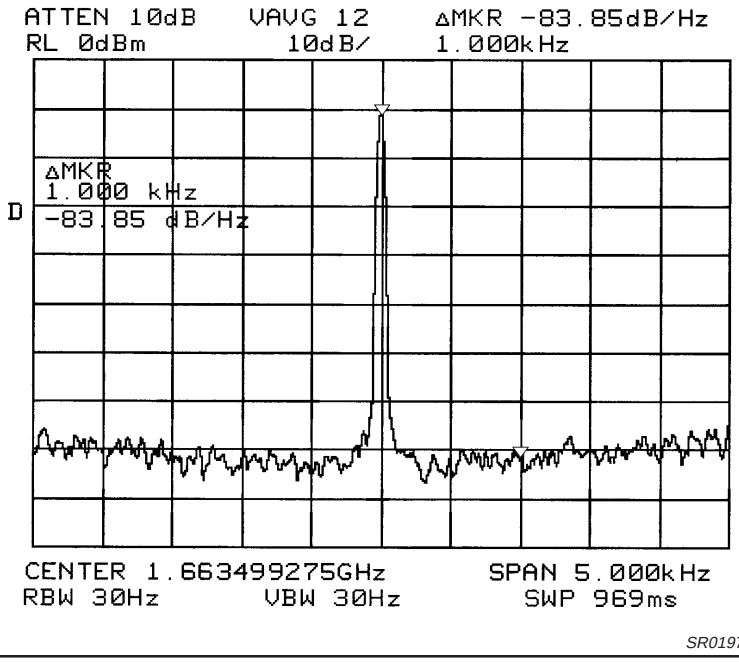


Figure 58. PHS phase noise

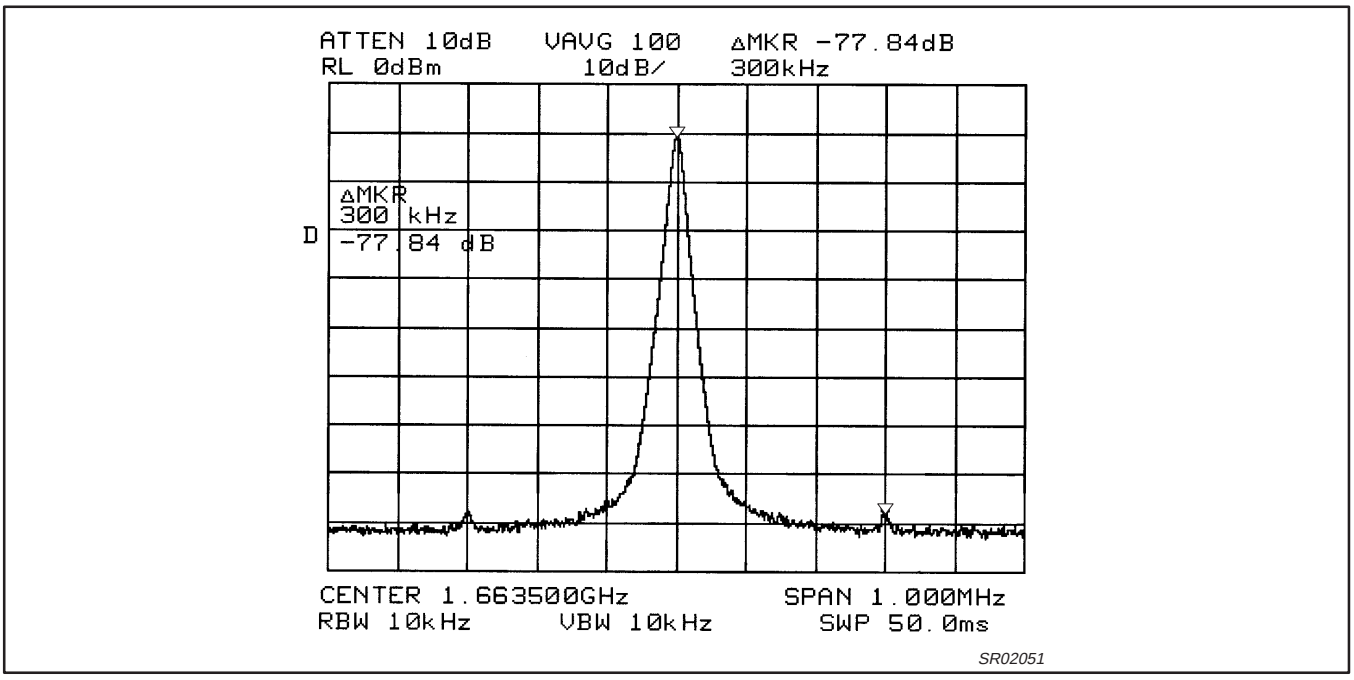


Figure 59. PHS fractional spur

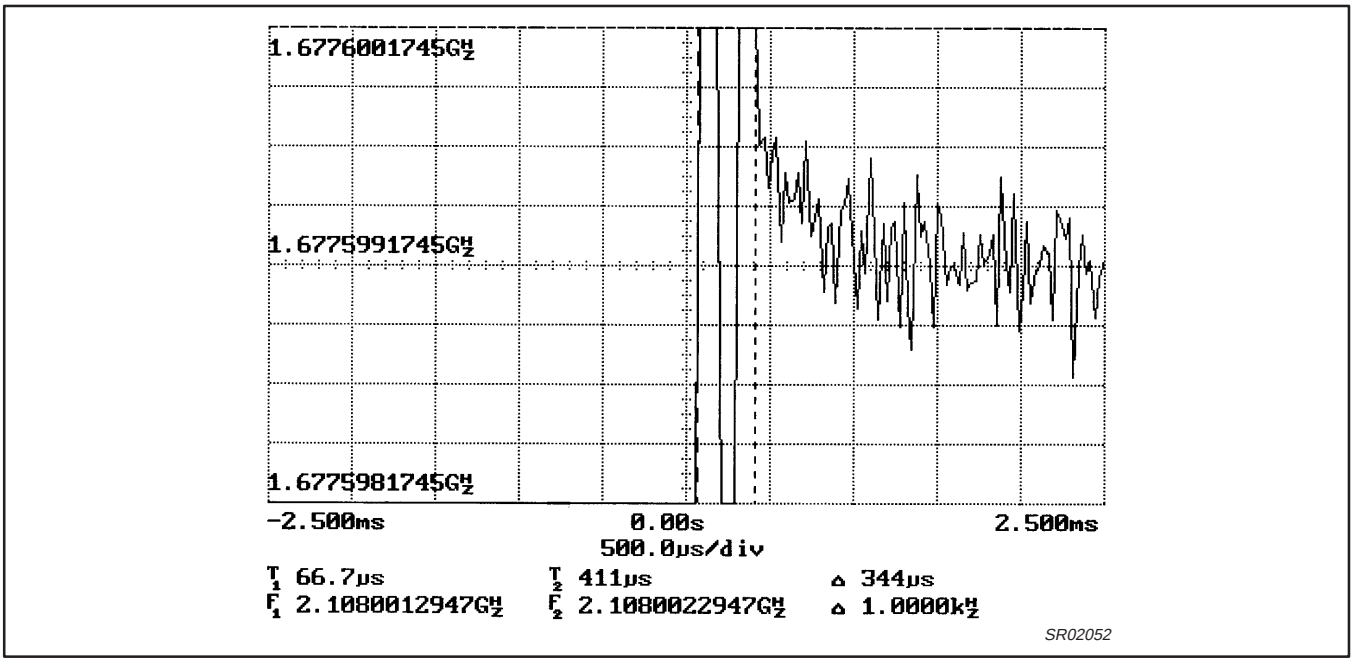


Figure 60. PHS switching time

4.4. PCS IS-95

Table 9. Measurement results for PCS CDMA

Parameters	**PCS IS-95 Application**		
Loop Components (NP = Not Populated)		C_1 = 47 nF C_2 = 4.7 nF C_3 = NP	R_1 = 12 kΩ R_2 = NP
VCO Murata	VCO Gain K_{VCO} VCO Frequency f_{VCO} Frequency Range	15 MHz/V 1780 MHz 1705 – 1795 MHz	
Channel Spacing [1]		10 kHz	
Comparison Frequency		80 kHz FMOD = 8	
Reference Frequency: VCTCXO KSS		19.2 MHz	
Charge Pump	Current Gain I_{CP} R_{SET} CP0, CP1	492 µA/cycle 7.5 kΩ CP0 = 0, CP = 0	
Results			
Loop Bandwidth		830 Hz	
Close-in Phase Noise @ 1 kHz		–60 dBc/Hz	
Integrated Phase Noise; 10 Hz – 100 kHz Residual FM; CCITT Filter	1780 MHz	56 mrad rms 62 Hz rms	
Fractional Spurs @ 10 kHz		–61 dBc	
Comparison Spurs @ 80 kHz		–80 dBc	
Switching Time to within 1 kHz	1760 to 1790 MHz	5.24 ms	

NOTE:

1. Because CDMA channel spacing is 1.25 MHz and AMPS is 30 kHz, the common channel spacing between the two for this design is 10 kHz.

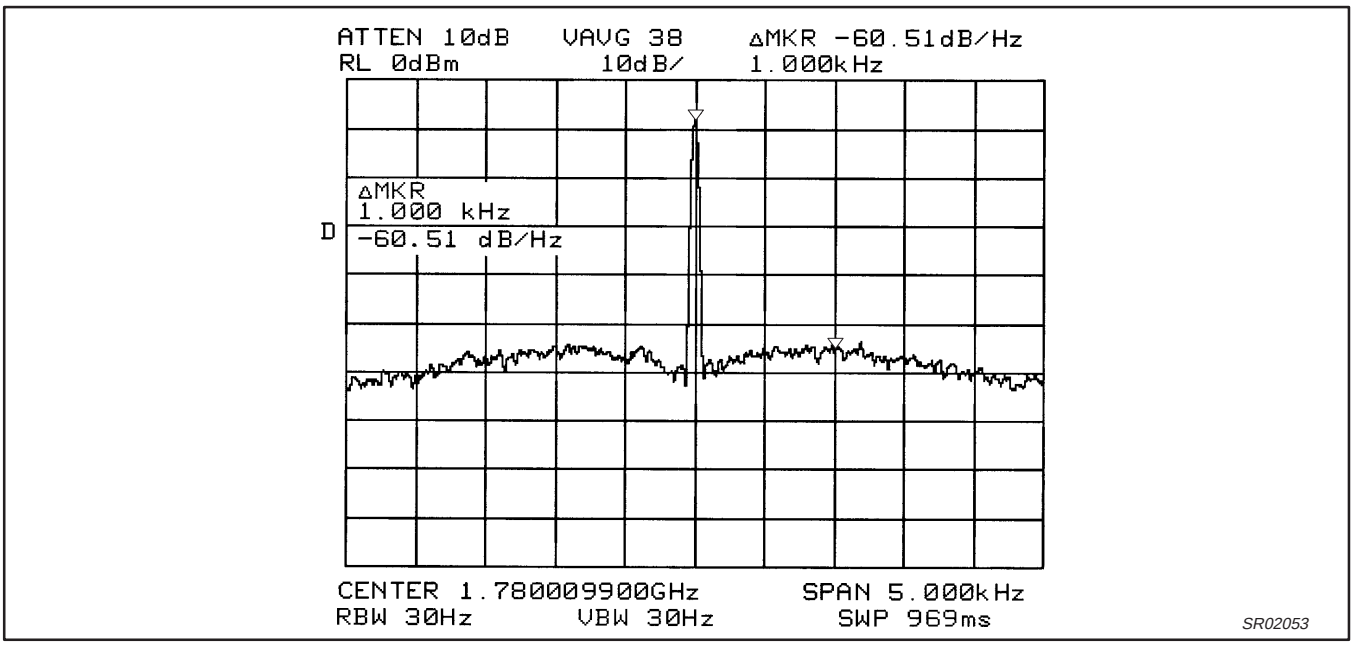


Figure 61. IS-95 phase noise

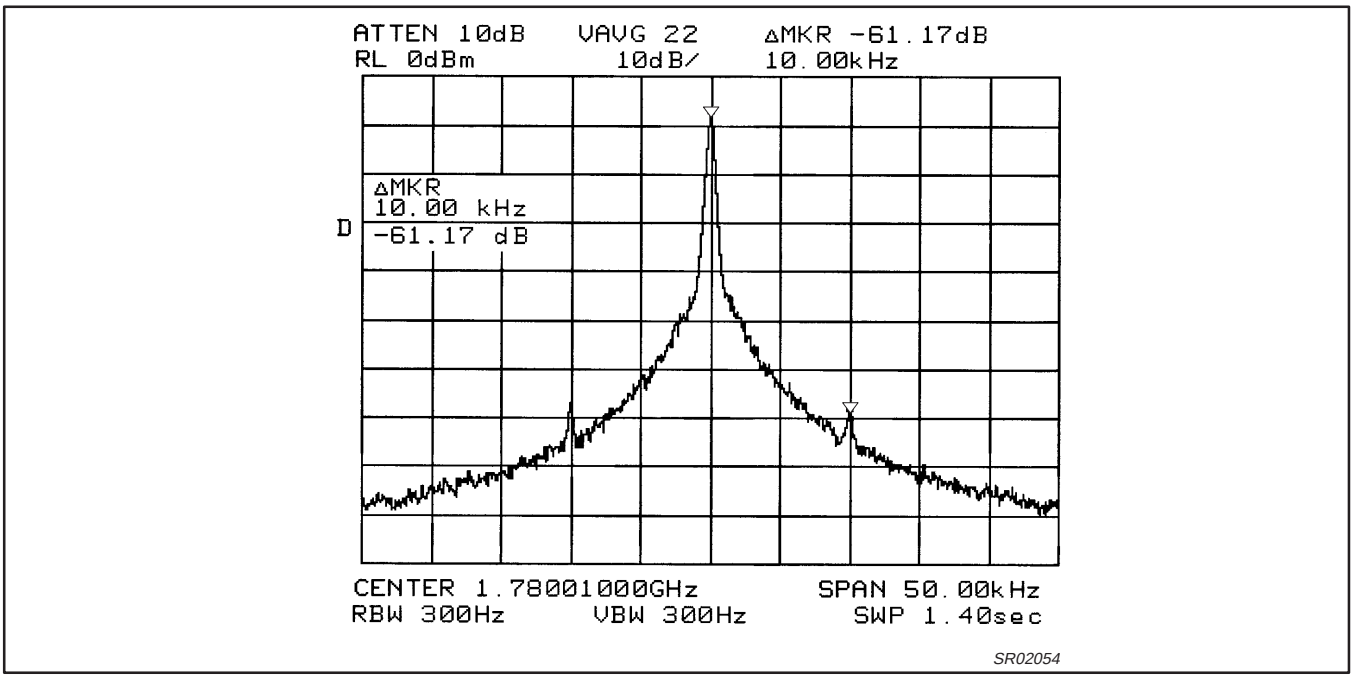


Figure 62. IS-95 fractional spur

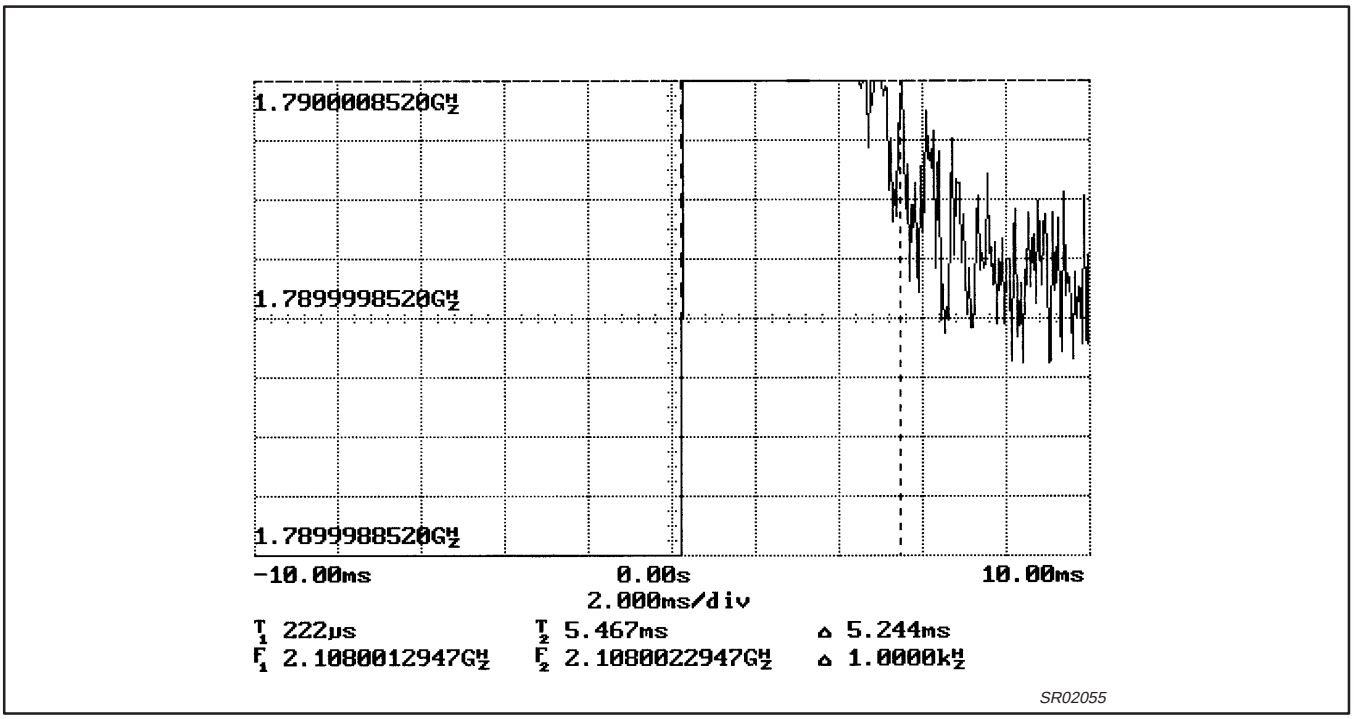


Figure 63. IS-95 switching time

5. FREQUENTLY ASKED QUESTIONS

Q: How much improvement in phase noise performance of the SA8026 compared to the SA8025?

A: It is around 6 dB better @ 1.7 GHz.

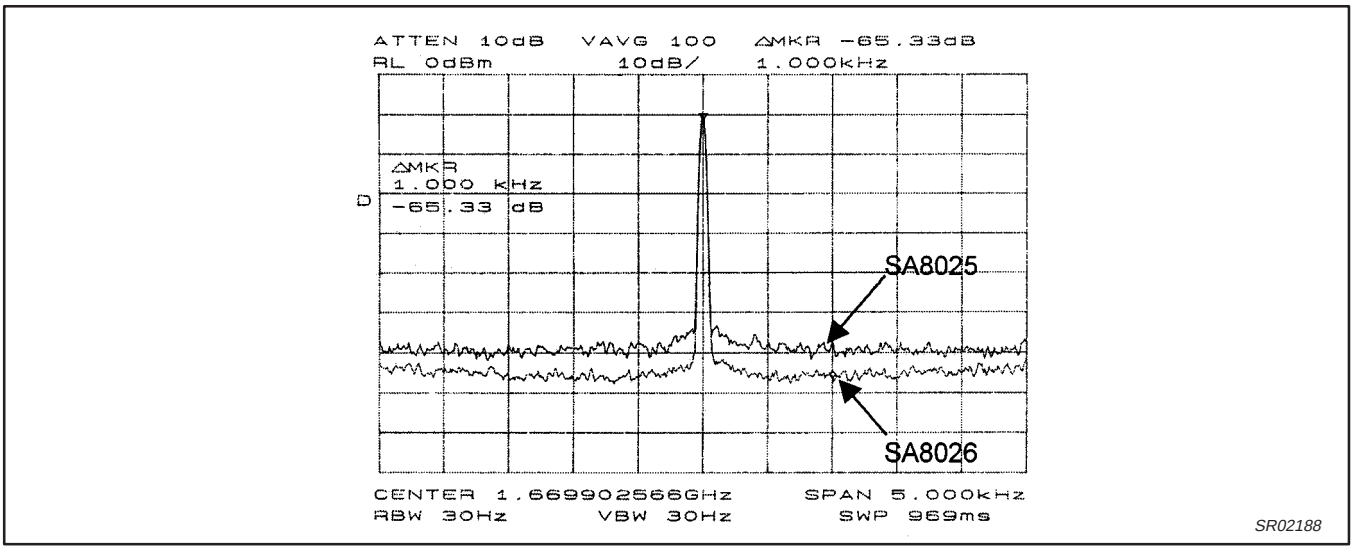


Figure 64. Phase noise comparison between SA8026 and SA8025

Q: The device latched up and I could not program it. What do I do now?

A: The device may have inadvertently entered the test mode. This test mode is only used at the plant to verify certain design parameters. The remedy for this problem is to reset the device by programming WORD E per data sheet.

Q: What should I do with unused inputs?

A: Unused inputs, such as RF_{in-}, should be AC ground.

Q: Bypass capacitors are recommended for all current setting resistors for SA025 to improve noise performance, is it the same for SA8026?

A: No. Unlike SA8025, SA8026 only has one current setting resistor and no bypass capacitor is needed. Using a bypass capacitor may cause the device to oscillate because of the internal circuit.

Q: Will fractional compensation vary from device to device?

A: Yes. However, we guarantee a 15 dB compensation.

6. APPENDIX A

6.1. Loop filter design

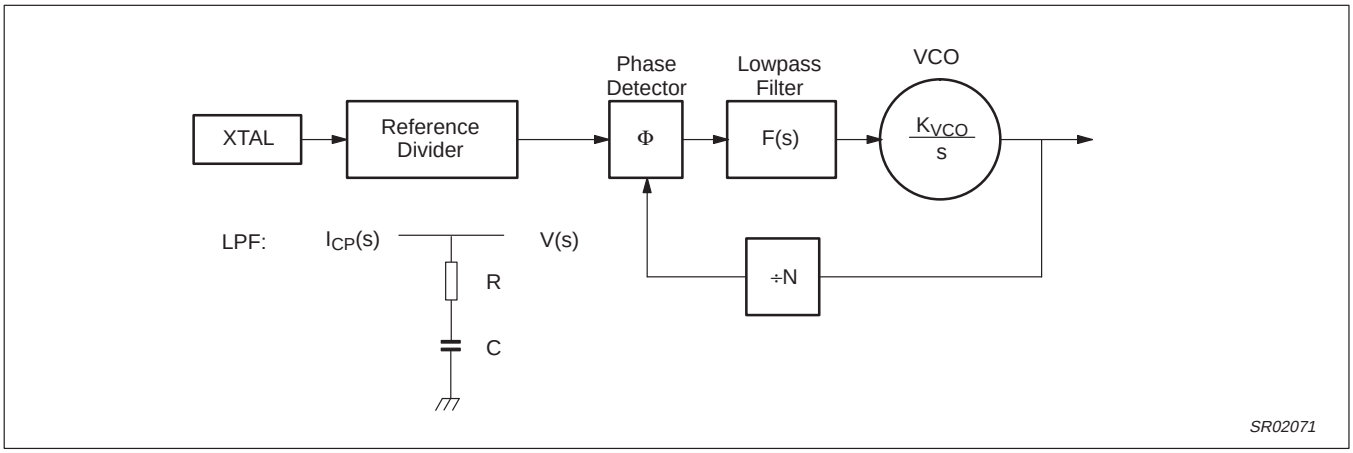


Figure 65. Loop filter block diagram

Derivation of 2nd order PLL formula used in this application note

$$F(s) = \frac{V(s)}{I_{CP}(s)} = \frac{sRC + 1}{sC} \quad (20)$$

From the block diagram, the open loop response of the system becomes:

$$G(s)H(s) = \frac{K_\Phi \cdot K_{VCO}}{Ns}\left(\frac{sRC + 1}{sC}\right) \quad (21)$$

To find the characteristics equation, equate 1+G(s)H(s) to 0.

$$1 + \frac{K_\Phi \cdot K_{VCO}(sRC + 1)}{s^2NC} = 0 \quad (22)$$

$$\Rightarrow \quad s^2 + \frac{K_\Phi \cdot K_{VCO} \cdot R}{N}s + \frac{K_\Phi \cdot K_{VCO}}{NC}$$

Comparing with the standard 2nd order characteristics equation ($s^2 + 2\zeta\omega_N s + \omega_N{}^2$)

$$\omega_N{}^2 = \frac{K_\Phi \cdot K_{VCO}}{NC} \quad \Rightarrow \quad C = \frac{K_\Phi \cdot K_{VCO}}{N\omega_N{}^2} \quad (23)$$

$$2\zeta\omega_N{}^2 = \frac{K_\Phi \cdot K_{VCO} \cdot R}{N} \quad \Rightarrow \quad R = 2 \cdot \zeta\sqrt{\frac{N}{K_\Phi \cdot K_{VCO} \cdot N}} \quad (24)$$

To find ω_N, use the envelope of the decaying unit step response of the second order system (0<ζ<1)

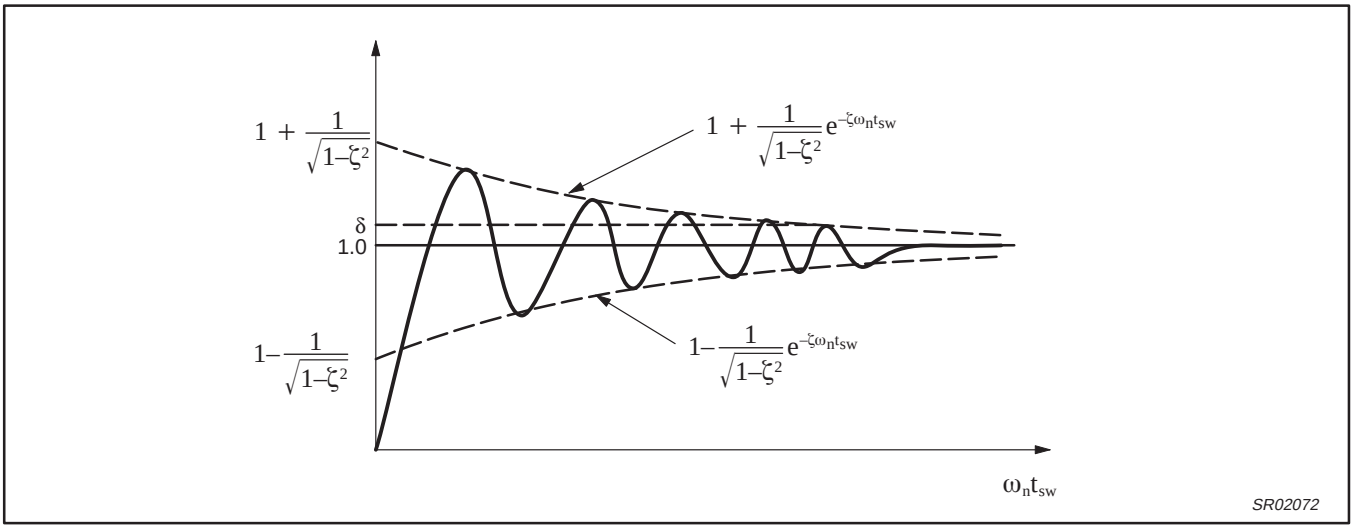


Figure 66. Envelope of decay unit step response of the second order system

Assuming δ is the resolution desired at lock time, we let the envelope shown above equal to this resolution

$$1 + \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t_{SW}} = 1 \cdot \delta \quad (25)$$

Solving for $\omega_n t_{SW}$, we have:

$$\omega_n t_{SW} = -\frac{1}{\zeta} 1n\left(\delta \cdot \sqrt{1-\zeta^2}\right) \quad (26)$$

$$\Longrightarrow \quad \omega_n = -\frac{1n\left(\delta \cdot \sqrt{1-\zeta^2}\right)}{\zeta \cdot t_{SW}} \quad (27)$$

7. REFERENCES

[1] SA8026 Data Sheet, Philips Semiconductors, 1998

[2] “Digital PLL Frequency Synthesizer”, Ulrich Rohde, Prentice Hall 1983

[3] “Automatic Control Systems”, Benjamin Kuo, Prentice Hall 1991

[4] “SA8025 Fractional-N Synthesizer for 2 GHz Band Application”, Philips Application Note AN1891

[5] “UMA1021M Low Voltage Frequency Synthesizer”, Philips Application Note AN96083

8. SA8026 DEMO BOARD

8.1. Setup instructions

8.1.1. Demo board setup

1. Connect the interface cable from the demo board to the interface card
2. Plug the interface card to the parallel port
3. Supply the demo board with 7 VDC
4. Switches are used to select regulated supply or external supply voltage
5. Tweak VR3 for appropriate VDDA (default is set for 3.7 VDC on the demo board)
6. Tweak VR1 for V_{DD} if V_{DD} is different from VDDA
7. Connect MAIN-OUT or AUX-OUT to spectrum analyzer
8. Run WINSYNTH.EXE to program the device

Optional Aux:

There are provisions for an optional SA602 on the board for designers that wish to check an Auxiliary frequency other than that VCO module.

Supply Voltage:	
Main VCO:	3.0 VDC
AUX VCO:	4.7 VDC
TCXO:	3.0 VDC

8.1.2. Synthesizer phase noise setup

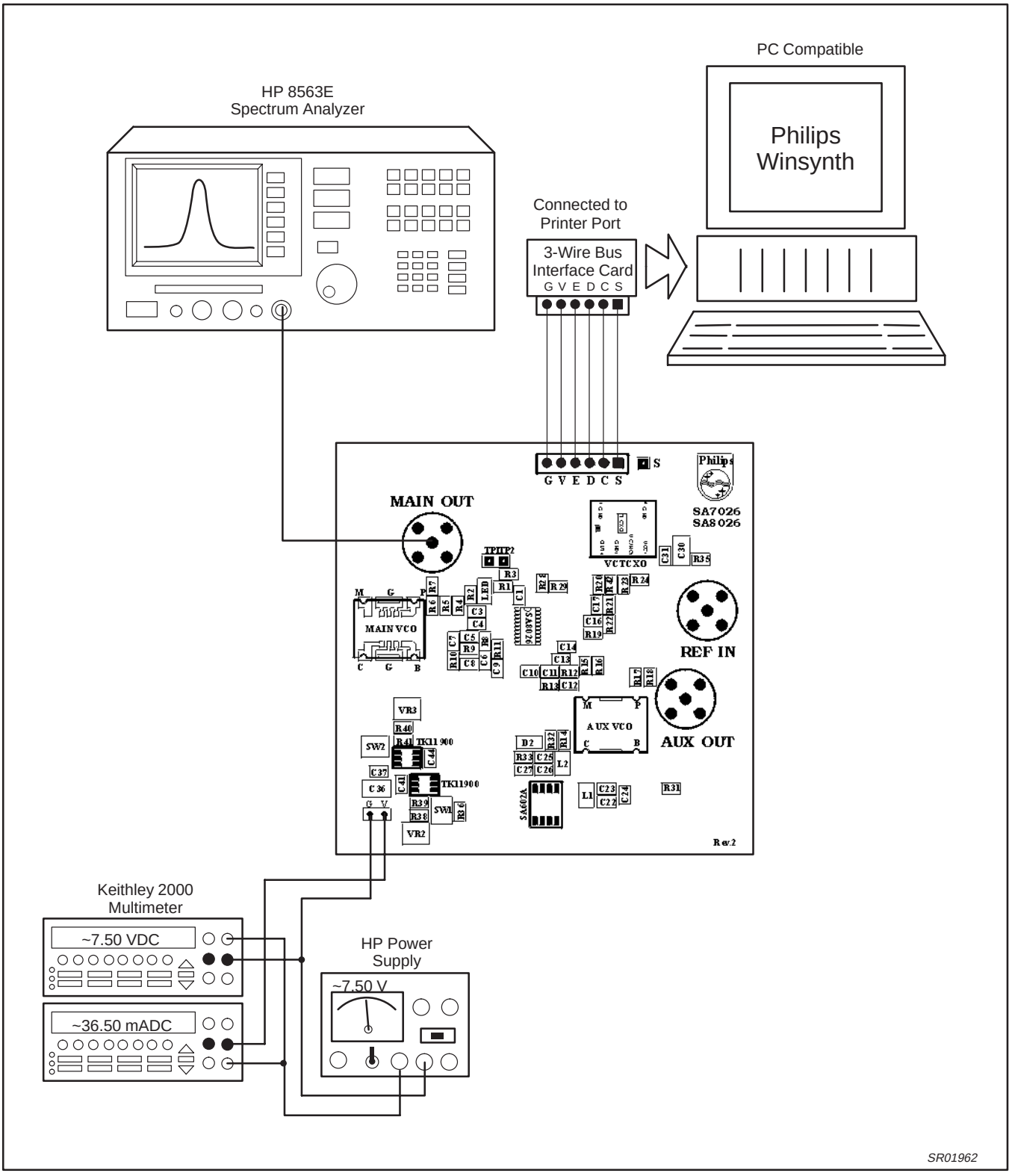


Figure 67. Synthesizer phase noise setup

8.1.3. Synthesizer switching time setup

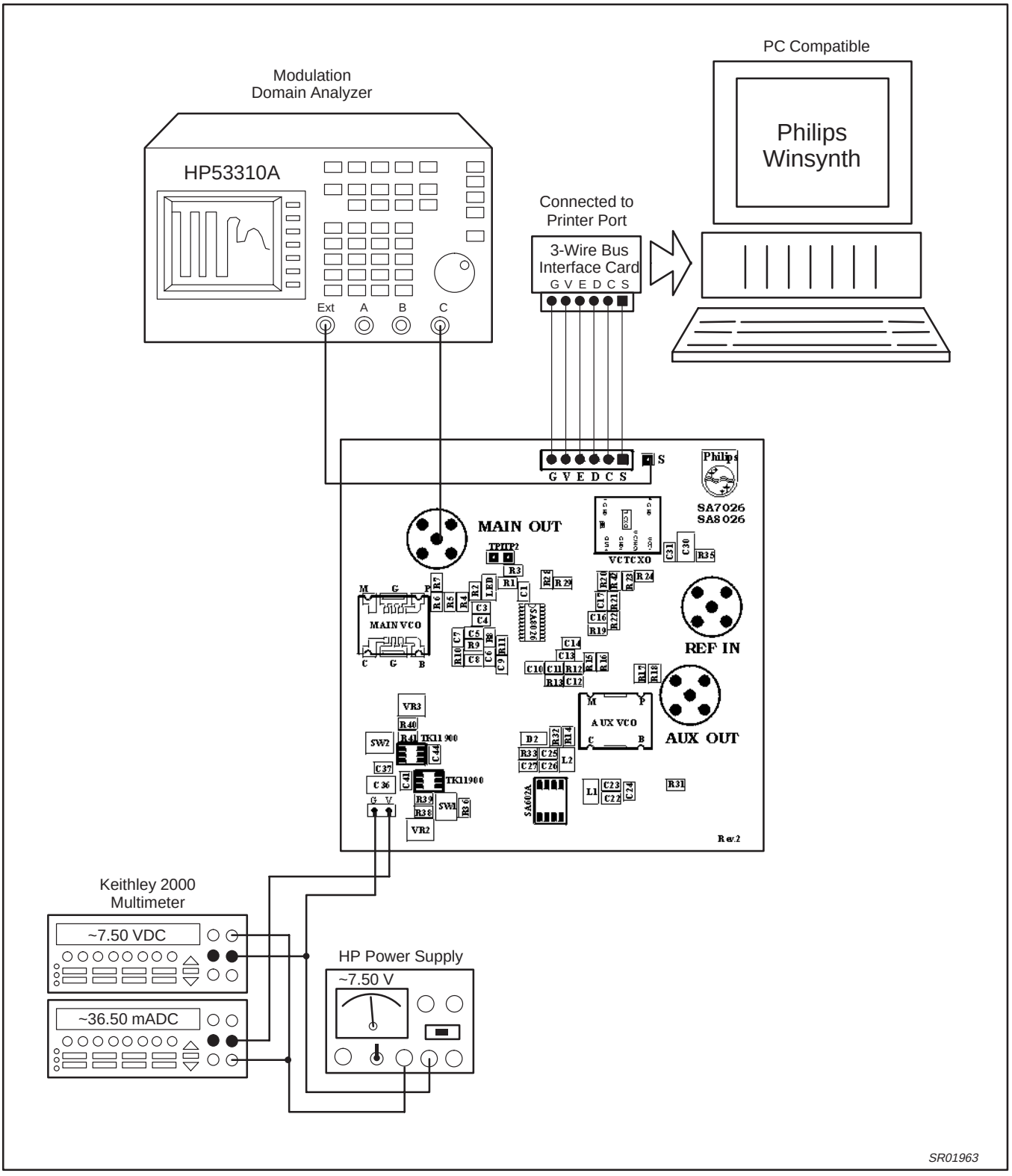


Figure 68. Synthesizer switching time setup

8.2. SA8026 demo board schematic

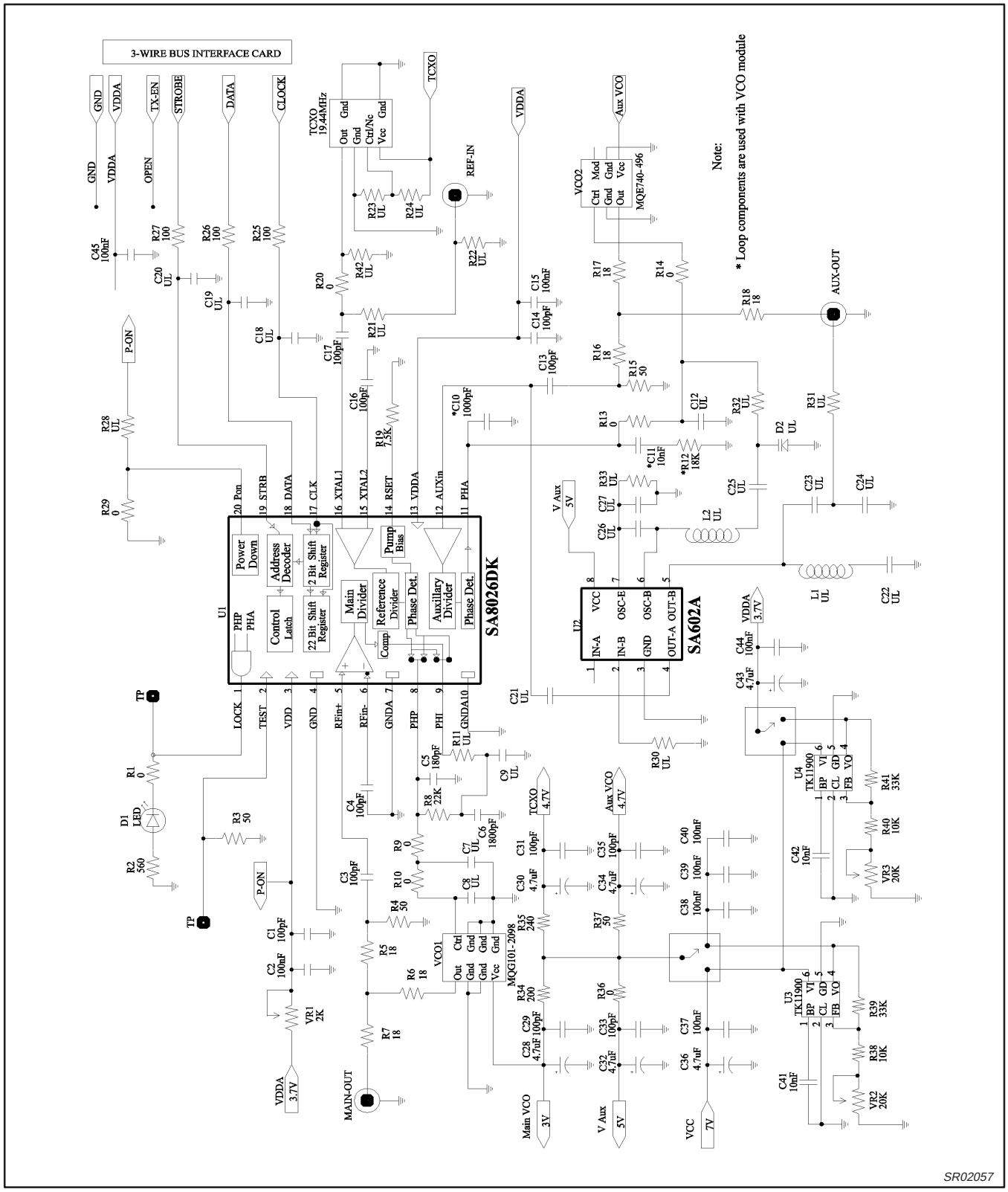


Figure 69. Demo board schematic

8.3. SA7026/8026 demo board layout

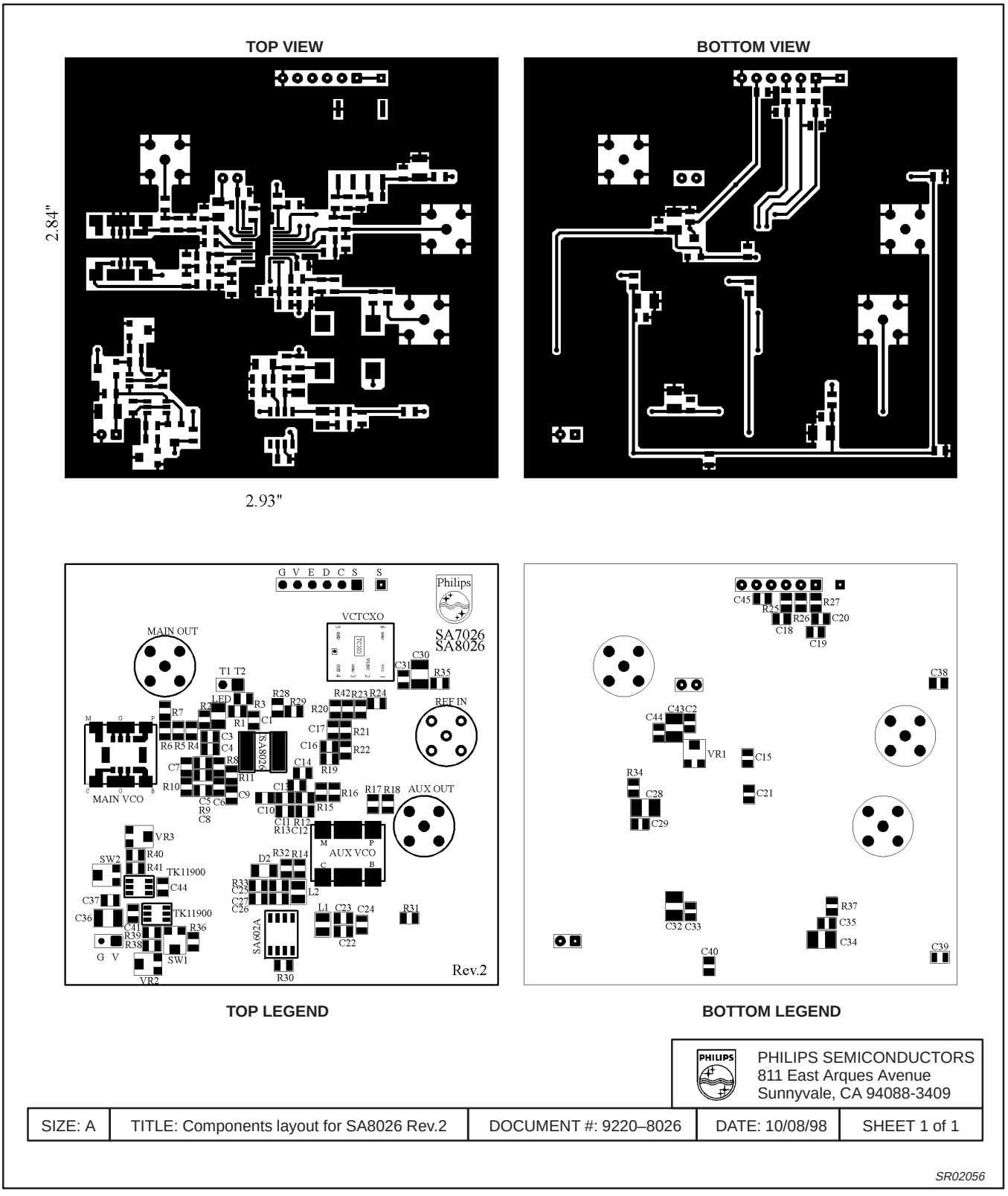


Figure 70. SA7026/8026 Demo board layout

8.4. SA8026 Bill of materials

Table 10. Application components list for SA8026 demo board

Qty	Volt	Value	Part Reference	Part Description	Vendor	Mfr	Part Number
Surface Mount Capacitor							
12	50 V	100 pF	C1, 3, 4, 5, 13, 14, 16 C17, 29, 31, 33, 35	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG101J9BB0
1	50 V	180 pF	C5	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG181J9BB0
1	50 V	1000 pF	C10	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG102J9BB0
1	50 V	1800 pF	C6	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG182J9BB0
3	50 V	0.01 μF	C11, C41, C42	CAP CER 0805 X7R ±10%	Garrett	Philips	08052R103K9BB0
8	50 V	0.1 μF	C2, 15, 37, 38, 39, 40, 44, 45	CAP CER 0805 Z5U ±20%	Garrett	Philips	08052E104M9BB0
6	16 V	4.7 μF	C28, 30, 32, 34, 36, 43	TANTALUM CHIP CAP	Garrett	Matsuo	267M 1602 475K 533
14		UL	C7, 8, 9, 12, 18, 19, 20, 21 C22, 23, 24, 25, 26, 27				
Surface Mount Resistor							
10	50 V	0 Ω	R1, 9, 10, 13, 14, 20, 29 R31, 32, 36	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A000-JK
6	50 V	18 Ω	R5, 6, 7, 16, 17, 18	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A180-JK
4	50 V	50 Ω	R3, 4, 15, 37	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A500-JK
3	50 V	100 Ω	R25, 26, 27	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A101-JK
1	50 V	200 Ω	R34	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A201-JK
1	50 V	240 Ω	R35	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A241-JK
1	50 V	560 Ω	R2	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A561-JK
4	50 V	10 kΩ	R30, 33, 38, 40	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A103-JK
1	50 V	12 kΩ	R19	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A123-JK
1	50 V	18 kΩ	R12	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A183-JK
1	50 V	22 kΩ	R8	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A223-JK
2	50 V	33 kΩ	R39, R41	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A333-JK
7		UL	R11, 21, 22, 23, 24, 28, 42				
Surface Mount Inductor							
1	50 V	UL	L1	Surface Mount Inductor	Coilcraft	Coilcraft	1008HS-181TKBC
1	50 V	UL	L2	Surface Mount Inductor	Coilcraft	Coilcraft	1008HS-751TKBC
Surface Mount Resistor Trimmer							
1	50 V	2 k	VR1	3mm 1-Turn J-H Trimmer	Garrett	Tocos	G3A202M
2	50 V	20 k	VR2, VR3	3mm 1-Turn J-H Trimmer	Garrett	Tocos	G3A203M
Surface Mount Selector Switch							
2	50 V	Switch	SW1, SW2	3mm Selector Switch	Digikey	Bourns	7813J-1-023E
Surface Mount Temperature Control Crystal Oscillator							
1	3 V	19.44 MHz	TCXO	TCXO	KSS	KSS	TCXO-201C1-19.44
Surface Mount Voltage Control Oscillator							
1	5 V	496 MHz	VCO	Voltage Control Oscillator	Murata	Murata	MQE740-496
1	3 V	2098 MH z	VCO	Voltage Control Oscillator	Murata	Murata	MQG101-2098
Surface Mount LED							
1	50 V	LED	D1	Surface Mount LED	Digikey	Lumex	LU60205CT-ND
Surface Mount Diode							
1	50 V	UL	D2	Variable Capacitance Diode	Philips	Philips	BB215
Surface Mount Integrated Circuit							
1	5 V	SA8026	U1	2.5 GHz Fractional-N-Synthe.	Philips	Philips	SA8026
1	5 V	UL	U2	Dual Balance Mixer Oscillator	Philips	Philips	SA602A
2	25 V	TK11900	U3, U4	Adjustable Voltage Regulator	Tocos	Tocos	TK11900
Miscellaneous							
1				Printed Circuit Board	KML Vector	Philips	SA7026/SA8026
3		SMA	Main-out, Ref-in, Aux-out	SMA Straight Receptacle	DC Elect.	Connex	132134
1		Header		Single Row Header 36-Pins	Mouser	Waldom	538-22-03-2121

8.5. 3-wire bus card schematic

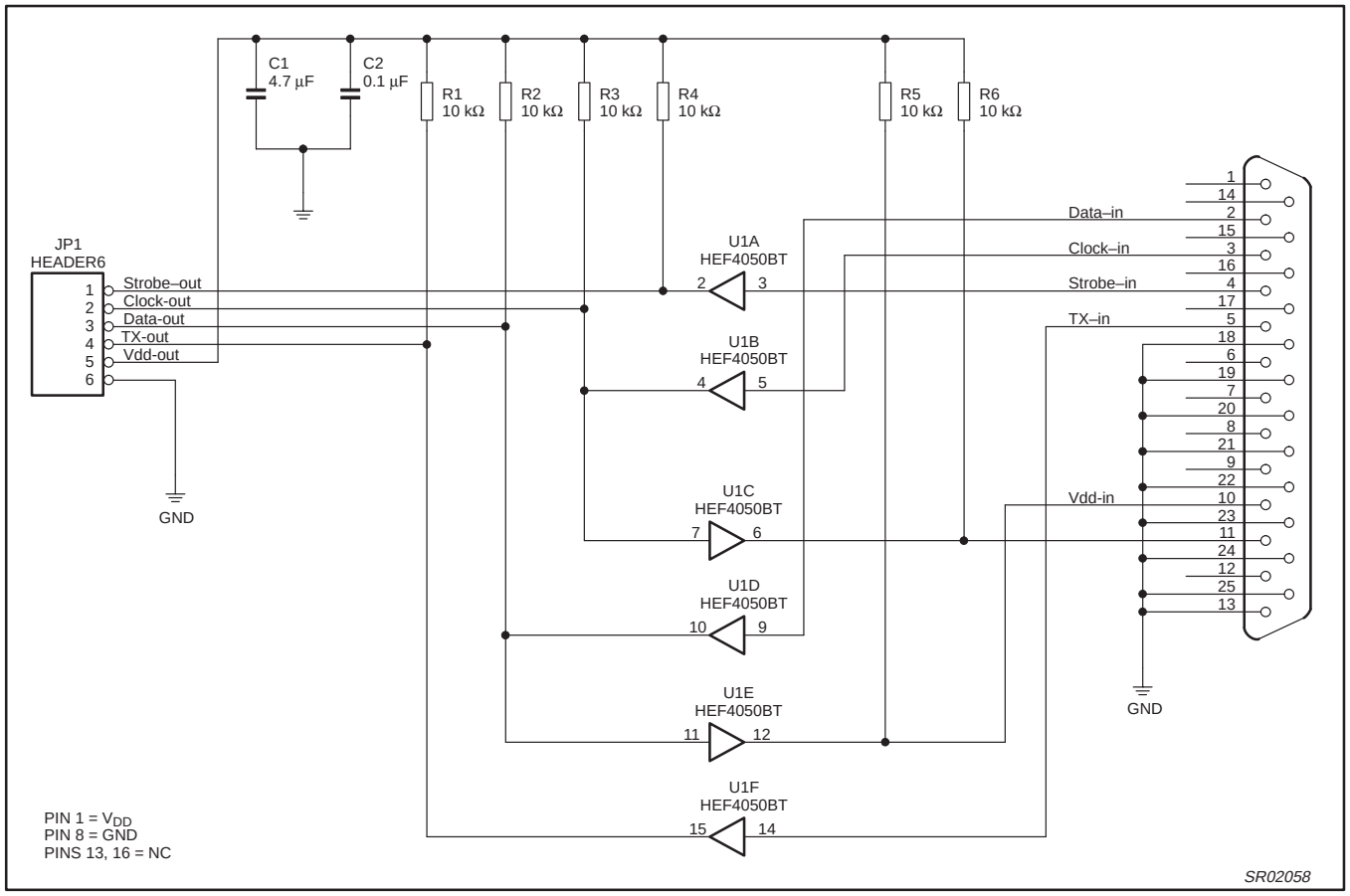


Figure 71. 3-wire bus card schematic

9. INTRODUCTION TO THE SA7026

9.1. Description

The SA7026 BiCMOS 1.3 GHz fractional-N dual synthesizer integrates programmable dividers, charge pumps and a phase comparator to implement two separate phase-locked-loop control functions, main and auxiliary, in one TSSOP20 package. The device is designed to operate at 3.0 volts with a maximum active supply current of 8.8 milliamperes, and a standby current of 1 μa. The main divider operates over a frequency range of 500 to 1300 MHz, with an RF input signal sensitivity of –18 dBm. The auxiliary divider operates over the range between 80 to 550 MHz with equal sensitivity. The external, high-precision reference oscillator provides low drift, low phase noise accuracy to the two sources. (Note: Please refer to the SA7026 data sheet for exact device specifications.)

9.1.1. Loop filter design vs. charge pump current

An example of the design of an effective loop filter is shown below. Note that loop filter bandwidth increases when the charge pump compensation switches to speedup mode during channel switching.

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}	I_{PHI}
0	0	$1.5xI_{SET}$	$3xI_{SET}$	$15xI_{SET}$	$36xI_{SET}$
0	1	$0.5xI_{SET}$	$1xI_{SET}$	$5xI_{SET}$	$12xI_{SET}$
1	0	$1.5xI_{SET}$	$3xI_{SET}$	$15xI_{SET}$	0
1	1	$0.5xI_{SET}$	$1xI_{SET}$	$5xI_{SET}$	0

9.2. Features

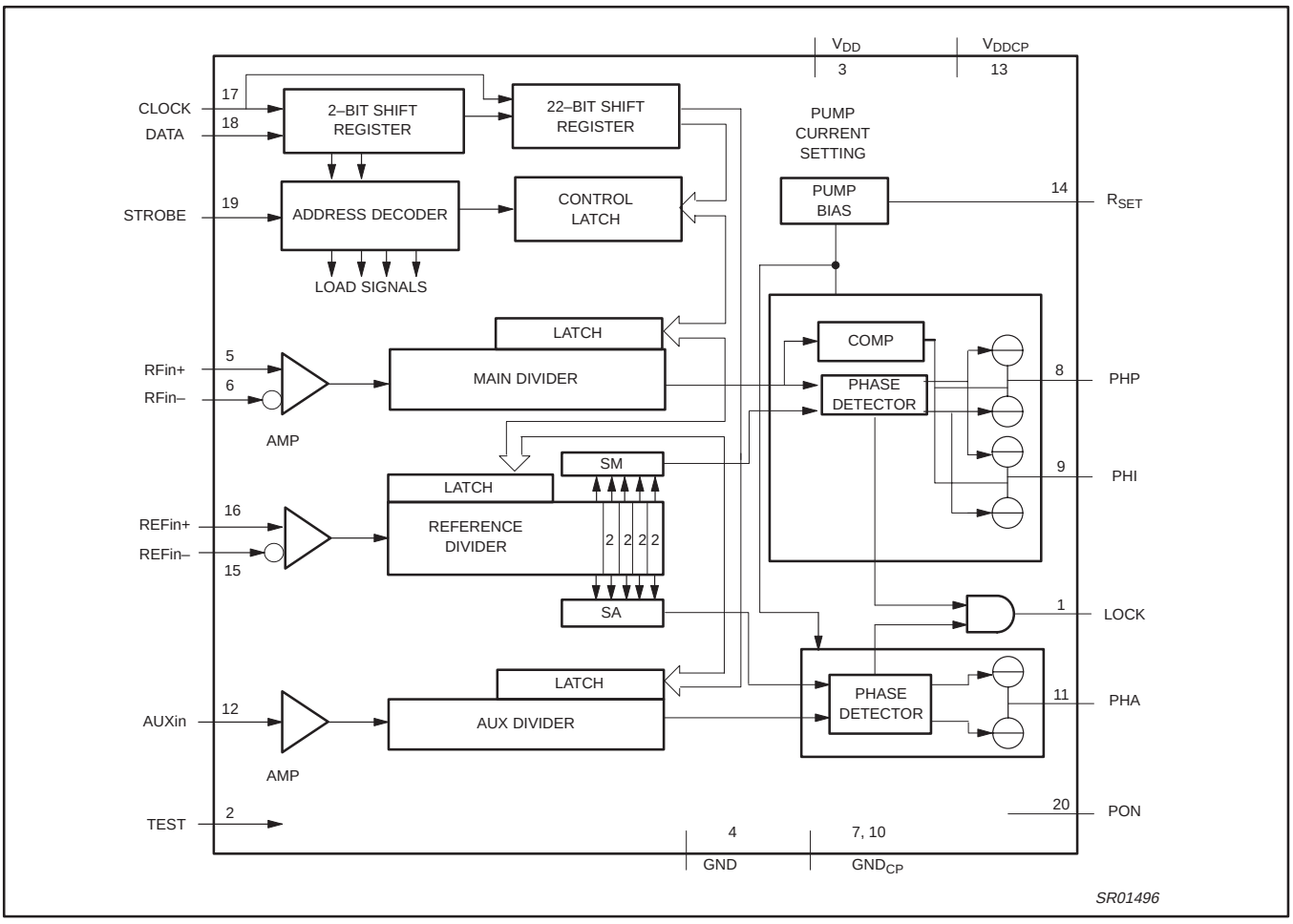


Figure 72. SA7026 block diagram

Table 11. SA7026 features

Typical performance:	
RF	
Main frequency range	1.3 GHz (max.)
Auxiliary frequency range	550 MHz (max.)
Reference frequency range	40 MHz (max.)
Phase comparison frequency	4 MHz (max.)
RF input sensitivity	–18 dBm (min.)
DC	
Supply voltage	2.7 V – 5.5 V
I_{CC} powered up	7.5 mA typical @ +3 V
I_{CC} powered down	1 μA @ +3 V
Features	
Low noise performance	
Fully programmable via 10 Mb/s 3-wire serial interface	
Hardware or software power-downs	
Package	TSSOP-20
Applications	
Mobile telephones	
Portable battery-powered equipment	

9.3. SA7026 Main loop filter design: 964 MHz

9.3.1. Design example:

VCO frequency (F_{VCO}) 940–970 MHz
Channel spacing (Fchan) = 30 kHz
Comparison frequency (Fcomp) = 8*30 kHz = 240 kHz
Switching time (t_{SW}) = 400 μsec
Switching step = 25 MHz
Frequency error = within 1 kHz
VCO gain (K_{VCO}) = 9 MHz/V Murata MQE001-964
Reference crystal TCXO (Fref) = 19.44 MHz

Determine R_{SET}:
Choose I_{CP} = 500 μA; CP = 00 or 10

$$I_{CP} = 3 \cdot I_{SET} = \frac{3 \cdot V_{SET}}{R_{SET}} = \frac{3 \cdot 1.25}{R_{SET}} = 500\ \mu A$$

R_{SET} = 7.5 kΩ
Determine N:
To ensure the same switching time from both directions, we use the worst case,

$$N = \frac{964\ MHz}{240\ KHz} = 4017$$

Determine ω_n:
From Equation (11) on Page 23:

$$\delta = \frac{1000}{25e6} = 0.04e\text{-}3$$

Pick $\zeta = 0.707$ … critically damped
From Equation (12) on Page 23:

$$\omega_n = \frac{-1n\left(0.04e{-}3 \cdot \sqrt{1{-}0.707^2}\right)}{0.707 * 400e{-}6} = 37034 \text{ rad/s}$$

Determine R_1, C_1, C_2:
Using Equation (13) on Page 23 with 2π from K_{VCO} (rad/V) and $1/2\pi$ from K_ϕ (A/rad) canceled out

$$C_1 = \frac{500e{-}6 \cdot 40e6}{4017 \cdot 37034^2} = 820 \text{ pF}$$

Using Equation (14) on Page 23:

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{4017}{500e{-}6 \cdot 9e6 \cdot 0.82e{-}9}\right)^{.5} = 47 \text{ k}\Omega\text{F}$$

Using Equation (15) on Page 23:

$$C_2 = 0.82\text{e}{-}9/10 = 82 \text{ pF}$$

Determine R_2, C_3:
Using Equation (16) on Page 23:

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_n$$

Auxiliary VCO:

F_{VCO} = 492.9 to 500.9 MHz
Fcomp = 240 kHz
Switching time = 1.8 ms
K_{VCO} = 6 MHz/V

Determine N:

$$N = \frac{500 \text{ MHz}}{240 \text{ kHz}} = 2083$$

Determine ω_n:

$$\delta = \frac{1000}{25e6} = 0.04\text{e-}3$$

Pick $\xi = 0.707$

$$\omega_n = \frac{-1n\left(0.04e{-}3 \cdot \sqrt{1{-}0.707^2}\right)}{0.707 \cdot 1800e{-}6} = 8230 \text{ rad/s}$$

Determine R_1, C_1, C_2:

$$C_1 = \left(\frac{250e{-}6 \cdot 6e6}{2083 \cdot 8230^2}\right) = 10.63 \text{ nF} \qquad \Rightarrow \text{use 10 nF}$$

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{2083}{250e{-}6 \cdot 6e6 \cdot 10e{-}9}\right)^{.5} = 16.67 \text{ k}\Omega \qquad \Rightarrow \text{use 18 k}\Omega$$

$$C_2 = \frac{10e{-}9}{10} = 1 \text{ nF}$$

9.3.2. Measured performance

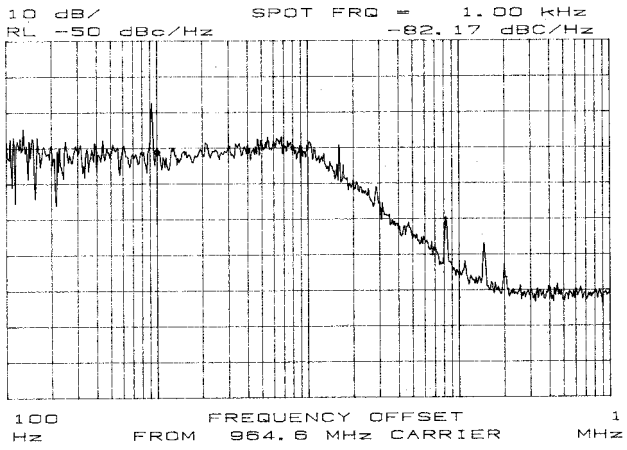


Figure 73. Loop filter response in Normal mode: CP = 10

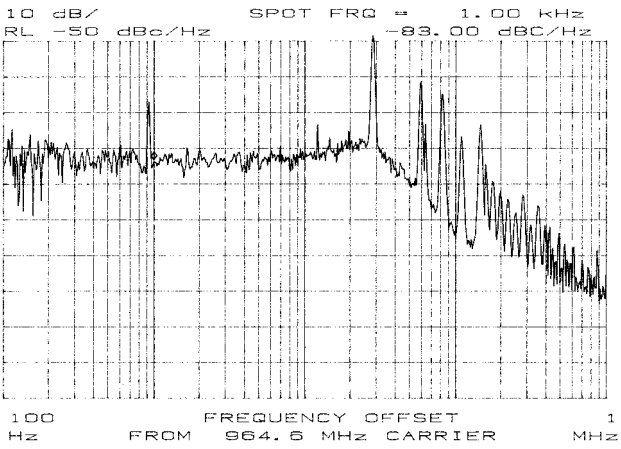


Figure 74. Loop filter response in Speedup mode: CP = 10

* With the same FDAC value as in normal mode, spurs are enhanced during the speedup mode. The designer needs to adjust the FDAC value if speedup mode is used all the time.

Loop BW calculated from Equation (17) on Page 23= 12.13 kHz

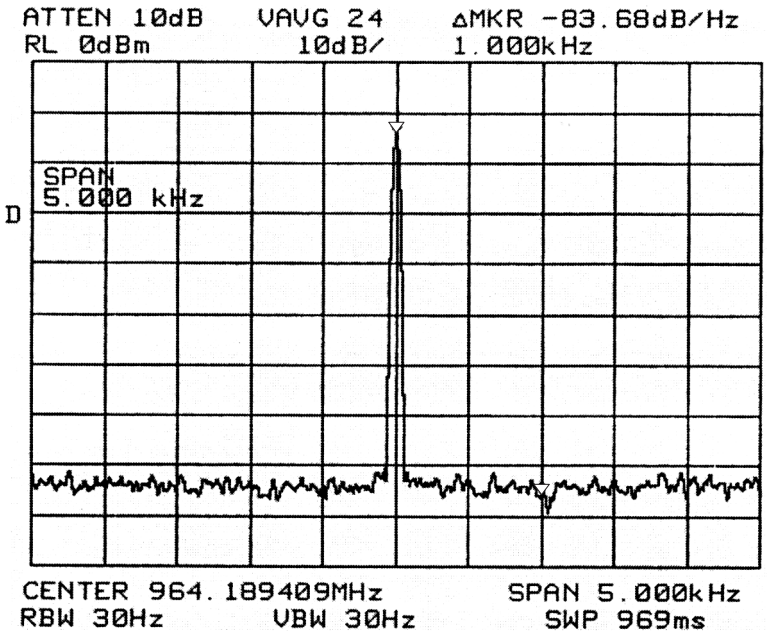


Figure 75. SA7026 Main phase noise measurement result (@1 kHz Offset = –83.68 dBc/Hz)

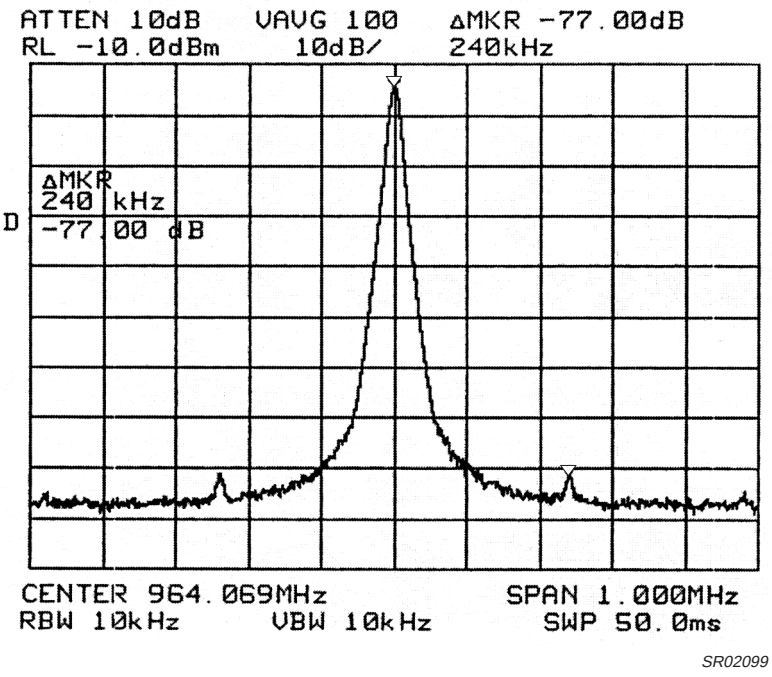


Figure 76. SA7026 Comparison spur measurement result 7026 (@240 kHz = –77.00 dB)

Fractional Compensation Performance:

The quickest way to check for Fractional Compensation Performance is to set FDAC = 0, then increase FDAC until optimal compensation is found. Note that this value might vary by a few counts from device to device. This variation is also board layout, V_{CC}, and I_{SET} dependent.

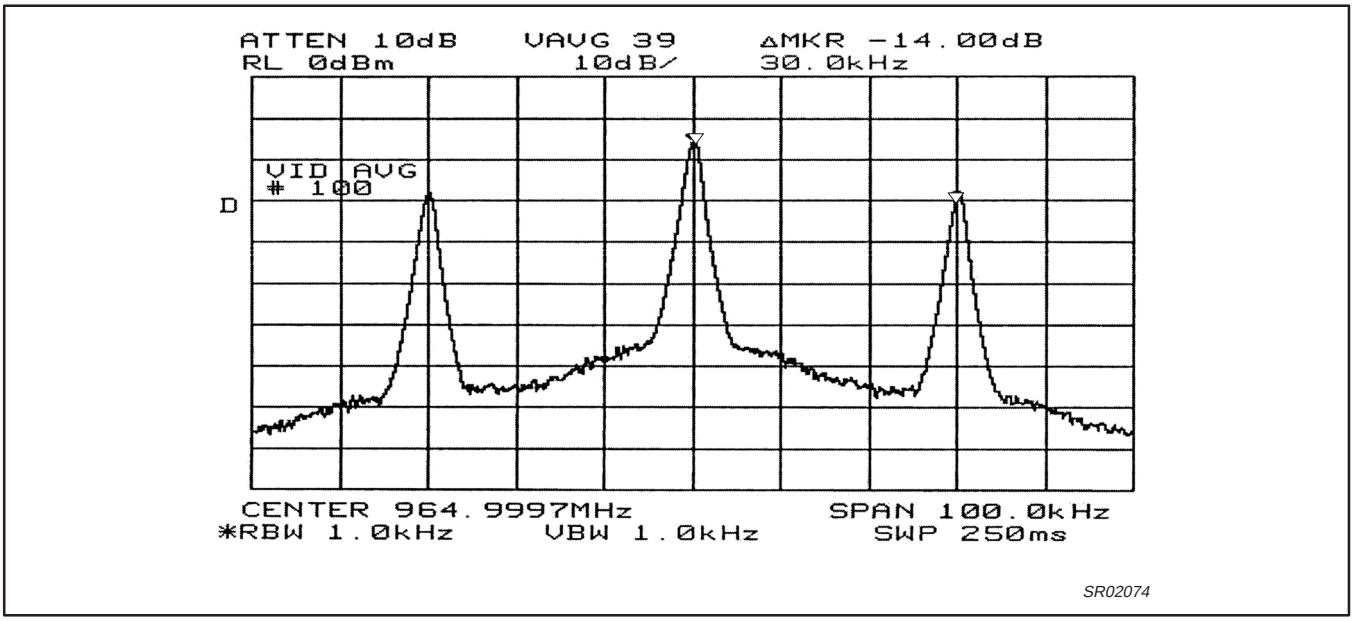


Figure 77. Fractional spur @ 30 kHz = –14 dBc; FDAC = 0 (uncompensated)

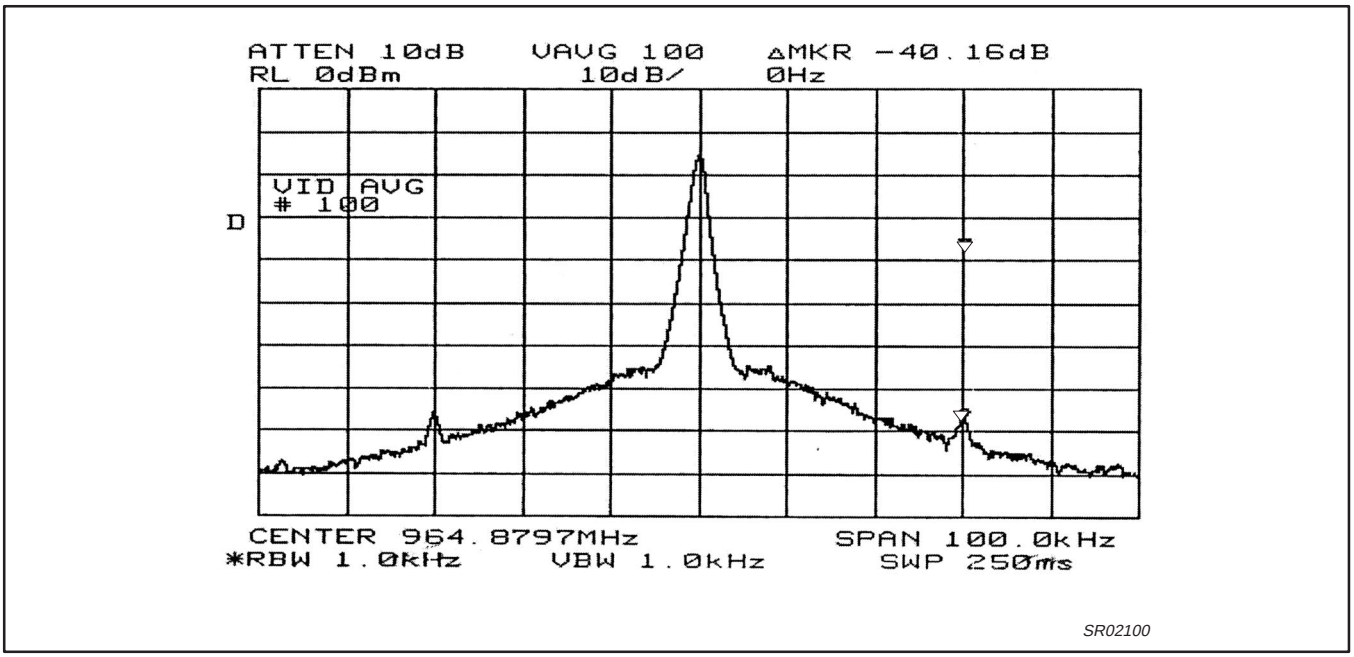


Figure 78. Fractional spur @ 30 kHz = –40.16 dBc; FDAC = 76 (compensated)

SA7026 Auxiliary phase noise

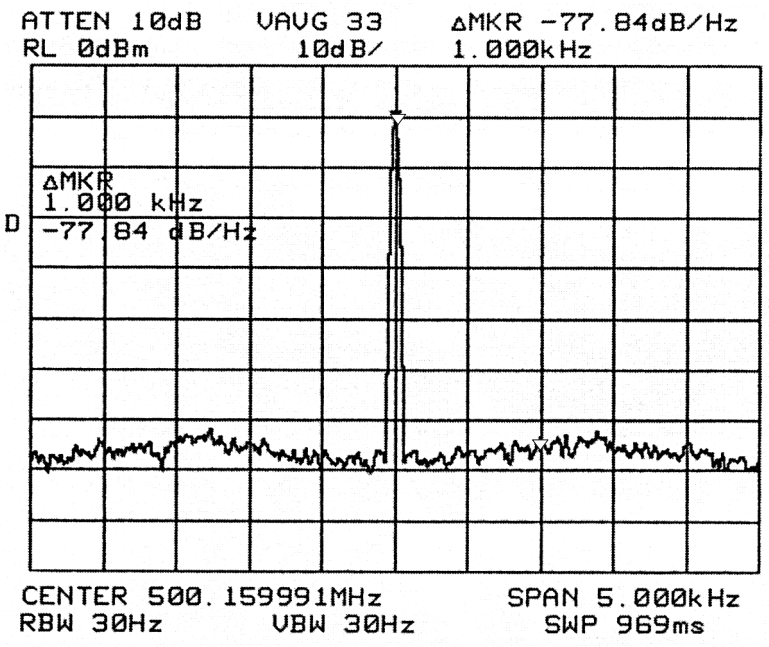


Figure 79. SA7026 AUX phase noise measurement result @ 1 kHz offset = –77.84 dBc/Hz

Optional AUX: (SA7026)

There are provisions for an optional Philips SA602 on the demo board for designers that wish to implement an Auxiliary frequency other than the standard VCO module allows.

Switching Time:

The Channel switching time response and settling time is identical to that shown in the application note for the SA8026 (see Section 8.1.3. on Page 52).

10. SA7026 DEMO BOARD

10.1. Setup instructions

10.1.1. Demo board setup

1. Connect the interface cable from the demo board to the interface card.
2. Plug the 3-wire interface card into the parallel port of the computer and attach to port connector on the demo board.
3. Supply the demo board with 7 VDC. Refer to the individual Demo Board schematic and layout for component placement and exact circuit values. (All supply voltages are set to proper value when board is shipped).
4. Switches SW-1 and SW-2 are used to select either the regulated on-board supply or external supply voltage. (For SA7026 and SA7016, set both SW-1 and SW-2 fully CCW).
5. Tweak VR3, regulator U4, for SA7026 pin 13 voltage equal to 3.7 volts.
6. VR1 on “bottom side” of 7026 board (V_{DD}, pin 3) is adjusted for 3.0 volts.
7. Connect MAIN-OUT or AUX-OUT to the spectrum analyzer.
8. Run WINSYNTH.EXE to program the device.
9. The Lock detect LED is ON when Main VCO **and** AUX VCO are locked.

Supply Voltage: Frequency Sources SA7026	
Main VCO:	4.2 VDC
AUX VCO:	4.7 VDC
TCXO:	3.3 VDC

See SA7026 power supply section board layout.

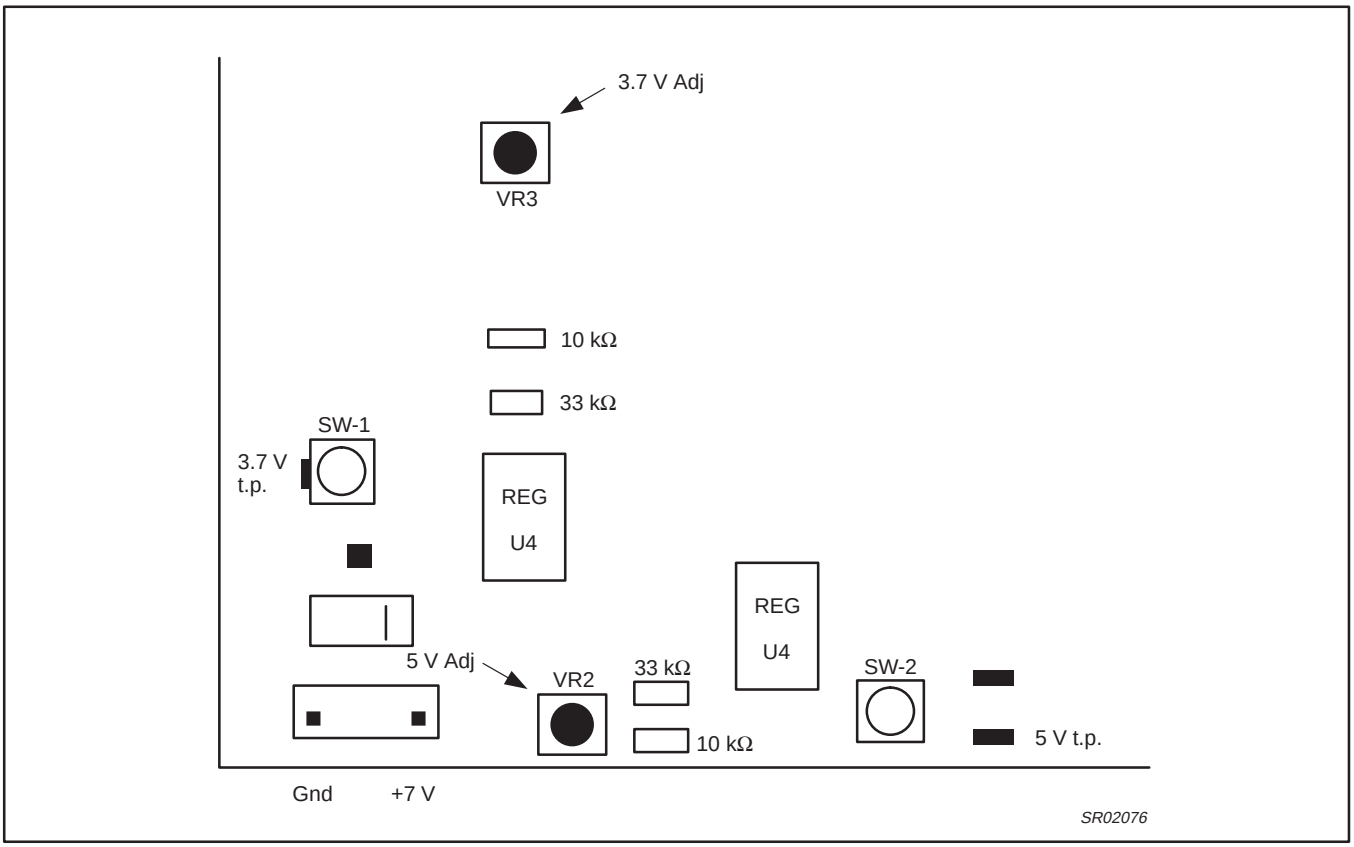


Figure 80. SA7026 demo board regulator section

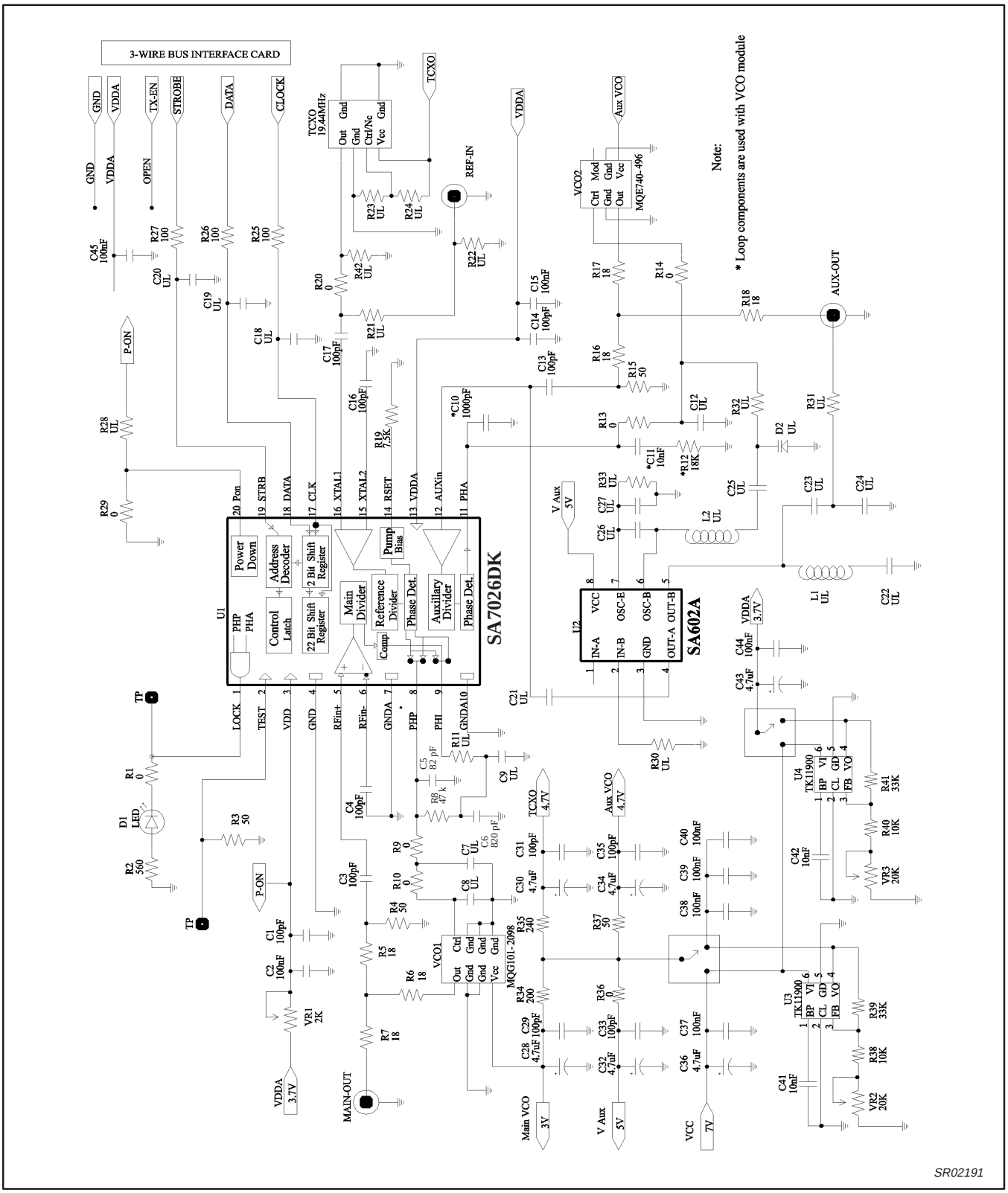


Figure 81. SA7026 demo board schematic diagram

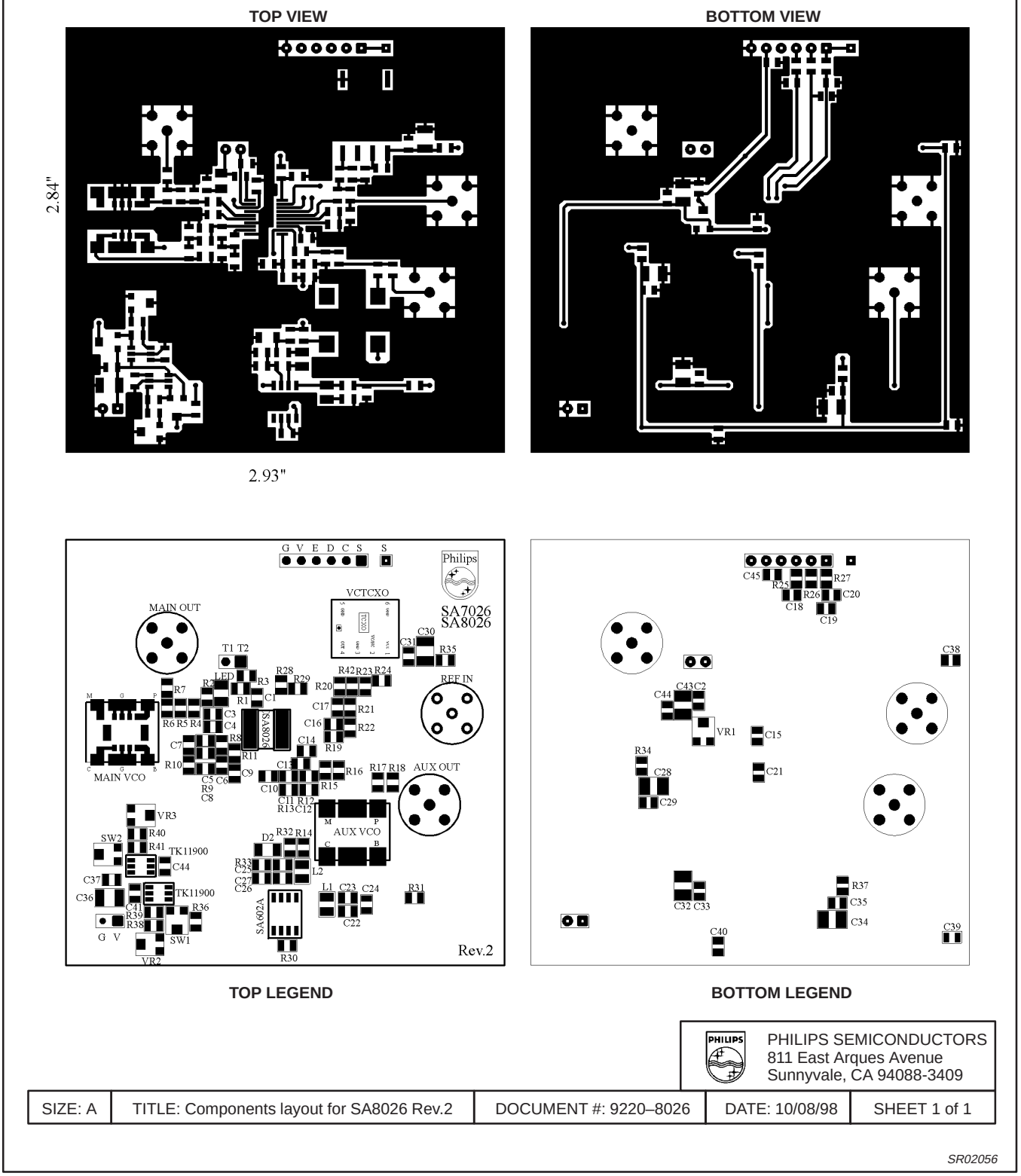


Figure 82. SA8026/7026 demo board

10.2. SA7026 Bill of materials

Table 12. Application components list for SA7026 demo board

Qty	Volt	Value	Part Reference	Part Description	Vendor	Mfr.	Part Number
Surface Mount Capacitor							
1	50 V	8.2 pF	C26	CAP CER 0805 NPO ±0.5 pF	Garrett	Philips	0805CG829C9BB0
1	50 V	12 pF	C27	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG120J9BB0
2	50 V	18 pF	C23, C25	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG829C9BB0
1	50 V	56 pF	C24	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG560J9BB0
1	50 V	82 pF	C5	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG820J9BB0
13	50 V	100 pF	C1, 3, 4, 5, 13, 14, 16, C17, 21, 29, 31, 33, 35	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG101J9BB0
1	50 V	820 pF	C6	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG821J9BB0
2	50 V	1000 pF	C10, C22	CAP CER 0805 NPO ±5%	Garrett	Philips	0805CG102J9BB0
3	50 V	0.01 μF	C11, C41, C42	CAP CER 0805 X7R ±10%	Garrett	Philips	08052R103K9BB0
8	50 V	0.1 μF	C2, 15, 37, 38, 39, 40, 44, 45	CAP CER 0805 Z5U ±20%	Garrett	Philips	08052E104M9BB0
6	16 V	4.7 μF	C28, 30, 32, 34, 36, 43	TANTALUM CHIP CAP	Garrett	Matsuo	267M 1602 475K 533
7		UL	C7, 8, 9, 12, 18, 19, 20				
Surface Mount Resistor							
10	50 V	0 Ω	R1, 9, 10, 13, 14, 20, 29 R31, 32, 36	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A000-JK
6	50 V	18 Ω	R5, 6, 7, 16, 17, 18	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A180-JK
4	50 V	50 Ω	R3, 4, 15, 37	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A500-JK
3	50 V	100 Ω	R25, 26, 27	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A101-JK
1	50 V	200 Ω	R34	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A201-JK
1	50 V	560 Ω	R2	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A561-JK
1	50 V	1.2 kΩ	R35	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A122-JK
1	50 V	7.5 kΩ	R19	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A752-JK
4	50 V	10 kΩ	R30, 33, 38, 40	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A103-JK
2	50 V	12 kΩ	R23, R24	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A123-JK
1	50 V	18 kΩ	R12	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A183-JK
2	50 V	33 kΩ	R39, R41	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A333-JK
1	50 V	47 kΩ	R8	RES CHIP 0805 1/10 W ±5%	Garrett	Philips	9C08052A473-JK
5		UL	R11, 21, 22, 28, 42				
Surface Mount Inductor							
1	50 V	180 nH	L1	Surface Mount Inductor	Coilcraft	Coilcraft	1008HS-181TKBC
1	50 V	750 nH	L2	Surface Mount Inductor	Coilcraft	Coilcraft	1008HS-751TKBC
Surface Mount Resistor Trimmer							
1	50 V	2 k	VR1	3mm 1-Turn J-H Trimmer	Garrett	Tocos	G3A202M
2	50 V	20 k	VR2, VR3	3mm 1-Turn J-H Trimmer	Garrett	Tocos	G3A203M
Surface Mount Selector Switch							
2	50 V	Switch	SW1, SW2	3mm Selector Switch	Digikey	Bourns	7813J-1-023E
Surface Mount Temperature Control Crystal Oscillator							
1	3 V	19.44 MHz	TCXO	Temp. Control Crystal Oscillator	KSS	KSS	TCXO-201C1-19.44
Surface Mount Voltage Control Oscillator							
1	5 V	496 MHz	VCO	Voltage Control Oscillator	Murata	Murata	MQE740-496
1	4.2 V	964 MHz	VCO	Voltage Control Oscillator	Murata	Murata	MQE001-964
Surface Mount LED							
1	50 V	LED	D1	Surface Mount LED	Digikey	Lumex	LU60205CT-ND
Surface Mount Diode							
1	50 V	BB215	D2	Variable Capacitance Diode	Philips	Philips	BB215
Surface Mount Integrated Circuit							
1	3.7 V	SA7026	U1	1.3 GHz Fractional-N-Synthe.	Philips	Philips	SA7026
1	5 V	SA602A	U2	Dual Balance Mixer Oscillator	Philips	Philips	SA602A
2	25 V	TK11900	U3, U4	Adjustable Voltage Regulator	Tocos	Tocos	TK11900
Miscellaneous							
1				Printed Circuit Board	KML Vector	Philips	SA7026/SA8026
3		SMA	Main-out, Ref-in, Aux-out	SMA Straight Receptacle	DC Elect.	Connex	132134
1		Header		Single Row Header 36-Pins	Mouser	Waldom	538-22-03-2121

11. INTRODUCTION TO THE SA8016/7016 LOW VOLTAGE FRACTIONAL-N FREQUENCY SYNTHESIZER

11.1. Description

The SA8016 and SA7016 low voltage, fractional-N synthesizers. They are single PLL counterparts of the SA8026 and SA7026 in the TSSOP16 package, in which there are no auxiliary PLL and PHI current charge pumps to achieve lower current consumption and reduced package size in single PLL applications. The SA8016 draws a maximum current of 9.5 mA and the SA7016 a maximum of 7.3 mA. A block diagram of the SA8016/SA7016 is shown in Figure 83 and the typical features are listed in Table 14.

The output charge pump current setting can be configured via software for the SA8016/SA7016 (see Table 13). The settings are different for the SA8026/SA7026 and can be found in Table 2 on Page 5.

The theoretical fundamentals, design example and performance measurements for the SA8016 and the SA8026 are the same. This is also true for the SA7016 and the SA7026. Please refer to the appropriate sections for additional details.

Figures 84 and 85 show the schematic and layout of the SA8016/7016 demo board.

11.2. Setup instructions

11.2.1. Demo board setup

1. Connect the interface cable from the demo board to the interface card.
2. Plug the interface card to the parallel port.
3. Supply the demo board with 7 VDC.
4. Switches SW-1 and SW-2 are used to select on-board regulated supply or external supply voltage.
5. Tweak R30 for appropriate VDDA; (default is set for 3.7 VDC on the demo board)
6. Tweak R4 for V_{DD} if V_{DD} is different from VDDA.
7. Connect MAIN-OUT to the spectrum analyzer.
8. Run WINSYNTH.EXE to program the device.

Supply Voltage:		
	SA8016:	**SA7016:**
Main VCO:	3.0 VDC	4.2 VDC
TCXO:	3.3 VDC	3.3 VDC

Table 13. Charge pump current settings for SA8016/7016

CP0	I_{PHP}	I_{PHP-SU}
0	$3xI_{SET}$	$15xI_{SET}$
1	$1xI_{SET}$	$5xI_{SET}$

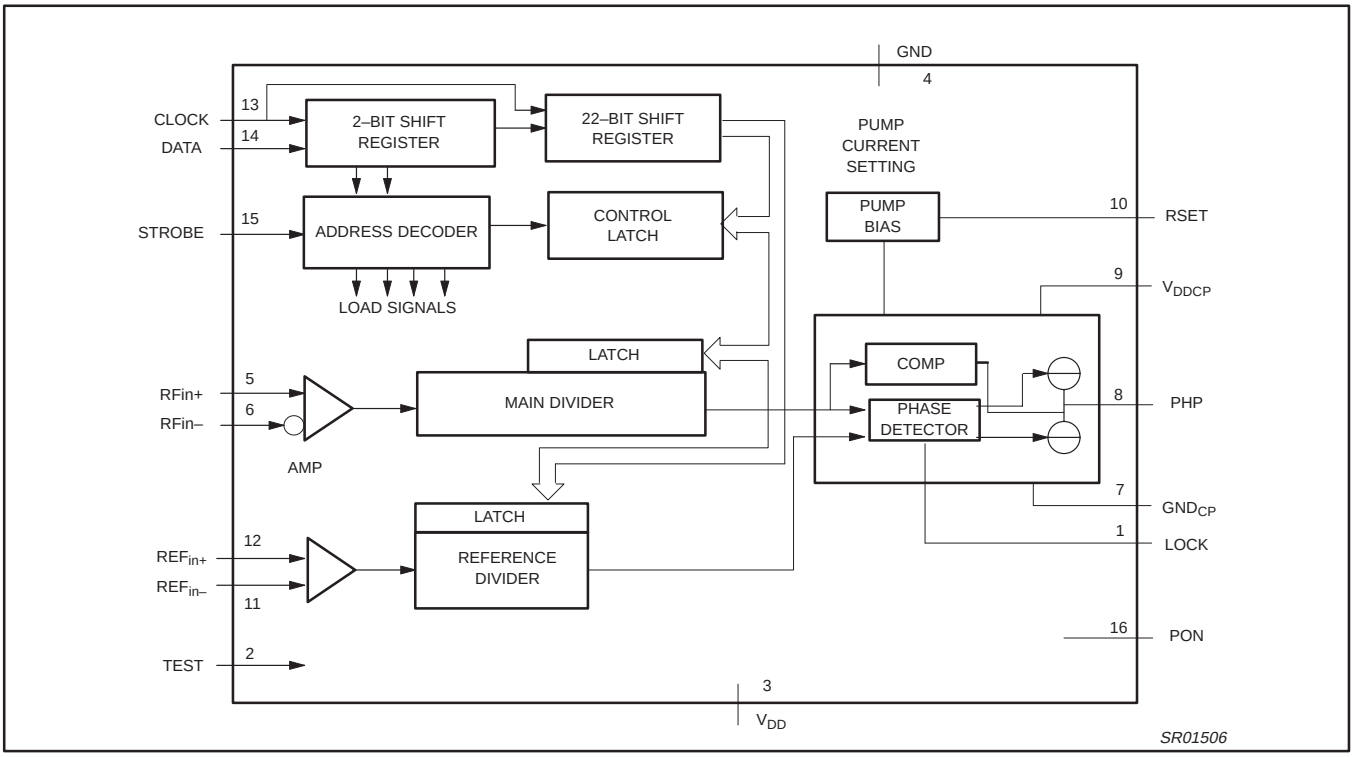


Figure 83. SA8016/SA7016 block diagram

11.3. Features

Table 14. SA8016/SA7016 features

Typical performance of SA8016		**Typical performance of SA7016**	
RF:		**RF:**	
Main Freq. Range:	2.5 GHz max.	Main Freq. Range:	1.3 GHz max.
Ref Frequency Range:	40 MHz max.	Ref Frequency Range:	40 MHz max.
Phase Comparison Freq.:	4 MHz max.	Phase Comparison Freq.:	4 MHz max.
RF Input Sensitivity:	–18 dBm min.	RF Input Sensitivity:	–18 dBm min.
DC:		**DC:**	
Supply Voltage:	2.7 – 5.5 V	Supply Voltage:	2.7 – 5.5 V
I_{CC} Powered-up:	8 mA Typ @ +3 V	I_{CC} Powered-up:	6.2 mA Typ @ +3 V
I_{CC} Powered-down:	1 μA @ +3 V	I_{CC} Powered-down:	1 μA @ +3 V
Features:		**Features:**	
Low-noise Performance		Low-noise Performance	
Fully-programmable via 10 Mb/s 3-wire serial interface		Fully-programmable via 10 Mb/s 3-wire serial interface	
S/W power downs		S/W power downs	
Package:	TSSOP-16	**Package:**	TSSOP-16
Applications:		**Applications:**	
2 GHz PCS mobile telephones, WLAN		1 GHz PCS mobile telephones, WLAN	
Portable battery-powered equipment		Portable battery-powered equipment	

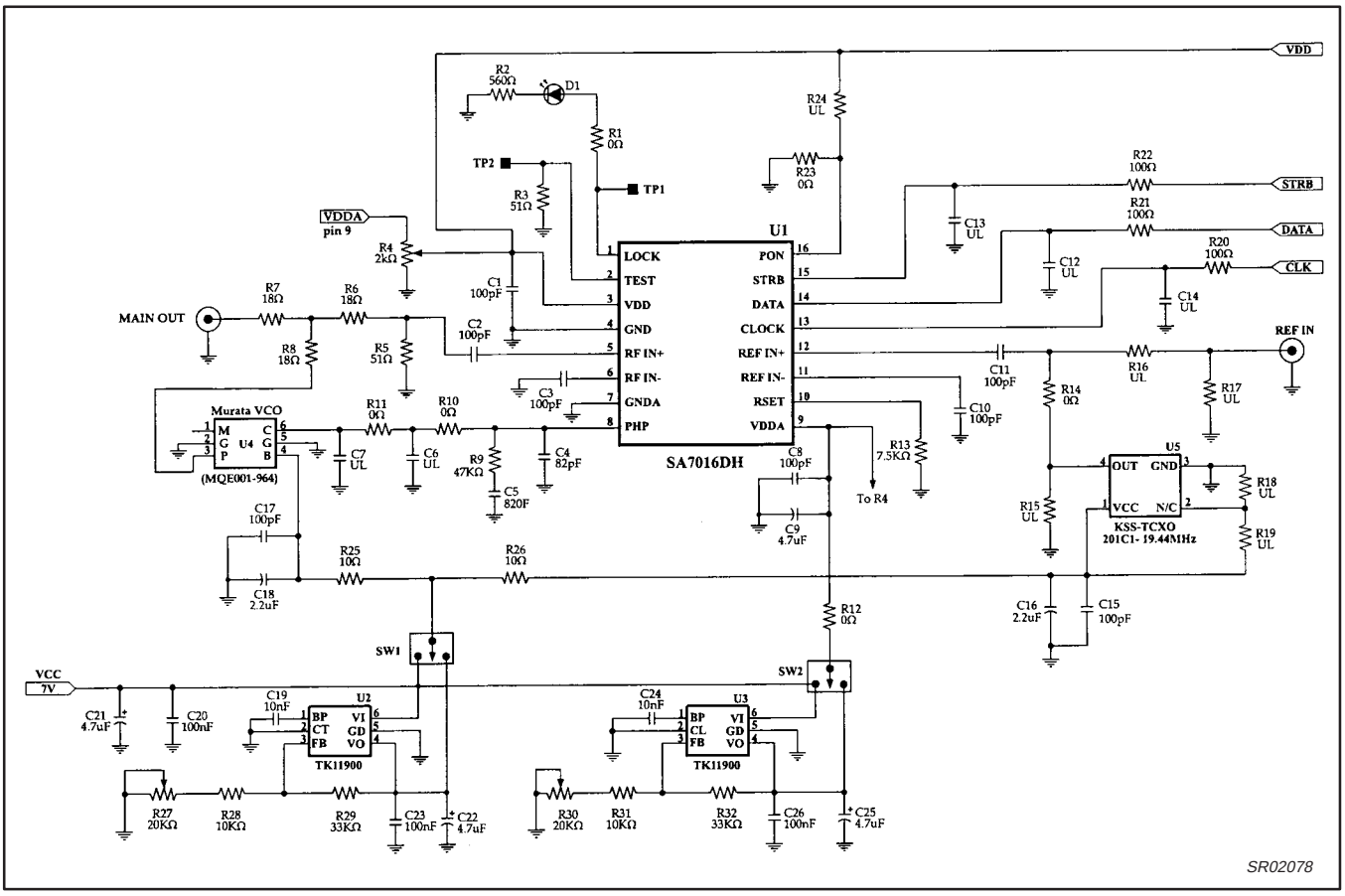


Figure 84. SA7016 Demo board schematic

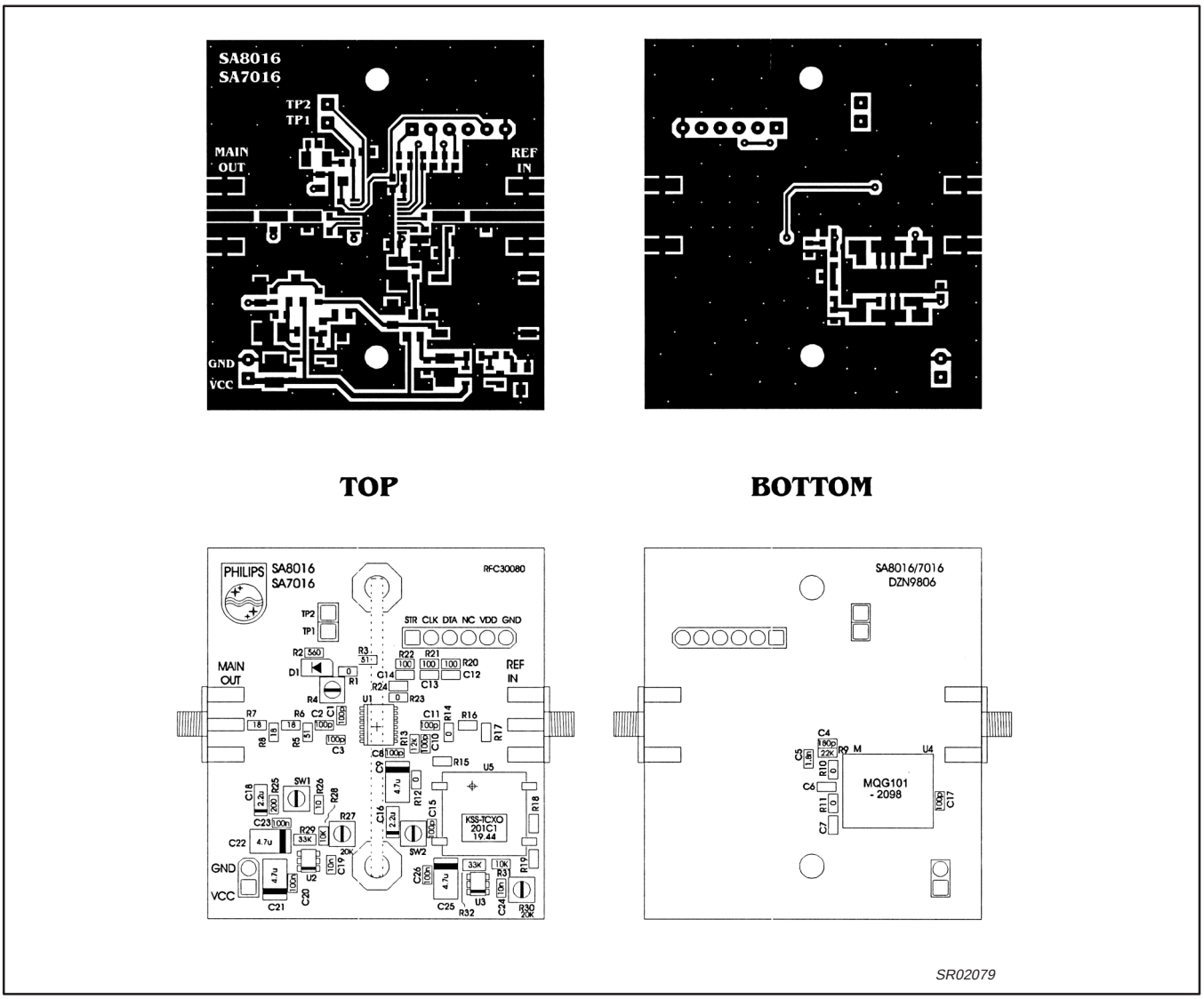


Figure 85. SA8016/7016 demo board layout

11.4. SA8016/7016 Bill of materials

Table 15. SA8016/7016 Bill of materials

Qty	Value	Part Reference	Part Description	Vendor Part Number	Manufacturer
Surface Mount Capacitors					
8	100 pF	C1, C2, C3, C8, C10, C11, C15, C17	NPO Ceramic 0603 ±5% 50 V	Garrett CE101J1NO	MMC
1	180 pF (82 pF[1])	C4	NPO Ceramic 0603 ±5% 50 V	Garrett CE181J1NO	MMC
1	1.8 nF (820 pF[1])	C5	X7R Ceramic 0603 ±5% 50 V	Garrett CE182K1NR	MMC
2	10 nF	C19, C24	X7R Ceramic 0603 ±10% 25 V	Garrett CC103K1NR	MMC
3	100 nF	C21, C23, C26	Z5U Ceramic 0603 ±20% 25 V	Garrett CC104M1NU	MMC
2	2.2 µF	C18, C16	Tant Chip Cap 10 V A M-series ±10%	Garrett 267M1002225K-533	Matsuo Electronics
4	4.7 µF	C9, C20, C22, C25	Tant Chip Cap 20 V B M-series ±10%	Garrett 267M1602475K-533	Matsuo Electronics
5	NL	C6, C7, C12, C13, C14			
Surface Mount Resistors					
6	0	R1, R10, R11, R12, R14, R23	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-000JK	Philips
1	10	R26	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-100JK	Philips
3	18	R6, R7, R8	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-180JK	Philips
2	51	R3, R5	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-510JK	Philips
3	100	R20, R21, R22	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-201JK	Philips
1	200 (130[1])	R25	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-201JK	Philips
1	560	R2	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-561JK	Philips
1	2 k	R4	3mm 1-turn J-H Res Trimmer	Garrett G3B202M	Tocos America
2	10 k	R28, R31	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-103JK	Philips
1	12 k	R13	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-123JK	Philips
2	20 k	R27, R30	3mm 1-turn J-H Res Trimmer	Garrett Garrett G3B203M	Tocos America
1	22 k (47 k[1])	R9	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-223JK	Philips
2	33 k	R29, R32	Chip Res 0603 1/16 W ±5%	Garrett 9C06031A-333JK	Philips
6	NL	R15, R16, R17, R18, R19, R24			
Surface Mount Integrated Circuit					
1	SA8016 (7016[1])	U1	2.5 (1.3[1]) GHz Low voltage fractional-N synthesizer	SA8016DH (SA7016DH)	Philips SA8016
Miscellaneous					
1		U4A	VCO	MQG101-2098 (MQE001-964[1])	Murata
1		U5	TCXO 19.44 MHz	TCXO-201C1-19.44	KSS
1		U2, U3	Voltage regulator	TK11900	Toko
1	LED	D1	SMT LED – red	P500TR-ND	Panasonic LN125C
1	0.100” header		Single row straight header 0.100”	Digikey S1011-36-ND	Sullins
		SW1, SW2	3mm switch	Digikey 7813J-023ECT-ND	Bourns
2			SMA edge connector	Digikey J502-ND	EF Johnson 142-0701

NOTE:
1. Component values are for the SA7016 demo board.

12. WINSYNTH – SYNTHESIZERS SOFTWARE CONTROL

12.1. What is Winsynth?

- Winsynth is a 3-wire bus, PC-based control program for the new frequency synthesizers and runs under the Windows environment.
- Winsynth is designed with ease of control in mind.
- Winsynth is designed to present the majority of controls in each control window for quick access.
- Winsynth is still under construction.

12.2. What parts can be controlled by the program?

- Currently the program is set up to control:

SA1630 – SA7016 – SA7026 – SA8016 – SA8026 – SA9025 – SA9550 (in development)

12.3. Introduction

This control program has been designed to run in the 16-bit Windows 3.xx environment and will run under the Windows 95 and Windows 98 operating systems. The program cannot run under Windows NT due to the nature of this operating system. “NT” will intercept any attempt to write to the printer port. This will generate a port error message notifying the user that port communication will not be successful.

Figure 86 shows how the screen for the SA8026 and other dual synthesizer parts will look. The control window is laid out with associated controls in the block with which they belong. The window is organized with the Main VCO control occupying the upper left and the associated register words in the lower left of the window.

The upper center portion holds the Reference Divider controls, and below this, the Auxiliary VCO controls. Bottom center is a messaging window where the system will report anything that may need attention.

Above the messaging window is a series of button controls that allow sending all words to the device or only a single word to the Main or Auxiliary VCO control registers.

The upper right-hand portion of the window holds the controls that affect the charge pump. R_{SET}, I_{SET} and I_{PHP} are part of a charge pump current calculator and are interactive with each other. FDAC and CP Ratio affect the part’s charge pump settings.

The lower right portion shows a block set aside for presets and sequencing of the main VCO. You will be able to save the main VCO frequency settings in any of 9 storage settings. You will be able to update the display by selecting a preset, or update the display in addition to updating the device at the same time.

The Auto Load function, located just above the Data Word frame in the lower left, will send any changes that are made to the device. The Data Word window allows the display of data in either Hex or Binary format.

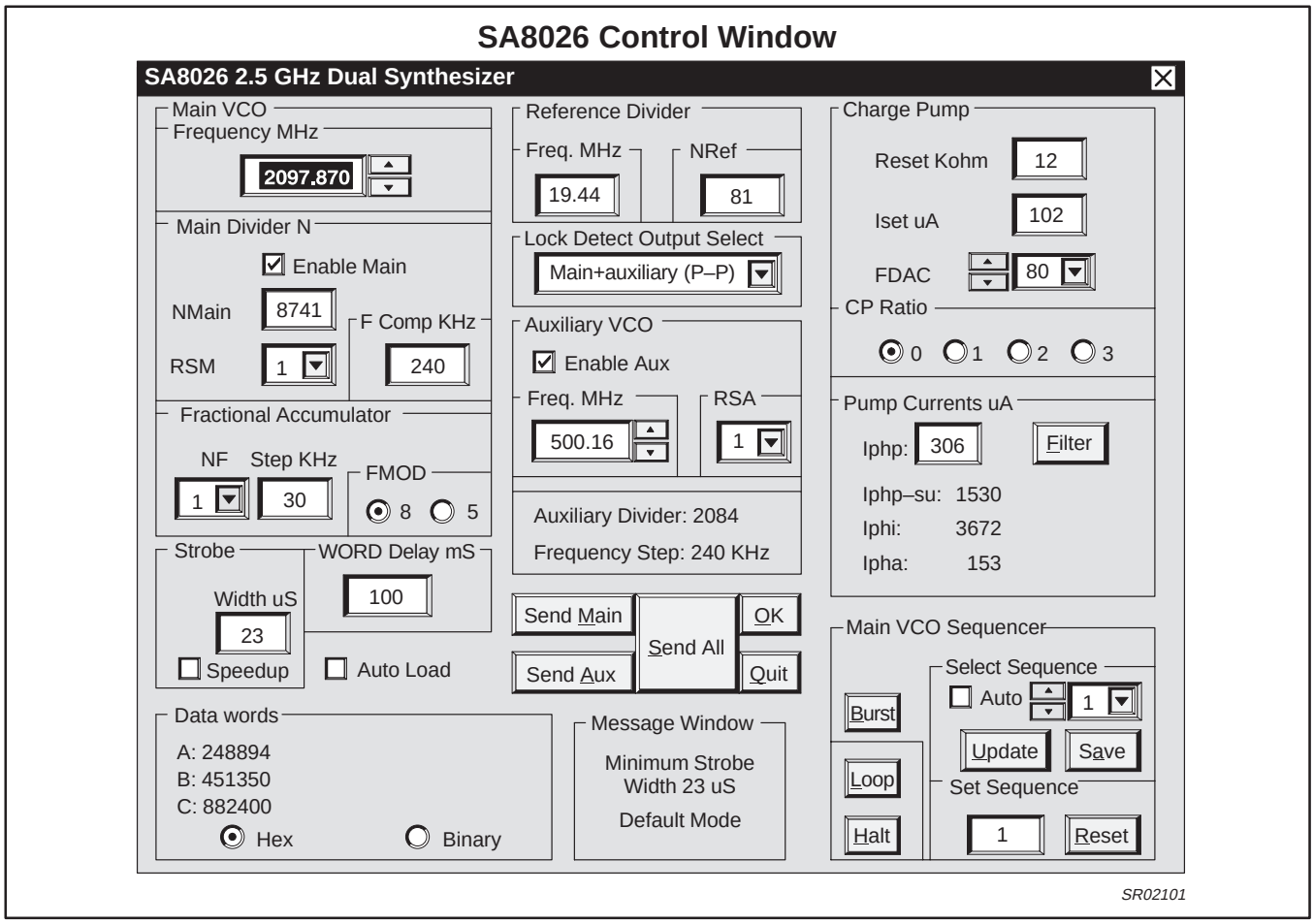


Figure 86. Shows the window for the dual synthesizer parts

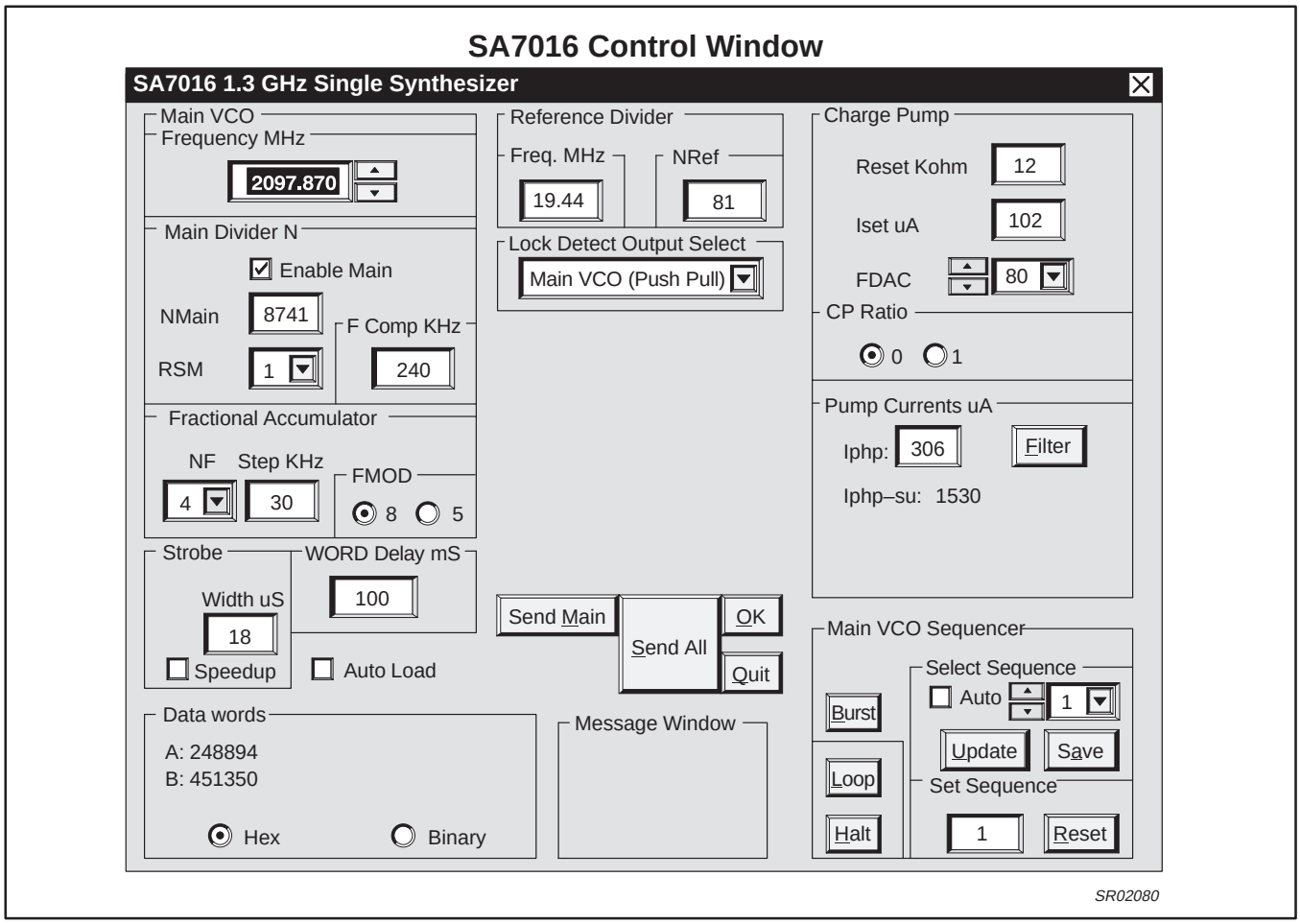


Figure 87. Shows the window for the single synthesizer parts

It can be seen that the two control windows are essentially the same, with the exception that in Figure 87 the Auxiliary VCO control is removed.

Figures 88 through 90 show the basic menu setup.

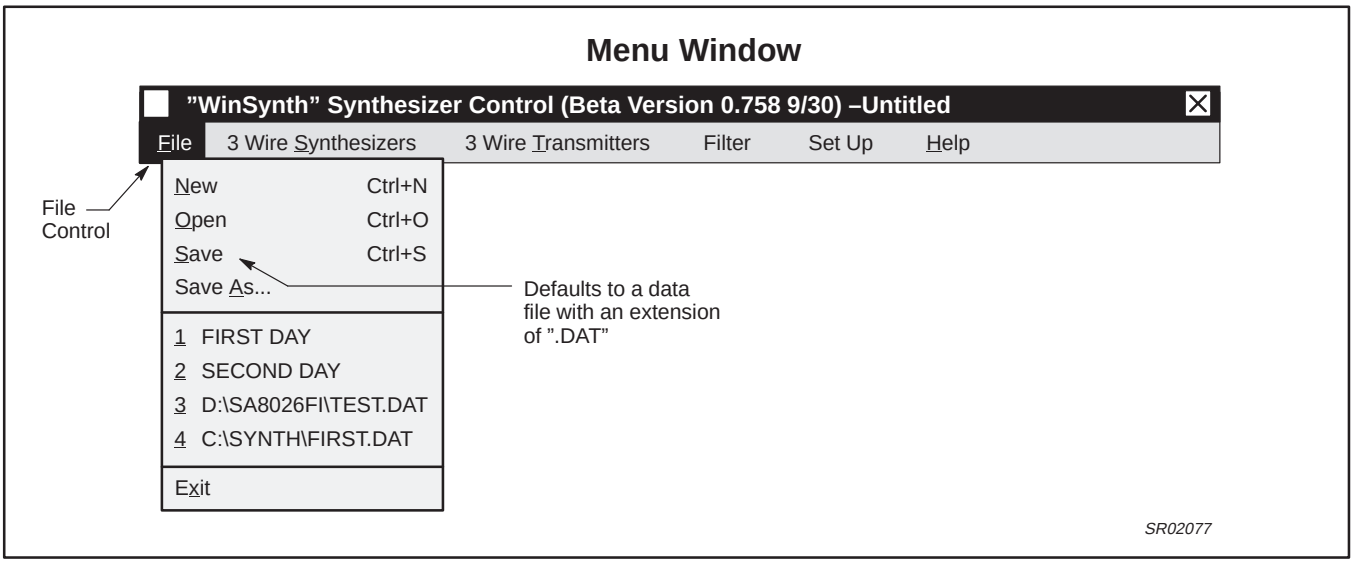


Figure 88.

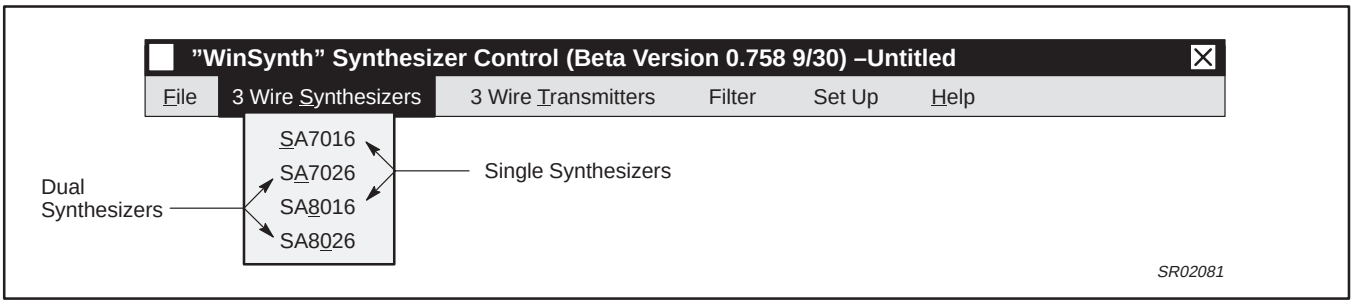


Figure 89.

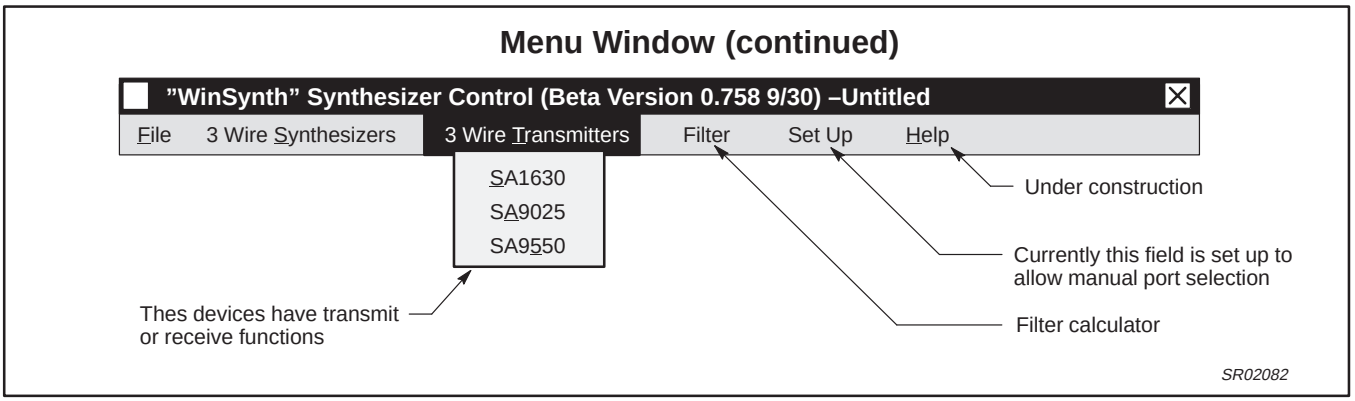


Figure 90.

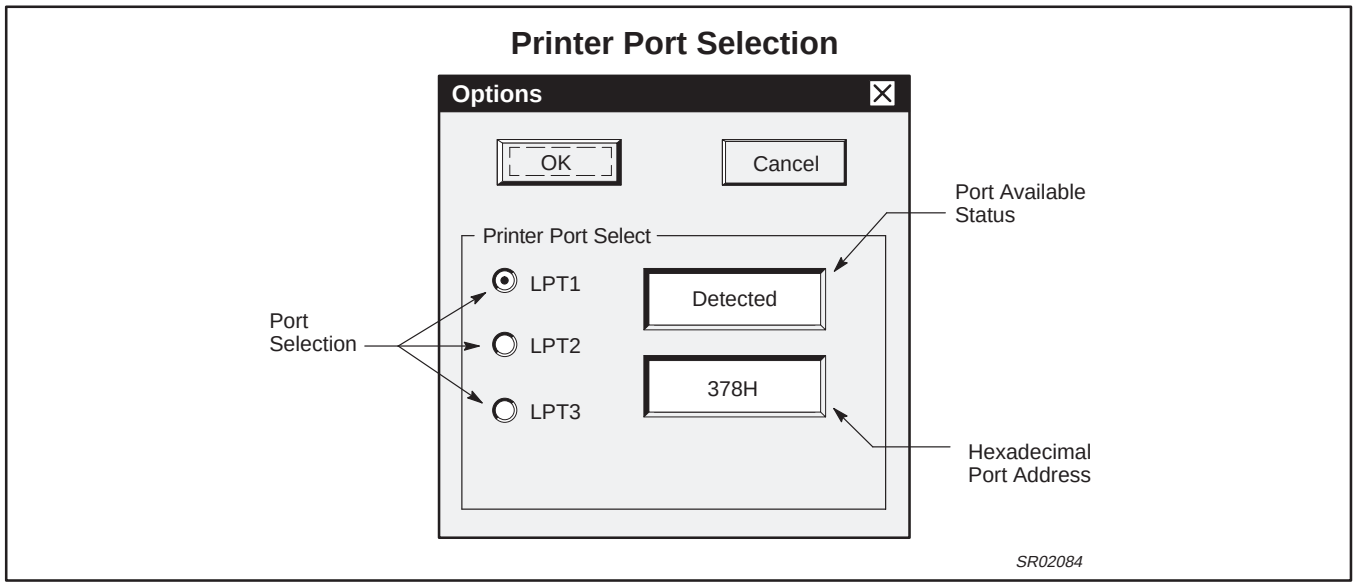


Figure 91. Printer port selection

The setup window (Figure 91) is currently configured for manual port selection and is accessed with the “Set Up” menu selection. After making a successful port connection, click on the “OK” button to save the settings. If “Cancel” is used, then no saving of settings will occur. The program will start up the first time defaulting to LPT1. If the hardware port is not the same address as selected, then there will be an error message generated indicating that there has been a “Port Error”. If this happens, then click out of the error box and select “Set Up” and reconfigure the port selection as seen here.

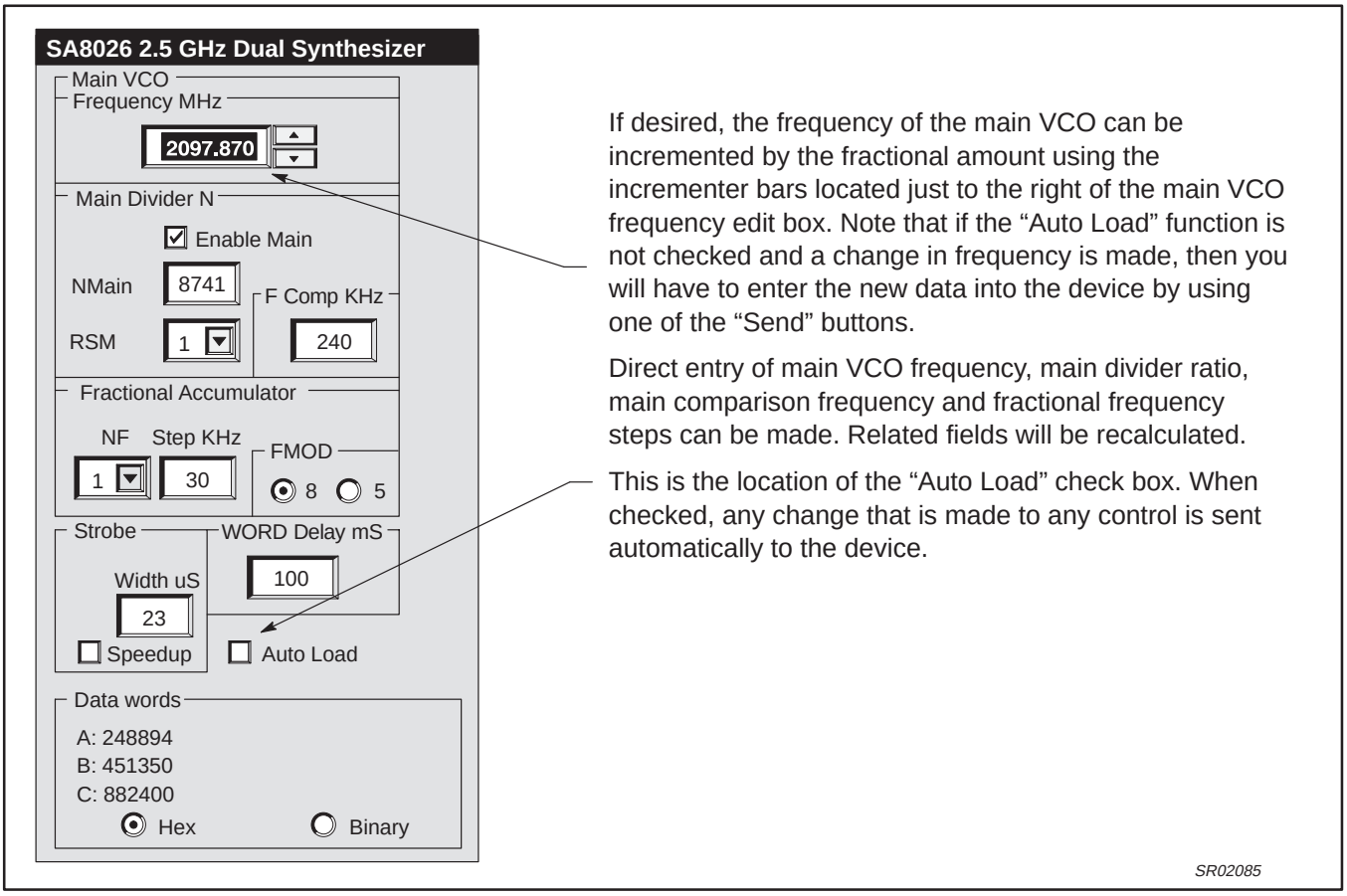


Figure 92.

Figure 92 shows the location of the “Auto Load” check box. When checked, any change that is made to any control is sent automatically to the device.

If desired, the frequency of the main VCO can be incremented by the fractional amount using the incrementer bars located just to the right of the main VCO frequency edit box. Note that if the “Auto Load” function is not checked and a change in frequency is made, then you will have to enter the new data into the device by using one of the “Send” buttons.

Direct entry of main VCO frequency, main divider ratio, main comparison frequency and fractional frequency steps can be made. Related fields will be recalculated.

Figures 93 and 94 focus in on the main VCO controls. It is suggested that the main comparison frequency be entered first, if different than the default value of 240 kHz used in the program. Then enter the desired reference frequency.

This is suggested because the reference frequency entries are related to the main comparison frequency. The reference divider ratio will be calculated using the main comparison frequency. You may find that it does not matter which order is chosen to initially set up this portion. With this taken care of, you can enter the desired VCO operating frequency. Note that all direct entries are set up not to use the enter key. Windows uses this key to execute the function or button that is highlighted. This is usually the “OK” button which normally will exit the window. There is a trap for this key that currently pops up a message box giving the user the option of exiting the current window.

Next, it may be desireable to send the current settings to the synthesizer. This can be accomplished in a number of ways. If it is decided that the device should be initialized with all words, then use the “Send All” button to perform this task. Otherwise, use the “Send Main” button to send just the one word associated with the main VCO register.

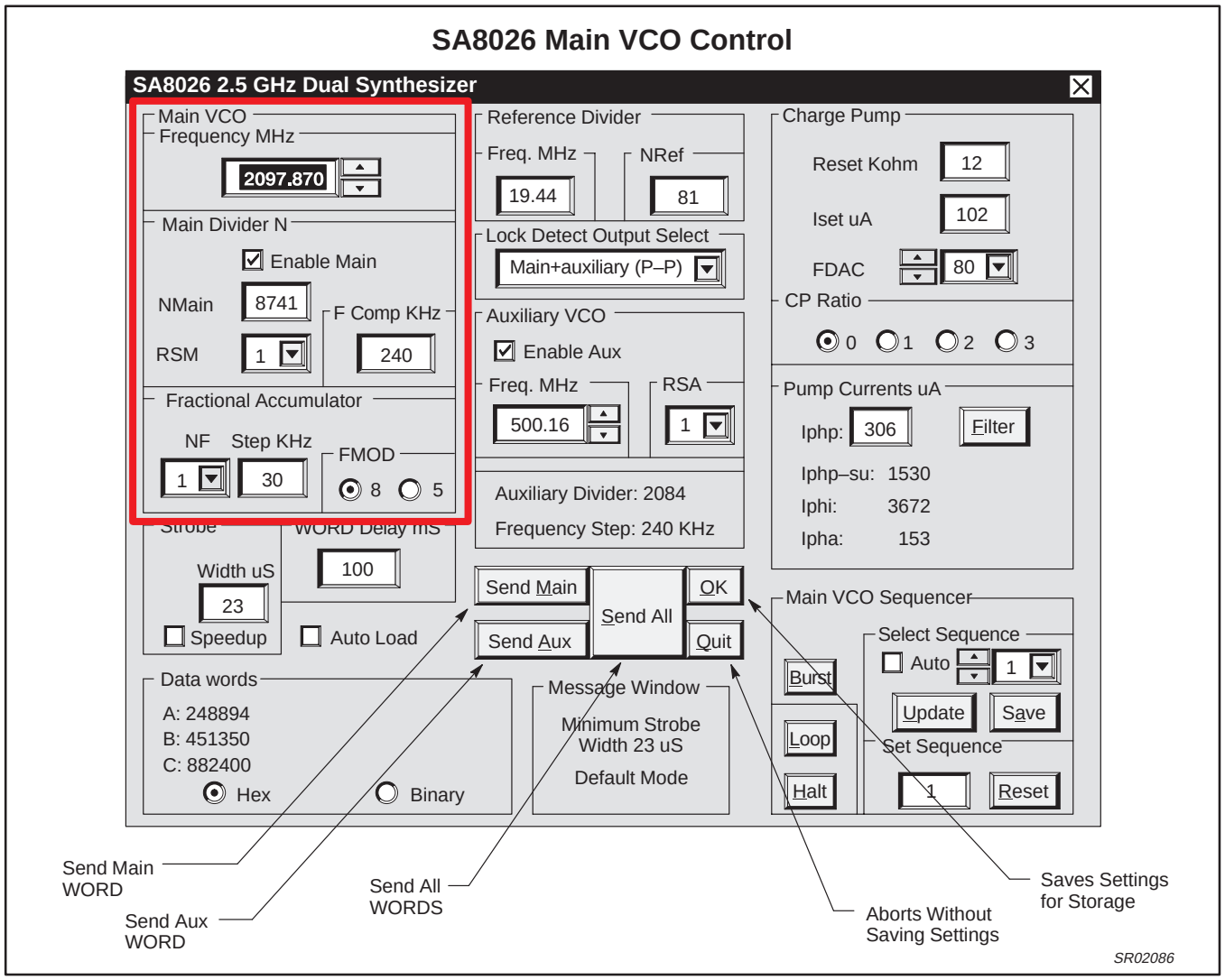


Figure 93. SA8026 main VCO control

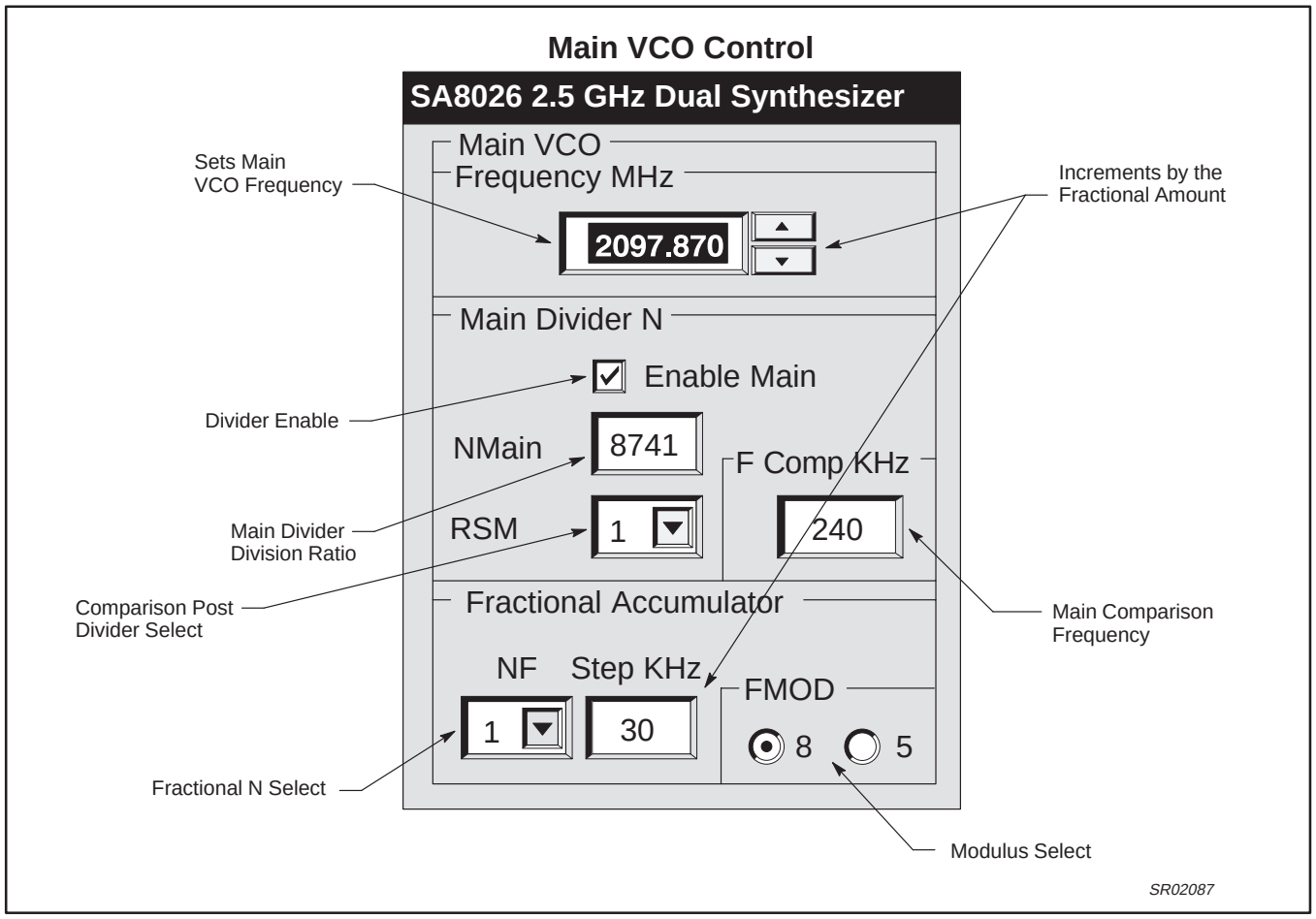


Figure 94. Main VCO control

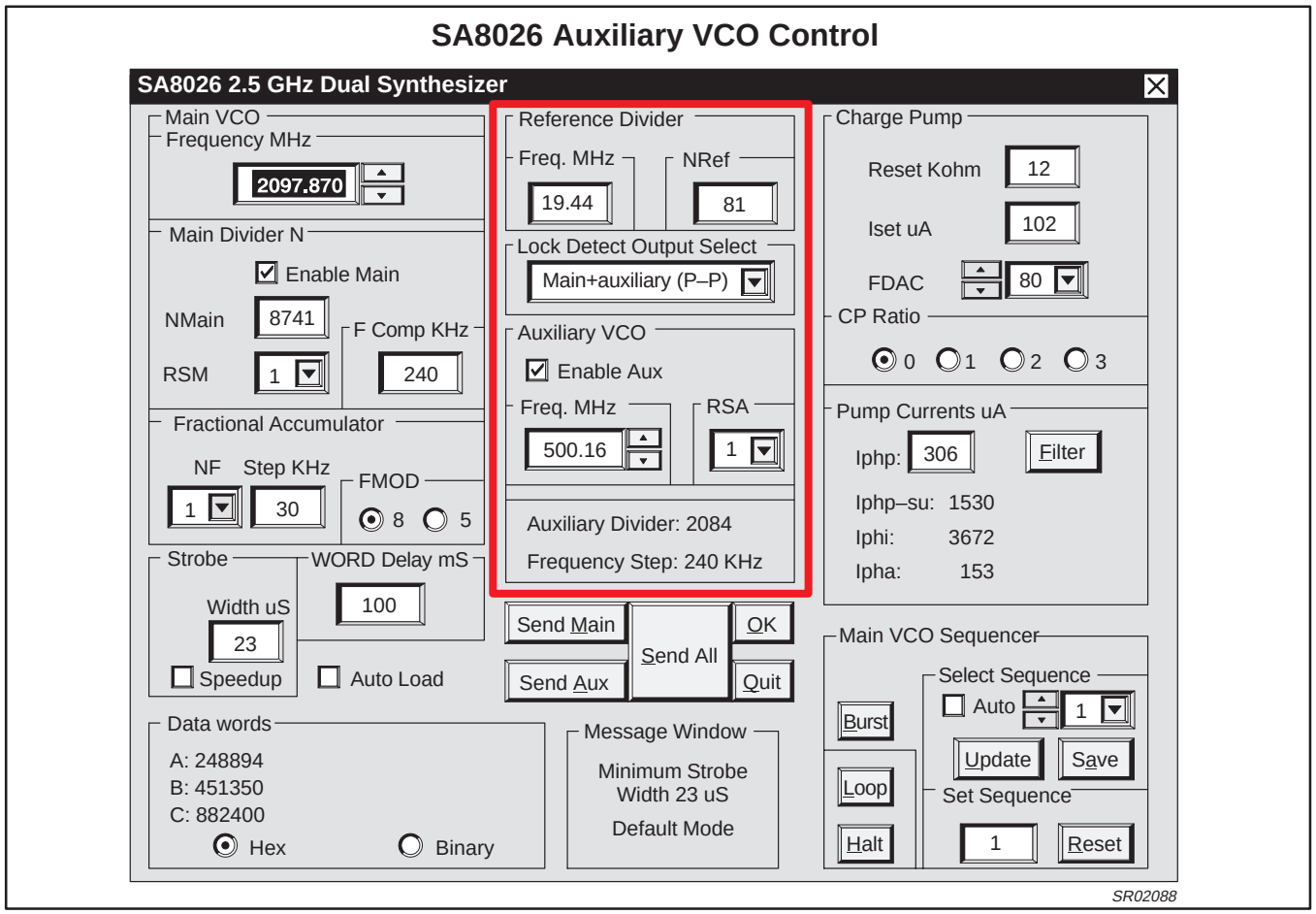


Figure 95. SA8026 auxiliary VCO control

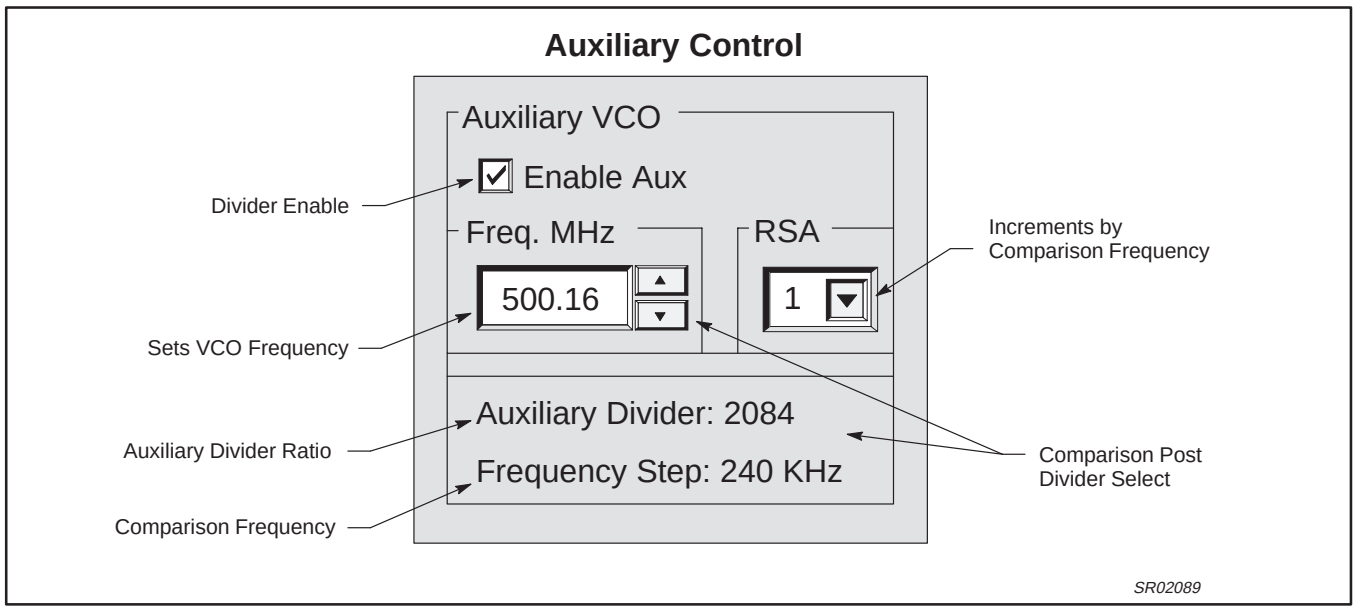


Figure 96. Auxiliary control

The auxiliary VCO controls operate in much the same way as the main VCO, with the exception that there are fewer of them.

Figure 97 shows the location of the charge pump control. There are only two items to control in this function. The rest is devoted to a calculator for the R_{SET} resistor. FDAC and CP ratio are the two active controls. FDAC controls the fractional spur compensation DAC while CP ratio controls the pump current ratios.

R_{SET}, I_{SET} and I_{PHP} are all interrelated. That is, when one is changed, the other two will be recalculated. CP ratio, when changed, will redisplay the new values in the I_{PHP}, I_{PHP-SU}, I_{PHI} and I_{PHA} fields. Refer to the SA8026 data sheet for the CP settings.

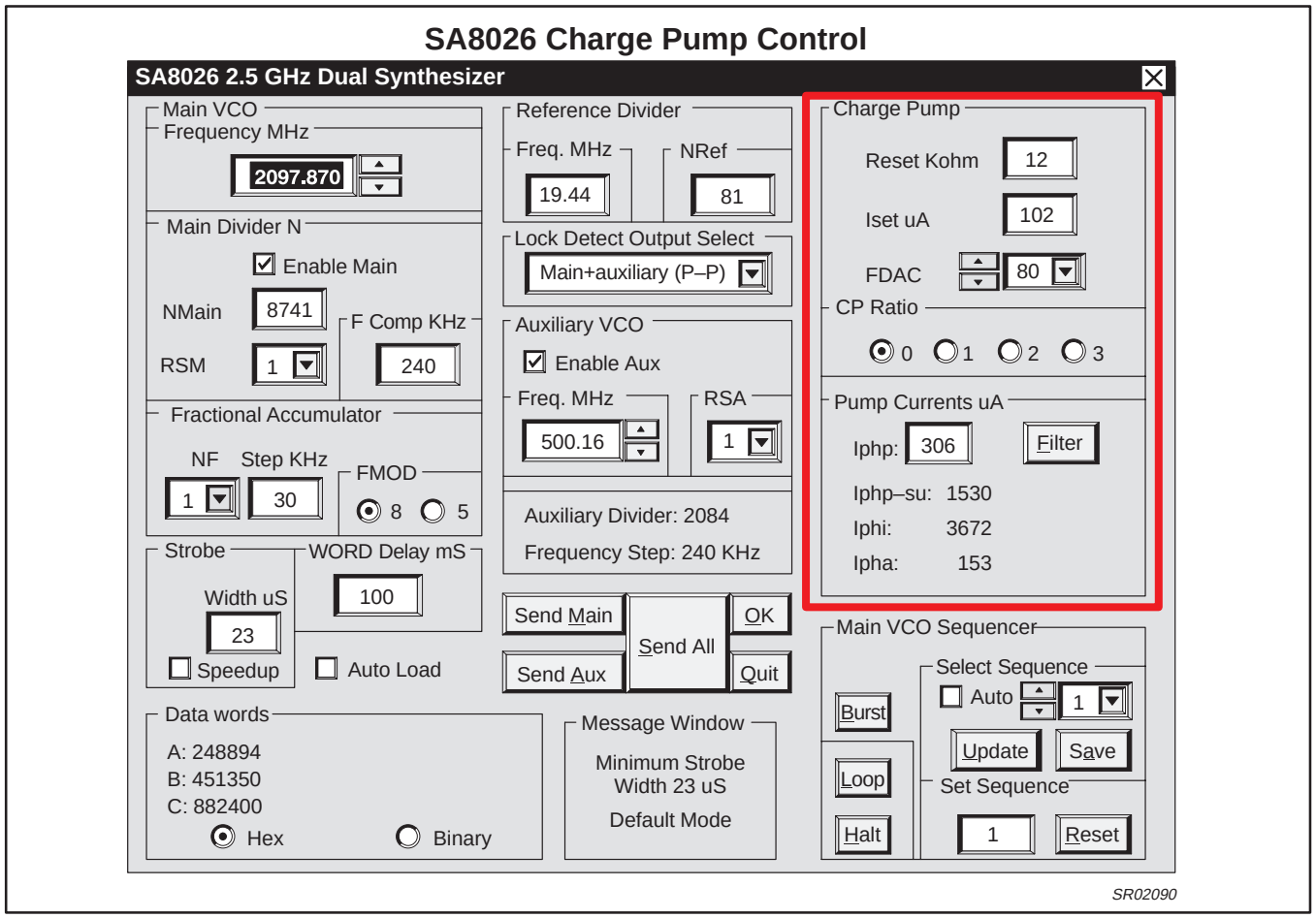


Figure 97. SA8026 charge pump control

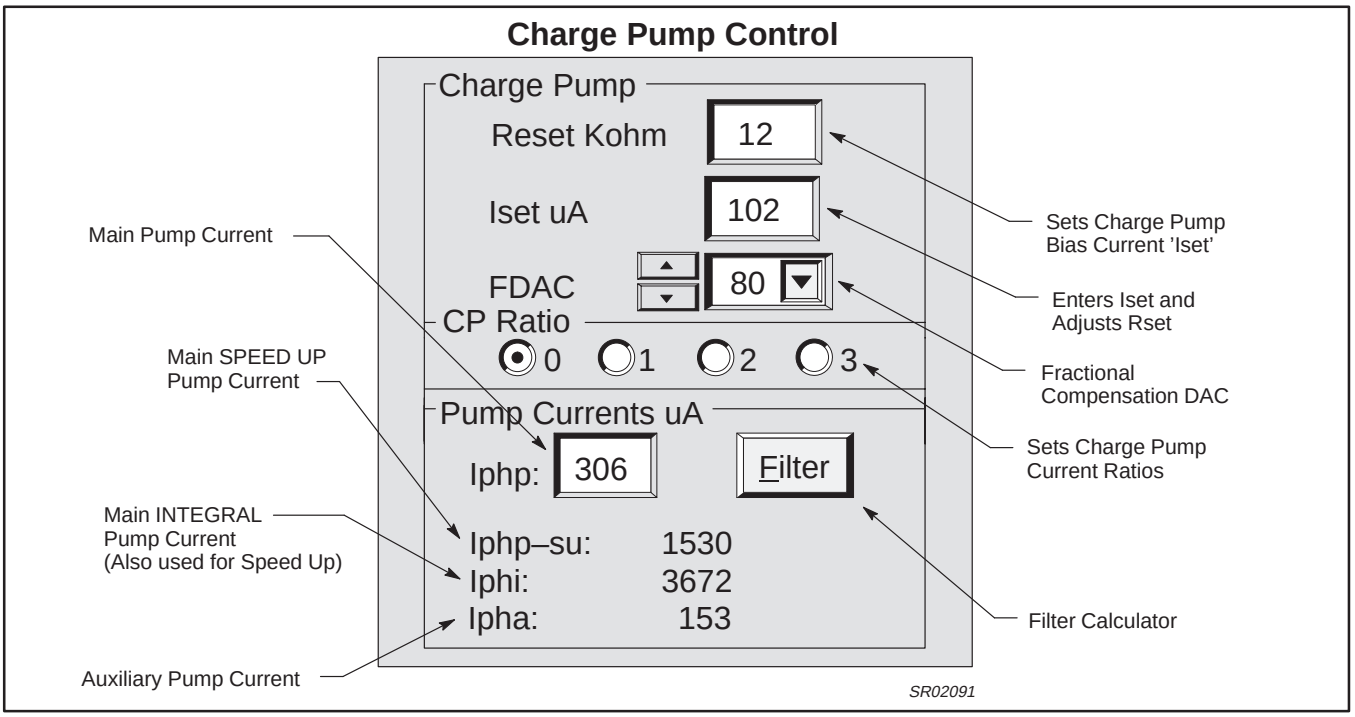


Figure 98. Charge pump control

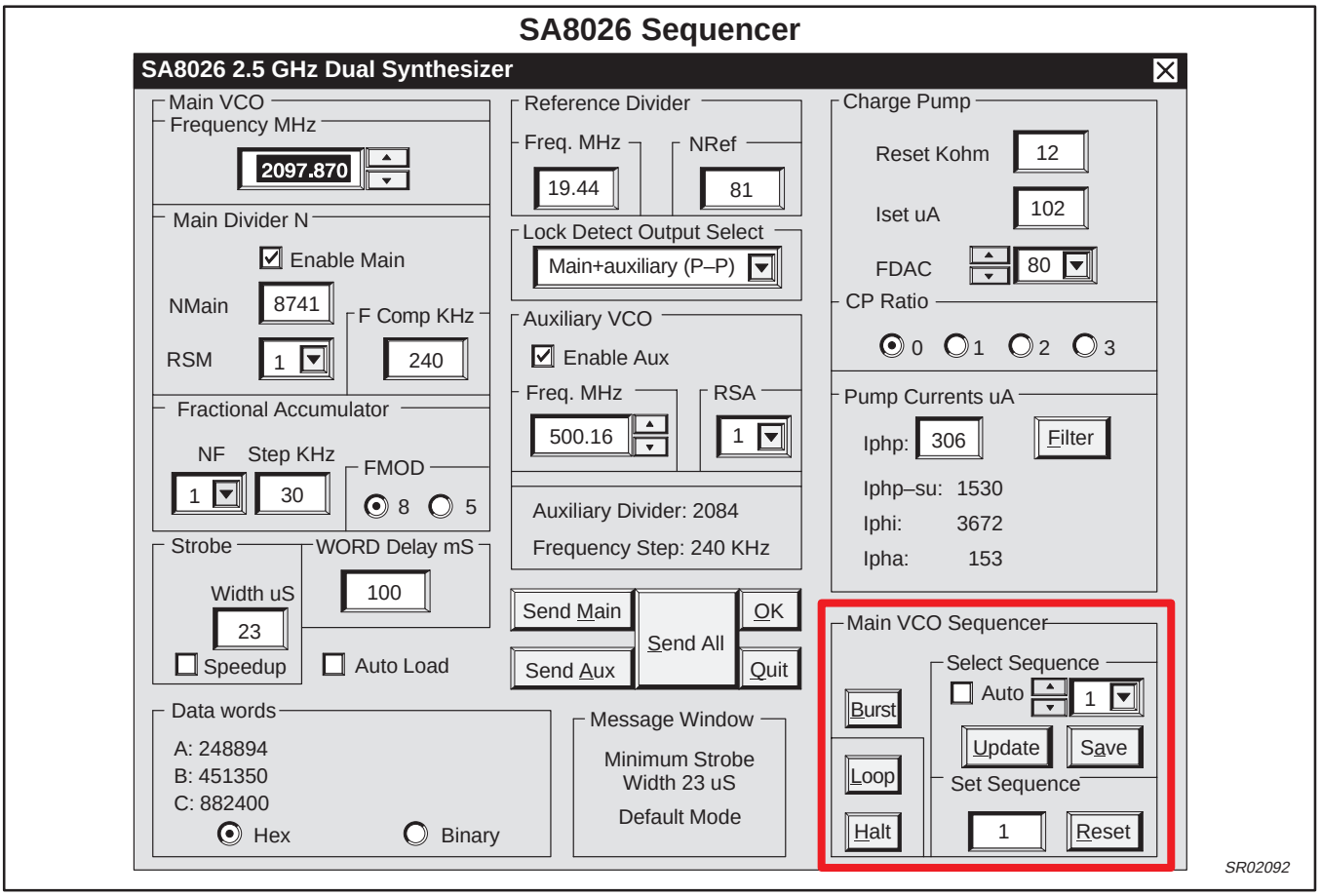


Figure 99. SA8026 sequencer

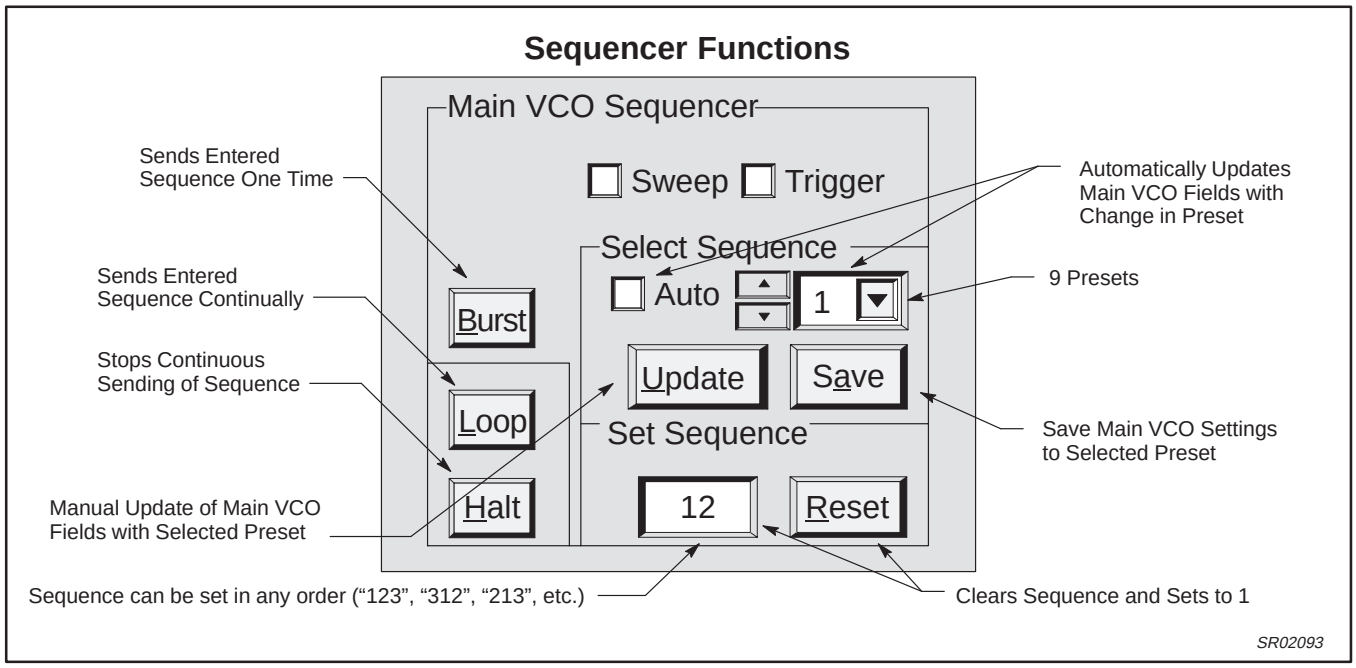


Figure 100. Sequencer functions

Two new controls have been added for greater flexibility of the “Main VCO Sequencer”. These new controls, named “Sweep” and “Trigger”, can extend the testing of the synthesizer by sweeping the frequency between a start and finish frequency or by stepping from one to the other. “Trigger” is used to issue a trigger pulse to a “Modulation Domain Analyzer” on the second frequency stored in the sequencer for measuring settling time. This helps to lessen the confusion of the instrument should a trigger be issued for both frequencies. The instrument will not read correctly or, if averaging is used, it will try to average both frequencies. This is not desireable as the frequency of interest in this case is only the second frequency entry.

The trigger pulse will be issued on the interface card labeled “TXEN”. This is a function that is not used for the SA8026 family and can be used to advantage here.

To set up the sequencer for either of these functions, enter in the “Main VCO” (see Figure 94) the start frequency and save it in position “1” of the sequencer. Then select the second frequency of interest and enter “2” in “Set Sequence” of the sequencer. The “Set Sequence” window will have to have sequence “2” entered so that the sequencer will know of the second frequency limit that has been stored. Click on “Loop” and the sequence will be repeated until halted.

Some Modulation Domain Analyzers like the HP 53310A may not have the resolution to give a good readable measurement with one trigger. The trigger function used in conjunction with the averaging function of the instrument can be used to advantage.

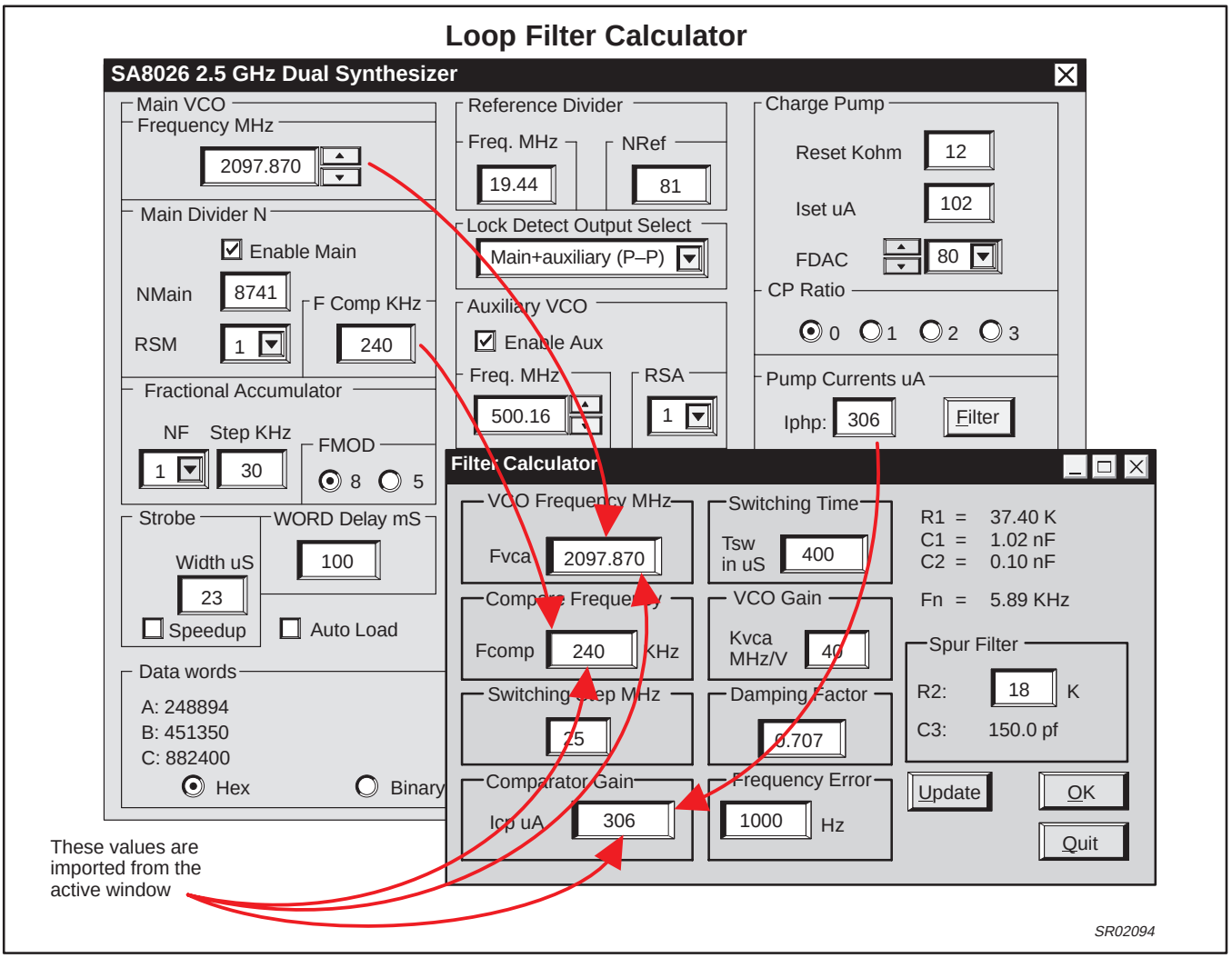


Figure 101. Loop filter calculator

Frequency and main comparison pump current, I_{PHP}, are imported when the filter calculator is enabled.

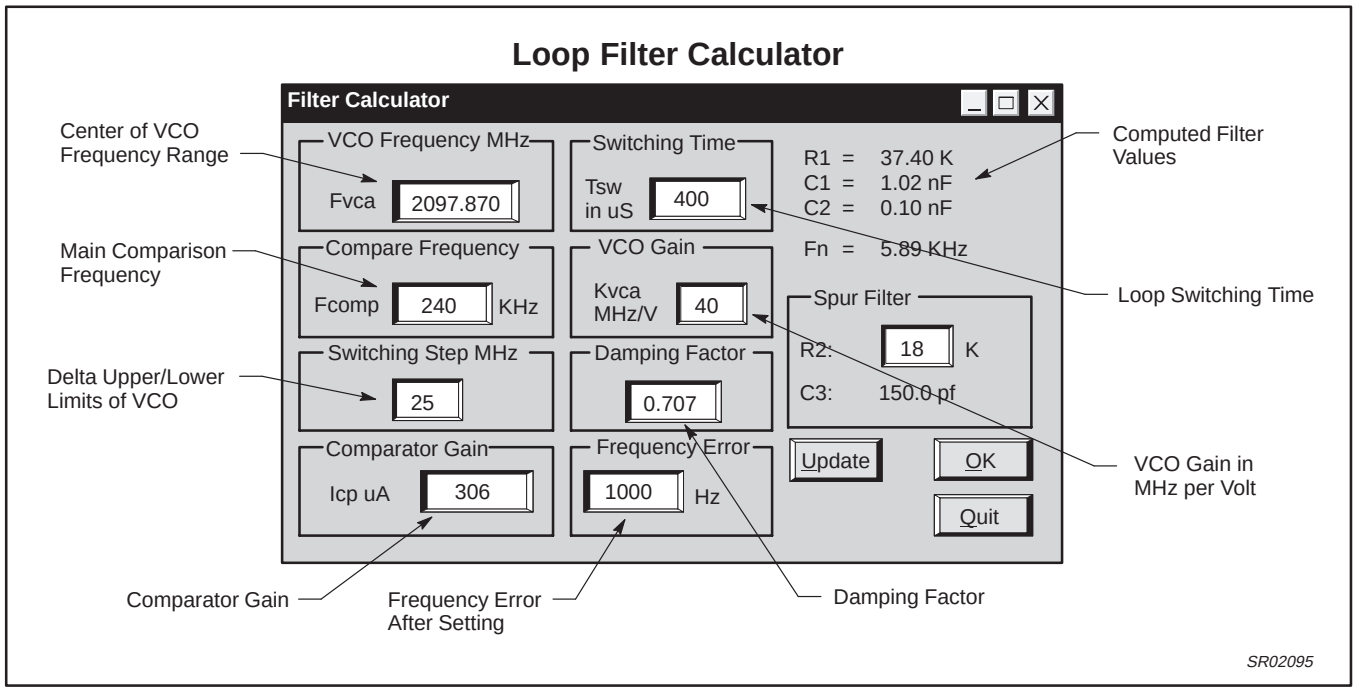


Figure 102. Loop filter calculator

For an explanation of the terms and calculations, as well as the location of the component references, refer to the section on design examples.

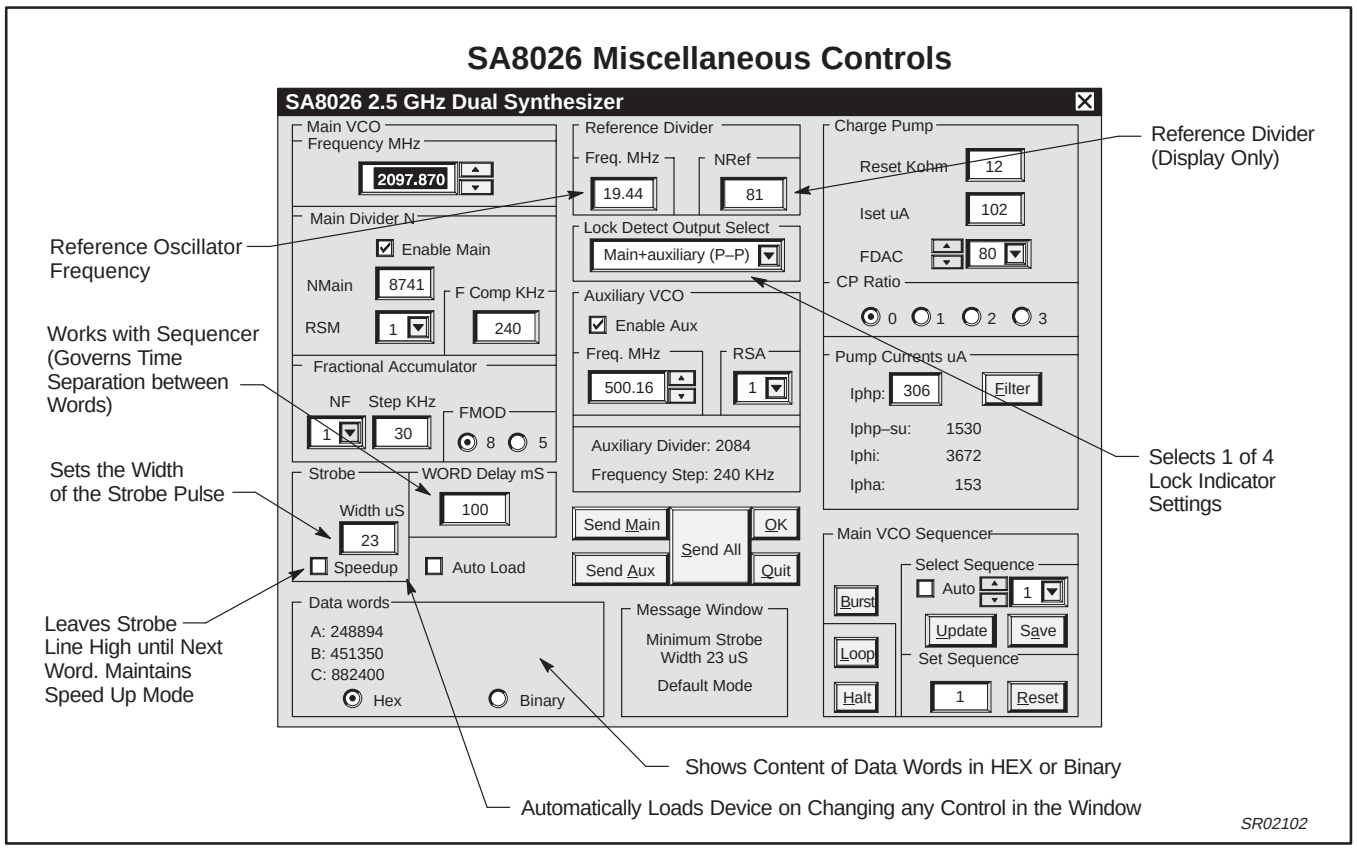


Figure 103. SA8026 miscellaneous controls

SA8026/7026/8016/7016
Low voltage fractional-N dual frequency synthesizer

AN1893

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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