# APPLICATION NOTE

## AN182

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

1991 Dec

Philips
Semiconductors

PHILIPS

# Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

# AN182

## INTRODUCTION

In order to obtain a local clock signal in Multiplexed Data Transmission systems, a phase and frequency coherent method of signal extraction is required. A Master-Slave system using the quartz crystal as the primary frequency determining element in a phase-lock loop VCO is used to reproduce a phase coherent clock from an asynchronous Data Stream.

The NE564, a versatile phase-locked loop (PLL) operating at frequencies of 50MHz, has inputs and outputs designed to be TTL compatible. The Philips Semiconductors NE564 is used to generate the phase-locked, crystal-stabilized clock reference signal.

Its particular adaptation, for use with a crystal-controlled VCO instead of the usual RC control elements, requires a brief review of the principles of the Phase-Lock Loop design.

The NE564 Phase-Locked Loop is a fully contained system, including limiter, phase detector, VCO, DC amplifiers, DC retriever and output comparator (reference Figure 1). For the clock regeneration system to be discussed, the portions of the NE554 implemented are the input limiter, phase detector and VCO.

The signal limiter amplifies low level inputs (until saturation is reached, which is typically 60mV$_{P-P}$ for the NE564). The signal limiter output is fed to the phase detector, where the "unknown" input is compared to the "known" VCO frequency of the NE564. The differential error signal that is generated is fed through a DC amplifier and a voltage-to-current converter. The change in the current generated forces the VCO frequency to vary in its frequency and/or phase relationship, such that a $\theta$ of 90$^o$ lagging is obtained (the actual phase relationship may be somewhat less than 90$^o$ depending upon the $K_dK_O$ (gain) product of the NE564 at the operating frequency and bias current). The external filtering incorporated at Pins 4 and 5 control the dynamic frequency response and loop stability criteria.

The NE564 is a first order system; therefore, the use of single capacitors (at Pins 4 and 5) will automatically create a "second-order" system. An RC series filter combination will cause a lead-lag condition that will permit dynamic selectivity, along with closed-loop stability.

## LOOP GAIN FUNCTIONS

The phase detector conversion gain ($K_d$) and the VCO conversion gain ($K_O$) determine, in large part, the lock range, capture range and linearity characteristics of the NE564. These device parameters are both dependent upon bias current and operating frequency. Some typical curves for each of the parameters are shown for the NE564 in Figures 2 and 3.

## CLOCK REGENERATOR CIRCUIT

The basic building blocks of the clock regenerator circuit are shown in Figure 4. The PLL is shown as a frequency multiplier incorporating a divide by "N" in the VCO phase detector feedback loop. The functions of the ringing circuit and the NE527 high-speed comparator will be discussed later.

The waveforms of Figure 5 indicate the waveforms transmitted over a T1 line. The bipolar signal transmitted has "no" DC components induced in the transmission line (reference should be made to the effect of normal mode and common effects on signal information). When transmitted over telephone wire pairs, the resultant signal (at the receive end) will have been degraded in both waveshape and signal-to-noise ratios. Typical attenuation factors for a T1 line are -30dB per 6000 feet. In addition, pair-to-pair crosstalk can degrade signal-to-noise ratios. The energy transmitted in the bipolar system of signal transfer is centered at 772kHz (generated by the bit format).

At the receiving end the bipolar signal information is converted to a unipolar pulse train after being amplified, filtered and fed through an automatic level control circuit. Some types of PCM systems use the rectified and filtered DC (average) to control the phase of the regenerator clock; however, in newer systems, bipolar signals are processed (or preconditioned) by terminal common equipment resulting in unipolar information.

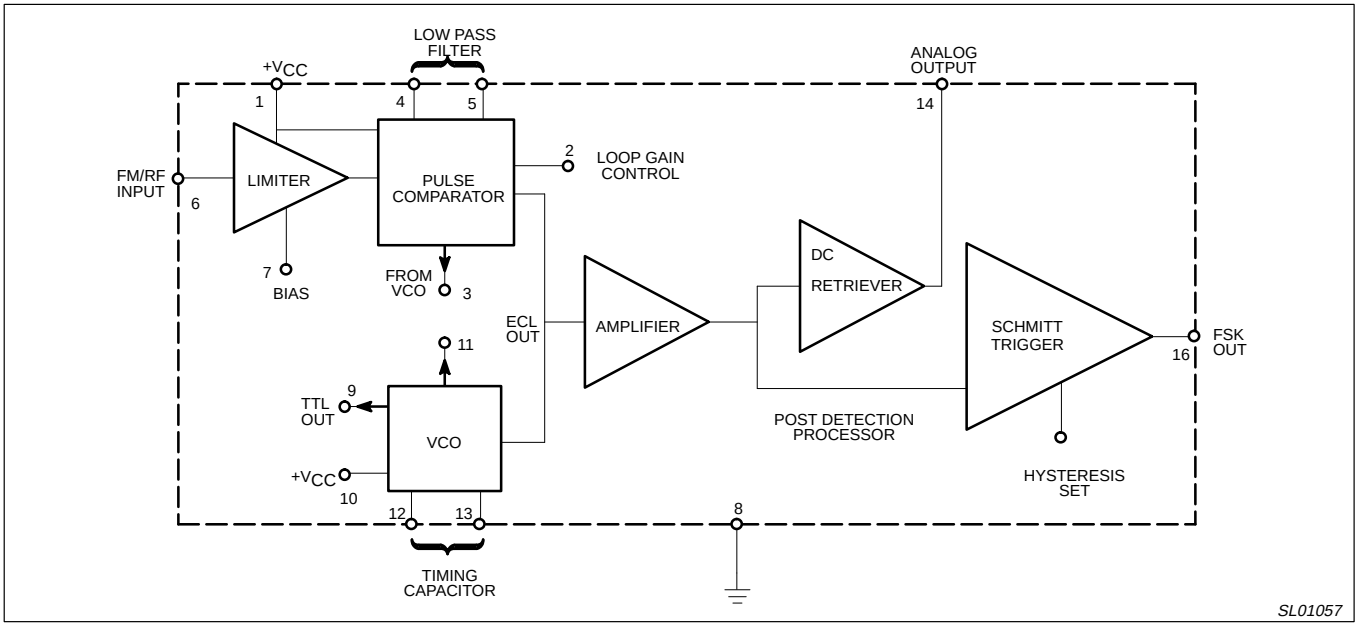


**Figure 1.**

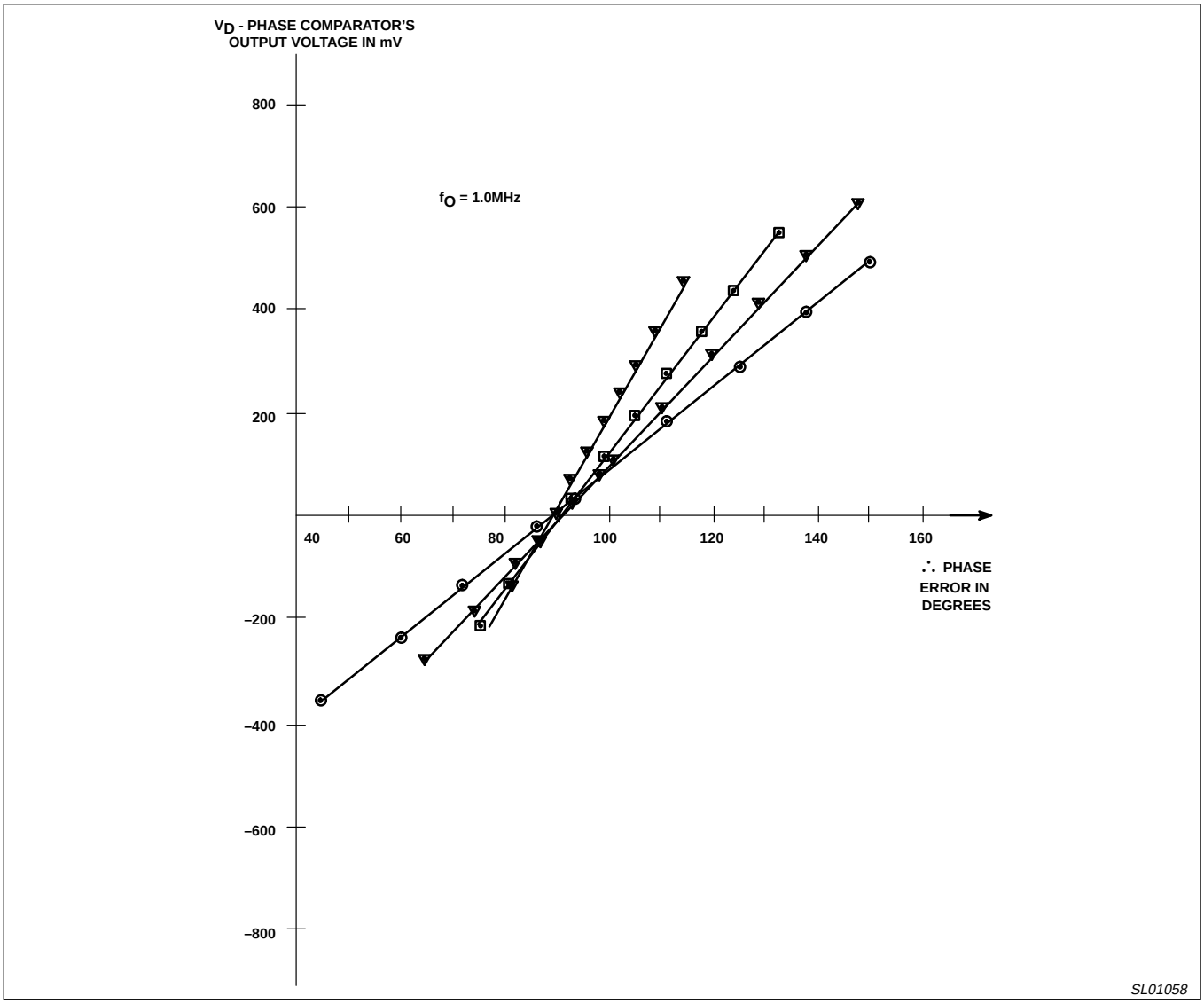


**Figure 2. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current**

# Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

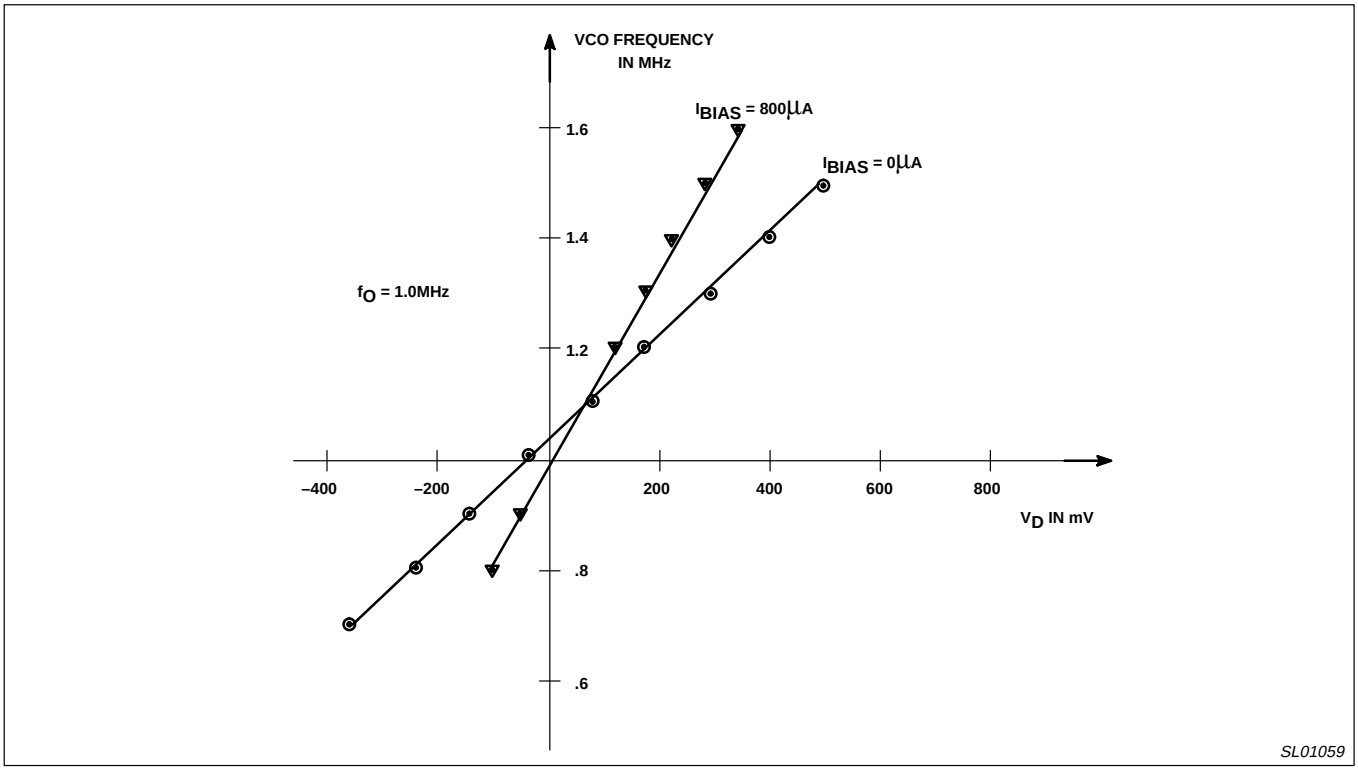


**Figure 3. VCO Output Frequency as a Function of Input Voltage and Bias Current**

## T1 Data Transmission

The bipolar signal, as transmitted on a T1 line, appears below with the original binary, converted unipolar and clock waveform (reference Figure 5).

The bipolar signal, when transmitted over standard wire pairs, will be degraded both in wave shape and signal-to-noise by the time it reaches the signal repeater. This is due to the attenuation factor of the cable which is nearly -30dB for 6000 ft. In addition, pair-to-pair crosstalk degrades signal-to-noise. The energy in the transmitted bipolar signal is centered at 772kHz due to the particular bit format. Bipolar signals have no DC offset.

At each receiving station the bipolar signal is amplified, filtered and fed through an automatic level control circuit. A full wave rectified signal is then sent to the clock regeneration circuit. This is essentially the format followed by some of the original T1 repeater equipment. The clock regeneration circuit described here could be adapted to this system.

## THE T1 SPECTRUM

The bipolar signal is similar to NRZ data in that it does not contain carrier information. In order to give the PLL coherent frequency

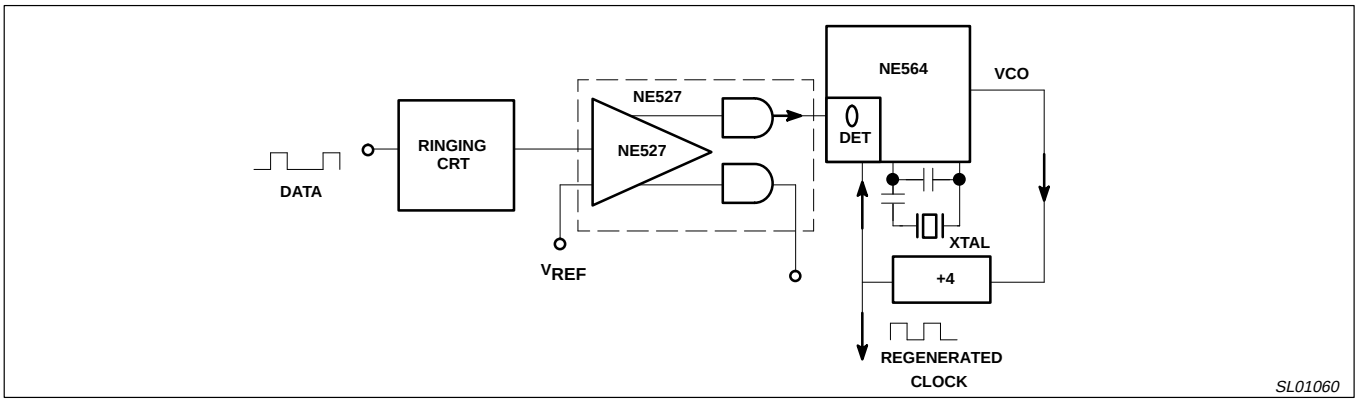


**Figure 4.**

information sufficient to obtain “capture” and lock, carrier components must be obtained from the data stream. The time duration of the frequency information fed to the PLL is also important in order to obtain accurate and stable information to update the PLL. In order to begin the extraction of frequency information, the positive-going portions of the bipolar data signals are used to drive a class “C” transistor tank circuit (reference Figure 4) which is sharply tuned to the basic clock frequency (1.544MHz). Each positive half cycle of data then starts a wave train of coherent information which is phase synchronous with each succeeding positive data bit. When the LC tank is optimally tuned, relatively extended periods without data bits can be tolerated with minimal loss of frequency and phase

information. The combination of good short-term frequency stability of the high “Q” LC tank, coupled with the long-term stability of the crystal-controlled VCO, is the foundation of the NE564 clock regeneration system accuracy.

It must be emphasized that dda pulse synchronization of the preprocessing circuit must be frequency coherent with the fundamental period of the time base to be extracted. That is, if the time period of the clock is $1/f_C = T$, where $f_C$ is the clock frequency, then the spacing between any positive code bit sequence must be n x t (reference Figure 6).

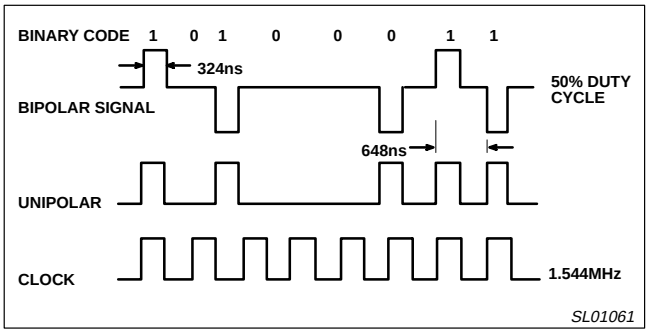


**Figure 5.**

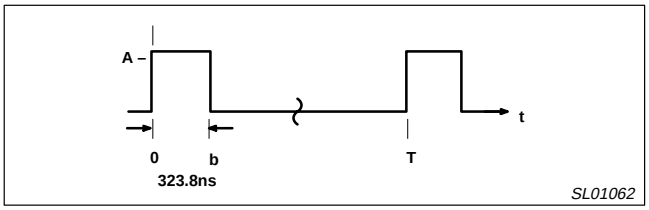


**Figure 6.**

Looking at the spectral analysis of the relative energy available to the clock extraction circuitry (with a worst-case duty cycle of 1 of 16) will demonstrate the need for enhancing the particular desired frequency component before applying the signal to the Phase-Lock Loop. For $f_O = 1.544MHz$, the period is T = 647.67ns. The pulse or bit width is 323.8ns.

Here the bit duration 323.8ns = b. The Fourier expansion of the discrete spectrum is related by the following equation:

(Ab)| sin(rt ) I Flnl T I n~iib In 0,1,2 (1)

The basic frequency component resulting from various bit spacing factors is defined by the equation

f = 1/T

If we consider the special case of a single pulse present out of 16 bipolar or 32NRZ periods, then

T = 16 bipolar bit times

= 16 x 647.67ns = 10.36ms

f = 96.5kHz

Accordingly, the spectral lines will be spaced in multiples of 96.5kHz. The spectrum for this particular worst case condition is shown in Figure 7 below.

It is evident that as the bit spacing increases to the point where $f_O$ is the 16th harmonic of the fundamental, very little $f_O$ energy is available to drive a phase-lock regeneration circuit. $F_{(16)}$ is also ineffective since it is an even subharmonic of $f_O$. The PLL will not normally lock to even harmonics, in fact, an error signal is produced which tends to force the VCO out of lock. This fact further stresses the need for preprocessing in the frequency domain. The class “C” pulsed resonant tank significantly multiplies the magnitude of the $f_O$ spectral component and filters out unwanted subharmonics.

The loop error voltage available from the phase detector for phase correction of the VCO is directly related to the product of the incoming coherent spectral energy multiplied in the balanced mixer with the reference signal derived from the VCO. Since the phase error information is integrated in the loop filters, the instantaneous magnitude of the DC error voltage is proportional to the time integral of coherent mixer products. Thus, as the magnitude and time duration of the desired frequency component is in creased in the preprocessing circuitry, the VCO phase accuracy is greatly improved. Capture time is obviously enhanced also.

The signal from the tuned tank is buffered by a FET follower N-channel enhancement mode device (reference Figure 12). This provides power gain with virtually no loading on the tank circuit and avoids degrading the “Q”. The buffered signal is then fed to a high-speed comparator (Philips Semiconductors’ NE527) which allows for waveform symmetry adjustment in addition to providing a standard TTL output to drive the NE564 PLL.

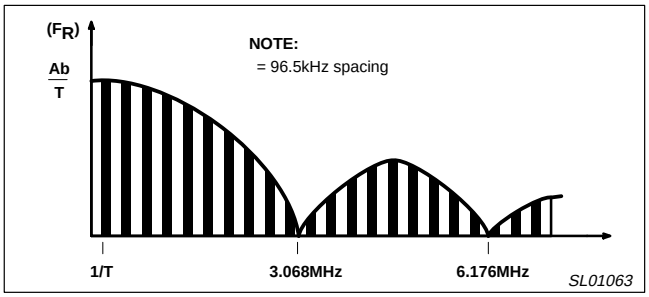


**Figure 7.**

In the particular circuit shown in Figure 12, the 1.544MHz information is applied to the phase detector input of the NE564 Phase-Lock Loop. The VCO, however, is operated at four (4) times this frequency in order to take advantage of economical and readily available crystals. The VCO signal is fed through a divide-by-four counter (74LS73) to provide the Phase Detector reference and final regenerated clock signal. To avoid loading, the clock signal (1.544MHz) is buffered by the 75451 peripheral driver which provides a high-speed open collector TTL output.. The input signal is AC coupled in order to reduce DC bias errors in the Phase Detector caused by “O” level variations.

## The Crystal

The crystal used was chosen to match the NE564 VCO drive characteristics. It is an “AT” cut oscillator crystal which operates near the anti-resonate or “parallel” mode in this circuit. The crystal may have to be fine-tuned, as indicated in Figure 8. The pulling characteristic of the crystal is adequate to allow for 0 to 70°C operational drift plus initial and aging accuracy tolerance factors and still retain lock between master and slave station VCXOs. The average lock range at room temperature with one of sixteen data bits present is typically 1000Hz for a 6.176MHz crystal with a capture range greater than 500Hz.

For VCO operation at 6.176MHz, $C_S$ is 22pF, $C_C$ is 18pF, and $C_t$, a 1 - 8pF trimmer capacitor (reference Figure 8).

## NE564 CRYSTAL-CONTROLLED VCO

As shown in Figure 6, the crystal is operated with a series capacitor. When properly trimmed, this allows the crystal to operate near the series resonant mode. A crystal manufactured to operate in the series resonant mode will do so only if it sees a pure resistance looking into the oscillator terminals. The circuit below shows an oscillator which looks inductive with the equivalent crystal circuit and trimmer capacitor $C_t$ (reference Figure 9).

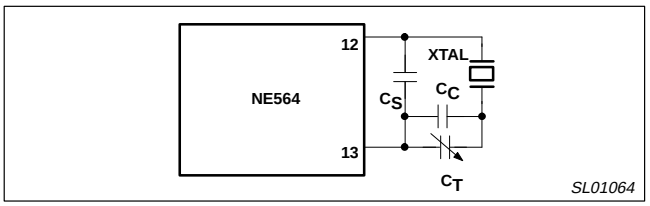


**Figure 8.**

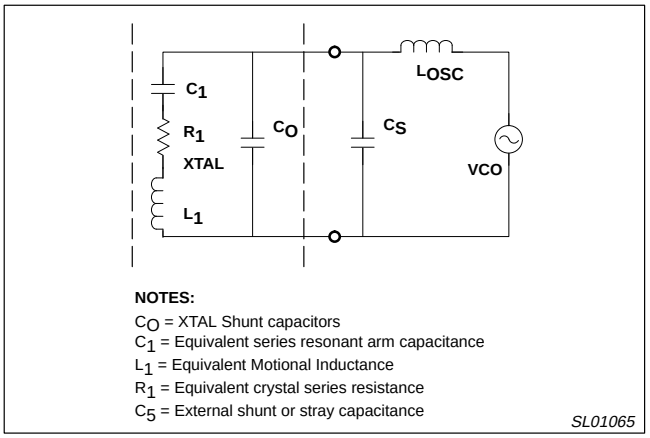


**Figure 9.**

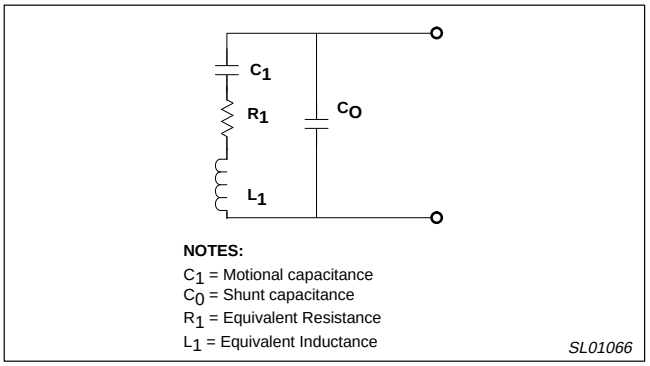


**Figure 10. Basic Crystal Equivalent Circuit**

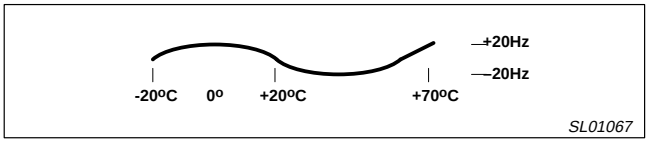


**Figure 11. Design Example**

If $L_O$ is small and the internal gain of the device high over a wide frequency range, $L_O$ may resonate with the $C_O$ of the crystal at a very high frequency. Under certain conditions the circuit may even tend to operate in the 3rd overtone mode unless measures are taken to roll-off the circuit gain. This is the purpose of $C_S$ in Figure 8. Since the gain or the VCO is a factor in spurious oscillation, the current injected into Pin 2 will also have an effect in this respect. ($K_O$ increases with $I_2$). At higher operating frequencies this parameter may become more critical in attaining stable start ups in the desired frequency mode. Obviously the size of $C_S$ must be smaller than the value needed to cause free running near the desired frequency without the crystal connected.

## CRYSTAL SPECIFICATION

Crystals may be manufactured to operate in either the series mode with no external capacitance (purely resistive load) or in the parallel mode with a specified value of load capacitance. The 564 tends to operate at a frequency above the specified value when a series mode crystal is used, for a design frequency of 6.176000MHz and zero load capacitance. Referring to Figure 8, for $C_S$ = 10pF and $C_T$ = 10pF the average center frequency for an NE564 sample measured in the lab was 6181.192kHz. For the same $C_S$, but with $C_T$ equal to 60pF, $f_O$ measured 6176.565kHz. A second crystal showed a spread of 6176.600kHz to 6160.855kHz. The effect of the VCO was to pull the crystal to a frequency above its design value. This effect is then nearly tuned out by the external capacitances $C_S$ and $C_T$. If $C_T$ is sufficiently increased, the crystal will see a purely resistive load and operate at its rated frequency.

A second approach is to specify a crystal which is to operate near the anti-resonate or parallel mode. Normally this is done with a certain value of external load capacitance specified by the customer which matches the existing circuit parameters. The maximum difference between series and parallel resonance for any crystal is 0.5% of $f_O$ (series resonant mode); for $f_R$ = 6.126MHz, 0.5% of $f_R$ = 30kHz. The usual value would be lower than this.

$r_O$ = electromechanical coupling factor, $f_a$ = parallel resonant frequency). The particular cut of the crystal material determines the drift response over temperature. For oscillator applications, the AT cut offers the best over-all stability over a wide frequency and temperature range. Final design uses second approach.

For a stability or total tolerance of ±15ppm over the rated operating range of -20°C to +70°C, a certain manufacturer's crystal actually performed as shown above (Refer to Figure 11).

Calibration accuracy is the allowable frequency tolerance at the reference temperature, i.e., +10ppm @ 25°C.

Third, is a long-term drift spec which determines the customer's maximum allowable drift due to aging effects. An acceptable value in quality crystals is +2ppm/year.

Using our reference crystal of 6.176MHz and the above specifications, the crystal limits over a 1 year period would be:

Temperature stability: ±15ppm x 6.176 = ±93Hz

Calibration tolerance: ±10ppm x 6.176 = ±62Hz

@25°C Long term drift: ±2ppm x 1 x 6.176 = ±12Hz

Total: (+ 1 67Hz)

The above figure of ±167Hz then determines the capture and lock range over which two crystal stabilized VCOs must track under worst case conditions when the exact same crystal specifications are used for master and slave units within an operational system.

## Crystal Specifications

### 'AT' Cut Oscillator Type

Fundamental mode operation HC-33 Case (Standard)

Calibration tolerance: ±15ppm @ 25$^{o}$C

Temperature stability: ±15ppm; -15$^{o}$C to +65$^{o}$C

Circuit operating condition: Parallel resonance

Frequency specified: 6.176000MHz

Part designation: Croven #A330 DEF-32 or equivalent

### Setup Procedure

Referring to Figure 12 the following setup procedure will aid the user in establishing proper circuit operation.

Regulated supply voltage of +5V and -6V are required. Current drain on the +5V line is @100mA, and 6mA for the -6V.

With proper voltage applied, (1) First check the supply currents to be sure they are in the range indicated above. (2) Check the operation of the NE564 VCXO by looking at Pln 9 with an oscilloscope (see Figure 13). A reasonably symmetric square wave should be present having a frequency near 6.1MHz. (3) Attach a DVM across the 2k resistor which feeds Pin 2 of the NE564 and adjust for a reading of 2.00V, indicating a 1mA$_{DC}$ current flowing into Pin 2 (The (+) lead of the DVM should be connected to the end of t he 2k resistor which ties to the wiper of the 10k pot and the (-) lead to Pin 2 of the 564; reference Figure 14). (4) The exact center frequency is set by adjusting $C_t$, the crystal trimmer cap, for exactly 6.176000MHz with no signal input (this sets the center frequency of the VCXO to free-run in the center of the capture range). (5) Enable strobe 'A' and 'B' with a +2.7V min. to +5V max. level. Apply a standard 1.544Mb/s NRZ data signal to the input terminal terminated in 50W. The amplitude should be +3 to +5V (0 to peak). Set the duty cycle for 1 bit in a 16-bit period. Note the data generator must be driven from a crystal-controlled master oscillator also adjusted for a center data rate of 1.544000Mb/s. Monitor the buffered output of the ringing circuit with a scope connected to the source of the SD213 (Figure 15). The waveform should appear as in Figure 17. (6) Adjust tank trimmer cap $C_T$ for a maximum amplitude and note that the cycle period should be 647ns. (7) Now monitor the comparator output signal at Pin 7 and adjust $R_t$ for a 50% duty cycle. The same signal will appear at Pin 5 of the NE527 except it will be inverted. The signal on Pin 7 of the NE527 and Pin 6 of the NE564 should appear as shown in Figure 19. Now attach one lead of a dual-trace scope to Pin 7 of the NE527 and the other to Pin 3 of the NE564 as shown (Figure 16).

The two signals should be in phase-locked with an approximate 90$^{o}$ differential as shown in Figure 20 (data signal applied to @ 1.544Mb/s). If lock does not occur a slight trimming of the crystal trimmer CT should connect for slight differences in master-to-slave crystal tolerance. It is recommended that master and slave crystals be of the exact same design and specification to insure optimal tracking over time and temperature. A recommended manufacturer and part number appears at the end of this application note for your convenience.

Once lock is attained, move one lead of the dual-trace scope to the buffered output of the 75451 Pin 3 leaving the other scope probe on Pin 6 of the NE564. The phase-locked waveform should appear as In Figure 25. If a data word generator Is being used, you may check overall operation for various bit patterns by synchronizing the scope trigger on the "end of word" pulse then observe the phase error effect as different combinations are fed in.

## PHASE JITTER

When operating with real-time data transmission, the PLL loop filters must be optimized to minimize regenerated clock jitter. A good grade of mylar capacitor is recommended as connected to Pins 4 and 5 of the NE564. A simple pair of shunt-connected loop filter caps of 0.33mF to 0.76mF was found to be adequate.

# Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

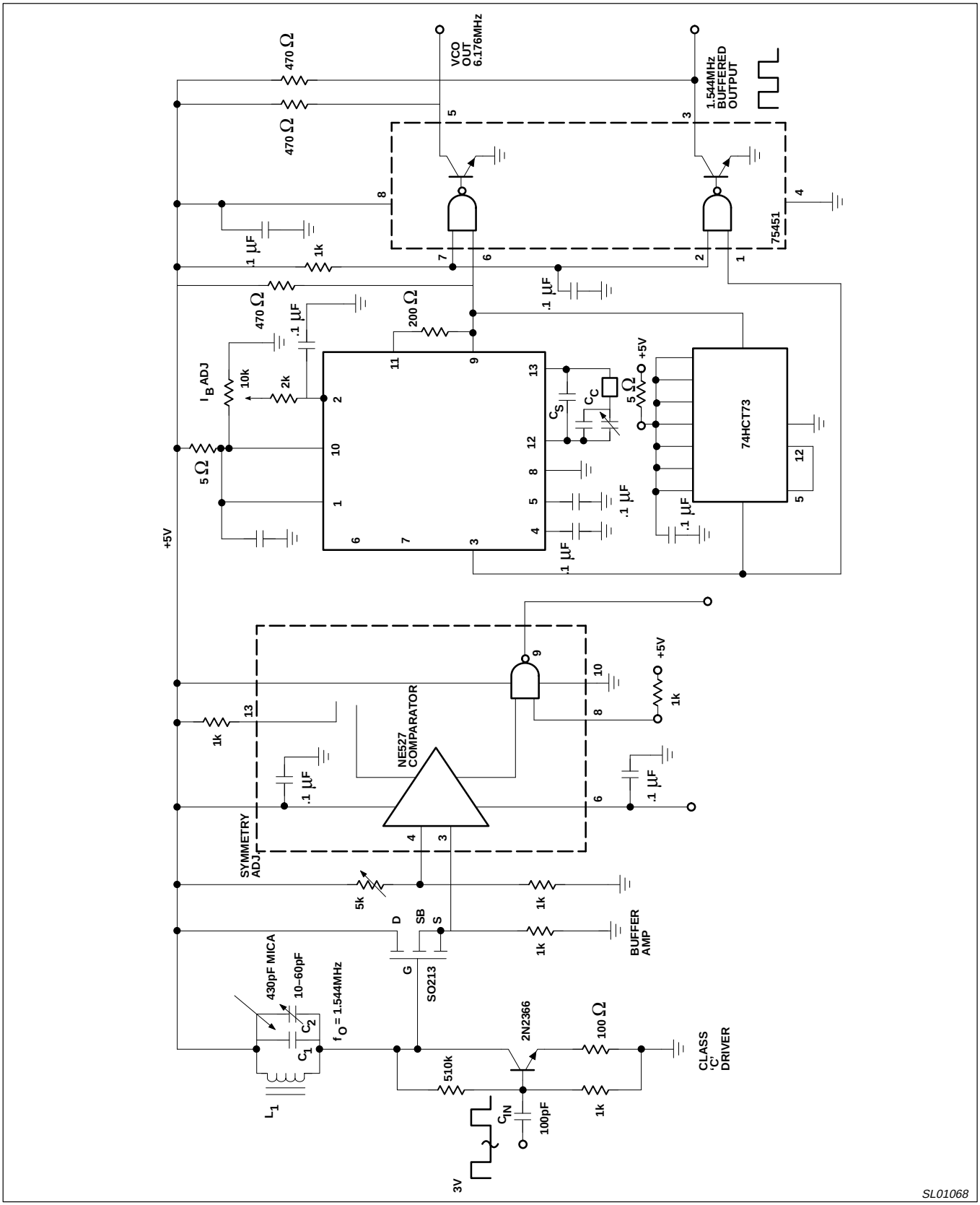


**Figure 12. Data Transmission System Clock Regenerator**

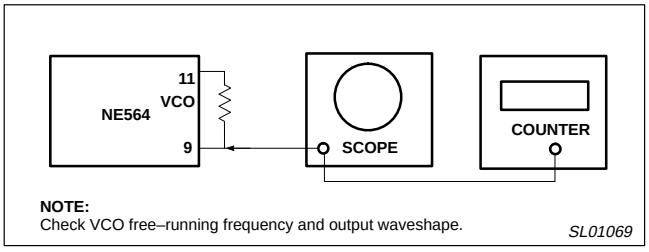


**Figure 13. Check VCO Free-Running Frequency and Output Waveshape**

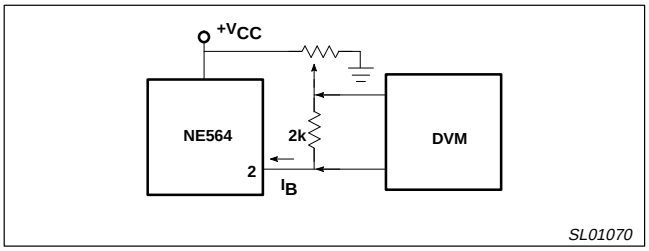


**Figure 14.**

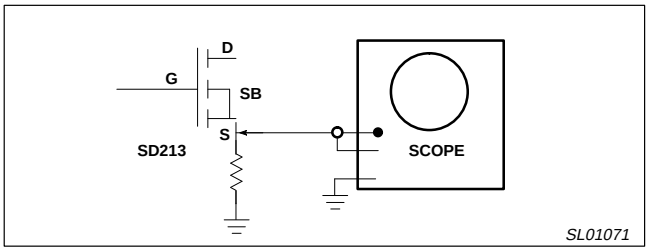


**Figure 15.**

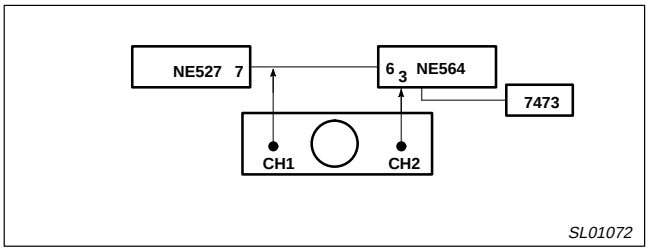


**Figure 16.**

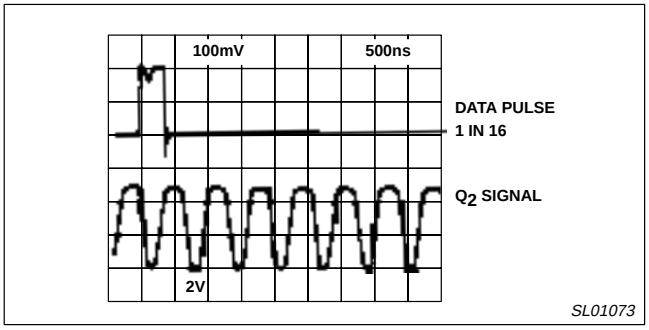


**Figure 17. Ringing Circuit Response (1 Data Pulse in 16)**

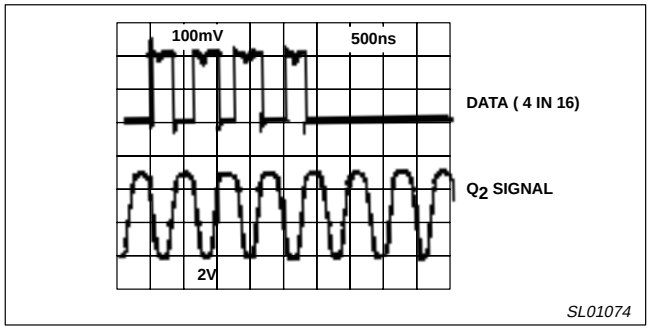


**Figure 18. Ringing Circuit Response (4 Data Pulse in 16)**

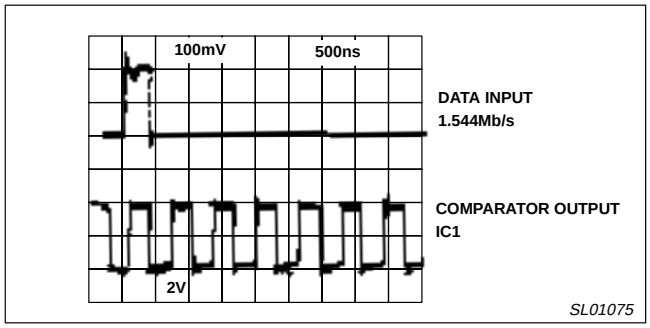


**Figure 19. Ringing Circuit to Square Wave Conversion**

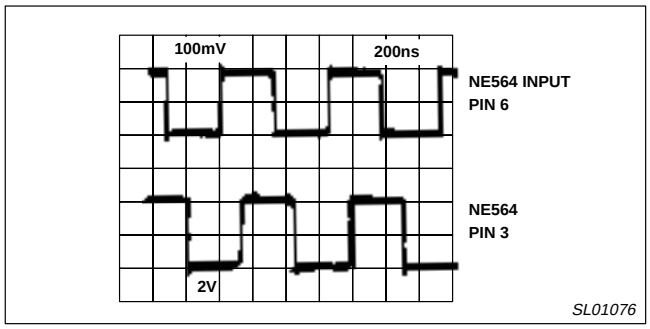


**Figure 20. Phase Comparator Signals (in Lock)**

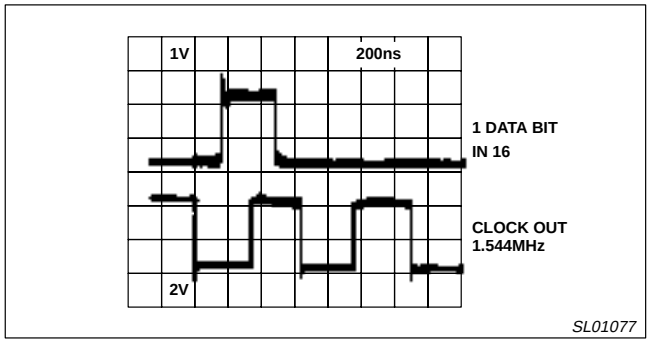


**Figure 21. Regenerated Clock Signals**

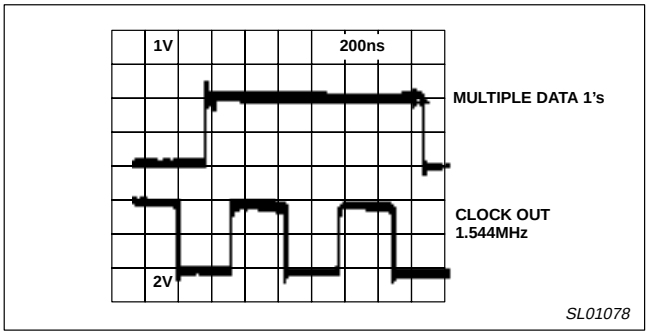


**Figure 22. Regenerated Clock Signals**

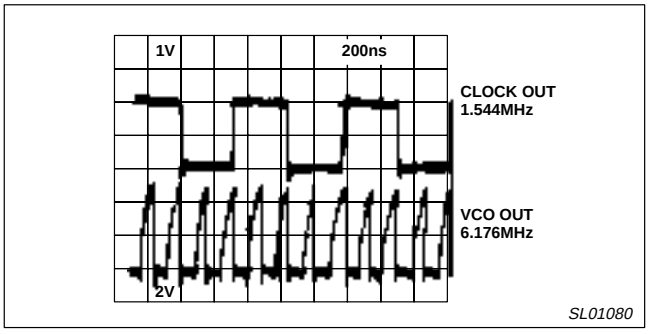


**Figure 24. Regenerated Clock Signal Relative to NE564 VCO Signal**

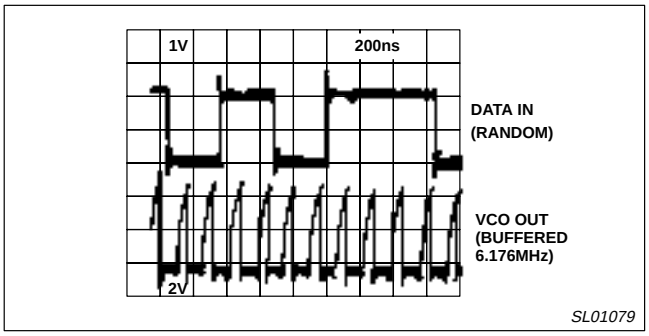


**Figure 23. Regenerated Clock Signals Relative to NE564 VCO Signal**

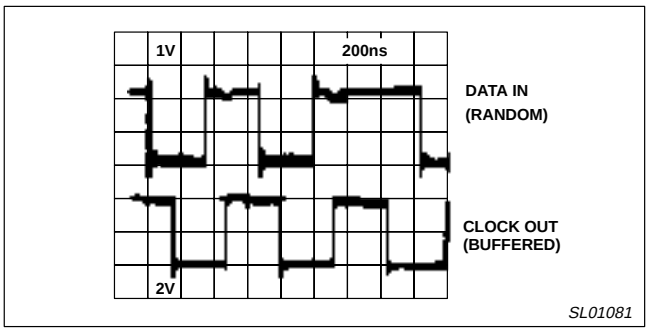


**Figure 25. Regenerated Clock Signal Relative to Random NRZ Data Signal**

**NOTES:**
1. Recent versions of this circuit no longer require series capacitors $C_C$ and $C_T$. See Figure 12.
2. Input levels to the NE564 have been reduced for this application to ≅ 800m$V_{P-P}$. See Figure 12.
3. Improved operation regarding clock jitter is obtained by carefully decoupling the divider counter ICs and the PLLs $V_{CC}$ line. This is accomplished by adding a small series "R" into the $V_{CC}$ line with the bypass capacitor to ground.

## References

1. "Fourier Analysis" by Hwei P. Hsu. Simon & Shuster Tech Outlines
2. "Pulse and Digital Circuits" by Millman and Taub. McGraw Hill
3. "Phaselock Techniques" by Floyd M. Gardner. Wiley, 1966