# APPLICATION NOTE

## AN181

A 6MHz converter design example for the NE564

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# A 6MHz FSK converter design example for the NE564 AN181

## Design Example

It is desired to design an FSK converter operating at 6MHz with deviation of ±1%. Supply voltage is 5V. Input to the 564 is from a radio receiver with an amplitude of $0.5V_{RMS}$. Worst case S/N is 10dB. An overall loop damping factor of 0.5 is specified ($\zeta$).

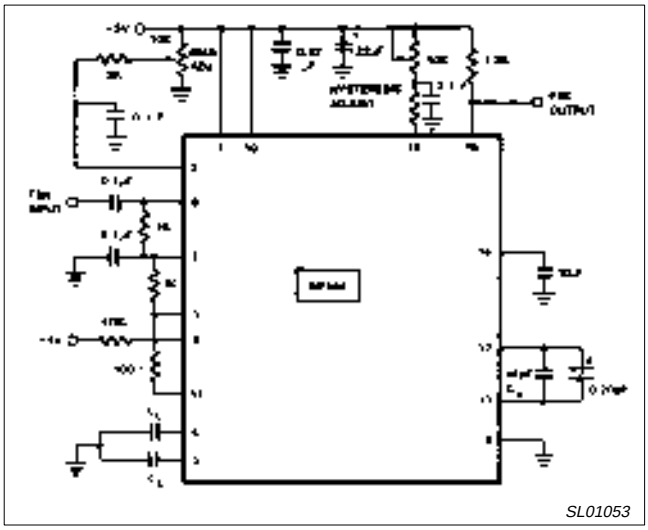



**Figure 1. FSK Decoder Using the 564**

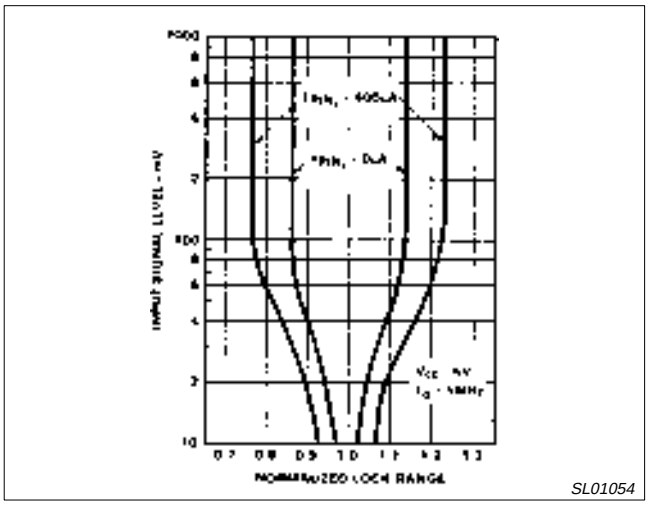



**Figure 2. Lock Range vs Signal Input**

**Using the circuit in Figure 1**

First the frequency determining capacitor must be established. Using the equation

$$f_O = \frac{1}{22R_CC_O}$$

where $R_C$ is the internal resistance in the VCO oscillator equal to 100Ω. Given two parameters the third is calculated $f_O$ = 6MHz; therefore

$$C_O = \frac{1}{22 \times 100 \times 6\ 10^6} = 75pF$$

A parallel 2 - 20pF trimmer and a 68pF ±5% fixed mica capacitor is chosen.

Next, signal level versus bias current and lock range is examined.

The signal input to the 564 is specified to be $0.5V_{RMS}$; in the lock range graph, the input level is well within the limiting region of the 564. Thus, no external AM limiter circuit is required and a 10dB S/N (3.1:1) min. should provide reliable communication with a narrow deviation of ±1% (±60kHz) and there is no problem with adequate lock range as it pertains to bias current. We are free to use any loop gain necessary. The bias current sinking into Pin 2 is set to an initial value of 200μA.

It's now possible to determine the damping factor of the closed–loop. First, the natural frequency of the loop is calculated from the relationship

$$\omega_n = \frac{\sqrt{K_OK_D}}{\tau} \quad (1.)$$

where

$K_O$ = VCO conversion gain in $\frac{\text{radians}}{\text{sec} \cdot \text{volt}}$

$K_O$ = Phase detector conversion gain in $\frac{\text{volts}}{\text{radian}}$

$\tau$ = loop filter time constant in seconds.

For $f_O$ = 6MHz and $I_B$ = 200μA, $K_O$ may be derived from Figure 3a by first constructing an extrapolated transfer line with slope one-quarter of the angle between the existing $I_B$ = 0 and $I_B$ = 800 plots.

Interpolation gives

$$K_O \approx \frac{1.48 - 1.25MHz}{0.4 - 0.2V} = \frac{\Delta f_O}{\Delta V_O}$$

Multiplying $\Delta f_O$ by $2\pi$ results in

$$K_O = \frac{1.45 \times 10^6 rad/sec}{0.2V}$$

$$= 7.2 \times 10^6 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$$

Next, using the $K_D$ graph (Figure 3b), ±1 radlan (–90° ±57°); i.e., $\Delta\theta$ = 1 radian, results in an output of 0.6V/rad.

Therefore, $K_D = \frac{0.6}{\text{rad}} = 0.6V/\text{rad}$ at $I_B$ = 200μA.

The value obtained for $K_O$ is for data taken at 1MHz and must be multiplied by 6 in order to find the correct value.

Therefore, $K_O = 0.6 \times 7.2 \times 10^6 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$

$$(6MHz) = 4.34 \times 10^7 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$$

$$K_OK_D = K_V = (4.34 \times 10^7)(0.6) = 2.6 \times 10^7$$

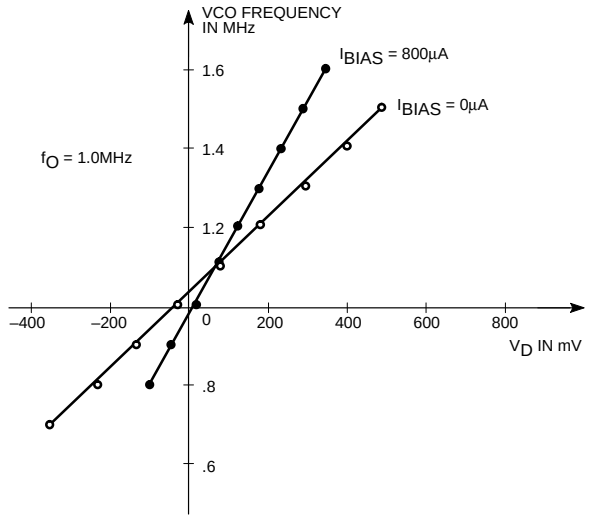
The damping factor specified (0.5) is now used to determine the necessary filter time constant (Pins 4, 5).

$$\xi = \frac{1}{2\pi\sqrt{\frac{K_OK_D}{\tau}}} = \frac{1}{2\sqrt{K_V\tau}} = \frac{\omega_n}{2K_V} \quad (2.)$$

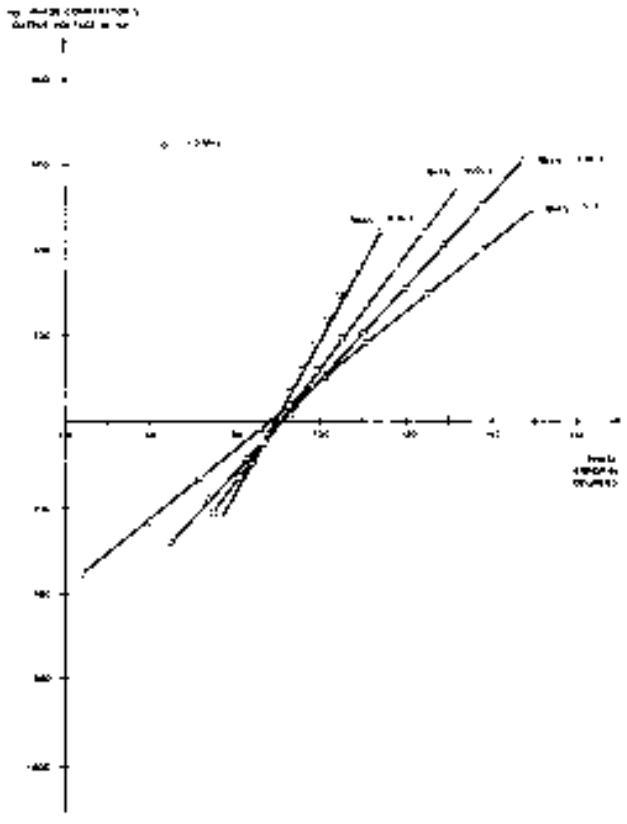
$$\therefore \tau = \frac{1}{(4)\ (2.6\ 10^7)\ (0.5)^2} = 38ns$$

Note that the filters on Pins 4 and 5 operate differentially with the net effect that break frequency is

$$\omega_p = \frac{1}{RC} \text{ (single pole filter – 3dB freq.)}$$




**a. VCO Output Frequency as a Function of Input Voltage and Bias Current ($K_O$)**



**b. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current ($K_D$)**

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**Figure 3.**

Now solving for $\omega_n$ using (1):

$$\omega_n = \frac{(2.6 \times 10^7)}{(3.8 \times 10^{-8})}^{1/2} = 26 \times 10^6 \frac{\text{radians}}{\text{sec}}$$

$f_n$ = 4.16MHz (natural frequency of the loop and approximate one–sided capture B.W.)

The value of the loop filter capacitor may be determined by dividing the time constant by the value of the internal resistance, 1.3kΩ.

$$C_L = \frac{\tau}{1.3k} = \frac{3.8 \times 10^{-8}}{1.3 \times 10^3} = 29pF$$

This value filter time constant will give a less than-critically-damped response allowing the fast excursion in VCO frequency necessary to good FSK reception. The tradeoff between response speed and carrier frequency harmonic rejection will have to be considered. A longer time constant gives more carrier rejection but slower response and less damping (Refer to equation 2).

The next step is to test the circuit under actual operating conditions with the specified FSK signal. The level on Pin 15 (hysteresis adjust) must be set in the vicinity of +1.4V in order to attain proper FSK demodulation. Final signal tests may be carried out with noise injected through a resistive summing network at the input (Pin 6) to simulate the 10dB S/N.

Note that the loop filter response actually operates on the frequency spectrum above (+) and below (–) the carrier center frequency, or center of deviation, for a symmetric FM or FSK signal. This may be seen in Figure 4.

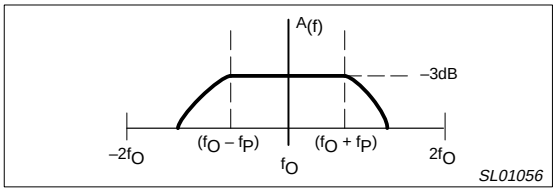


**Figure 4. Bandpass Effect of Loop Filter**