APPLICATION NOTE

AN1802

FM and FSK and BPSK demodulation using the Philips NE/SE564 phase-locked loop_demoboards

Author: L. J. Hadley

1995 Aug 25

Philips
Semiconductors

PHILIPS

FM and FSK and BPSK demodulation using the Philips NE/SE564 phase-locked loop demoboards

AN1802

Author: L.J. Hadley

INTRODUCTION

The new demoboard set for the NE/SE564 provides the capability for demonstrating three different applications: An FM demodulator for wideband analog signals; a data receiver for high speed FSK signals; and a simplified BPSK adaptation.

These particular boards use direct feedback between the VCO and the reference input to the phase detector and do not allow frequency multiplication. Both TTL and ECL VCO implementation are described herein.

The gain of the loop is set by the magnitude of the current, I_{BIAS}, sinking into Pin 2. The graphs of K_O and K_D (see data sheet) show the gain vs. bias current for the NE564 for a typical range of bias currents between 200 and 800 μA. Note that grounding Pin 2 will disable the phase detector, making an added function available to gate the phase detector on and off by using an external logic signal.

FM DEMODULATION

Using the demoboard as a simple FM demodulator is accomplished by feeding an FM signal into Pin 6 of the phase detector. Note that the phase detector has a voltage limiting function which reduces AM sensitivity for signals greater than 200 mV_{RMS}.

The signal-to-noise ratio of the FM demodulated signal is directly proportional to the frequency deviation of the input carrier. Note that the FM signal must track over the lock range of the device and this is dependent on the loop gain, K_V, which is controlled by bias current at Pin 2, as discussed above. The NE/SE564 is capable of handling carrier deviations of 40%, however, a deviation of ±20% is adequate to give superior performance with regard to the fidelity and signal-to-noise ratio of the demodulated signal. The demodulated analog output is present on Pin 14, but must be properly filtered in order to remove the mixer harmonics. This may be accomplished by the use of a simple low pass filter at Pin 14. The source impedance may be approximated as 10k in order to find the correct shunt filter capacitor. NOTE: An external buffer amplifier and active filter may also be used to provide better load matching and performance if required.

FM demodulator Example

A simple demodulator having a second-order loop filter is shown in Figure 1 below .

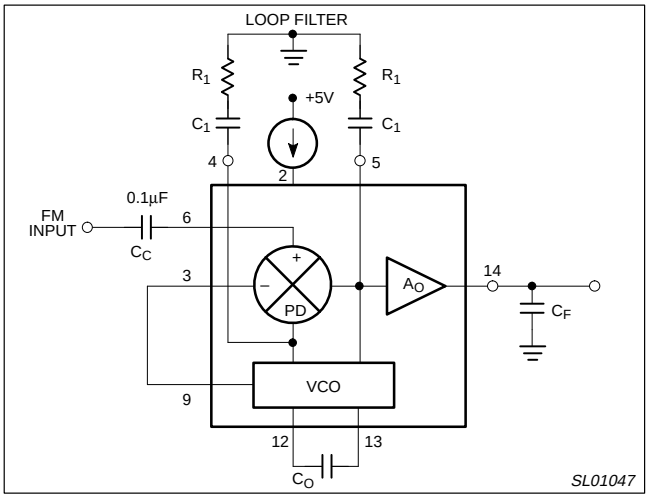

Figure 1. Loop Filter

The Loop Filter

The loop filter consists of the dual differential network labeled R_1, C_1 in Figure 1. In the example to follow, the VCO is operating at 20 MHz. The loop filter constants are chosen to produce a pole, f_P, at 1 MHz and a zero, f_Z, at 7 MHz. For this example the bias current sinking into Pin 2 is set to 500 μA. Figure 2 below shows the calculated closed loop response for a particular set of filter constants as described below.

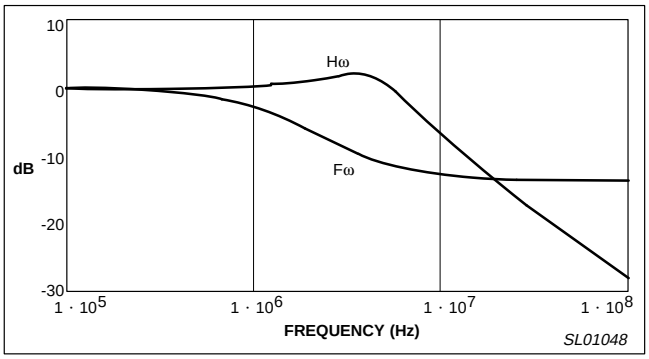

Figure 2. NE564 Closed Loop Response H vs Loop Filter F Transfer Function in dB

The natural frequency of the loop ω_n is calculated below using the loop filter resistor value for R_1 equal to 330 Ω and a capacitor C_1 of 100 pF:

$$\tau_1 = 330\Omega \cdot 100pF = 33ns$$

$$\tau_2 = (330\Omega + 1300)\ (100pF) = 160ns$$

$$\omega_n = \sqrt{\frac{K_V}{(R_1 + R_S) \cdot C_1}}$$

Loop Gain

$$K_V = \left[\frac{0.65V}{Rad} + 9.4 \cdot 10^{-4}\mu A \cdot \frac{V}{Rad}\right] \cdot \left[\frac{6 \cdot 10^6 \cdot Rad}{(V \cdot sec \cdot MHz} \cdot 20MHz\right]$$

$$= \frac{1.2V}{Rad} \cdot 1.2 \cdot 10^8 \cdot \frac{Rad}{V \cdot sec}$$

$$= 1.3 \cdot 10^8 \cdot sec^{-1}$$

Therefore,

$$\omega_n = \sqrt{(1.3 \cdot 10^8\, sec^{-1})}$$

$$(1.6 \cdot 10^{-7}\, sec)$$

Natural Loop Frequency = $2.9 \cdot 10^7$ Rad · sec^{-1}

and the damping is calculated as:

$$\zeta = \frac{1}{(2 \cdot \omega_n)} \cdot \frac{(K_V \cdot R_1 \cdot C_1 + 1)}{(R_1 + R_S) \cdot C_1}$$

$$= \frac{(1.8 \cdot 10^8) \cdot (4.3 + 1)}{(1.6 \cdot 10^{-7})}$$

$$= 0.46$$

Note that the damping constant is a strong function of R1 so that small adjustments in this external resistor allows the designer to tailor the transient response of the PLL receiver with one simple adjustment. For a majority of demodulator applications, a damping factor of 0.5 is considered optimum for the best signal-to-noise ratio.

Closed Loop Bandwidth as it Affects Baseband Signal Fidelity

In observing the graph in Figure 2, it is apparent that the Loop Filter response has both a pole and a zero. The pole is located by finding the -3 dB frequency of the response at the low frequency end, and then tracing down the slope to a point 3 dB above the plateau of the final portion of the curve. This locates the approximate position of the pole at 1 MHz and the Zero at about 7 MHz. It is the second-order pole-zero ratio that determines the degree of damping. A pole-zero plot in the s-plane could be used to solve the figure-of-merit graphically, as shown in application note AN178, Figure 6c of Philips Data Book IC11 (General Purpose Linear ICs). A vector drawn from the origin of the main axes to the circular locus of the roots will determine an angle whose cosine is the damping function. The length of the vector from the origin to the locus of the roots has the magnitude of ω_n, while the adjacent axis has magnitude $\cdot \omega_n$. Therefore, the quotient of the adjacent side and the hypotenuse is the damping factor.

FSK DEMODULATION-Digital Data Transmission

The NE564 is a general purpose phase-locked-loop demodulator for both linear and digital FSK data reception. By feeding an NRZ or RZ data signal into the transmission modulator, the FM carrier is forced to vary between mark and space frequency modes (bi-modal operation). The NE/SE564 is capable of the added feature of processing an FSK signal and generating a digital output from Pin 16 of the device. This is due to the presence of an internal Schmitt trigger which processes the Phase Detector output. In addition, there exists a DC retriever which precedes the Schmitt, and minimizes the effect of duty cycle induced threshold variation which can produce data errors.

Data transmission errors are affected by the signal-to-noise ratio of the input signal, as well as how the hysteresis voltage (Pin 15) is adjusted. An optimum setting is +1.45 V_{DC} (see AN181 in Philips Data Manual IC11 for details of a typical FSK receiver design, including how to determine the proper loop filter for best transient response).

PSK Reception

It is possible to receive PSK (Phase Shift Keyed) signals with the NE/SE564. However, external circuitry must be added to the device to complete the decoding processor.

As shown in the block diagram in Figure 3, the NE564 may be used as a carrier recovery processor to generate the phase coherent reference for the main phase detector of a BPSK (Binary Phase Shift Keying) receiver. With BPSK, each data transition causes the carrier to shift by 180°, while the frequency remains constant.

The pre-processing stage before the NE564 serves as a bandpass filter to allow only the carrier to pass, and as a frequency doubler plus an additional post-filter to remove the multiplier sidebands leaving only the 2f component. The NE564 then locks to the 2f component, at which point he output of the loop must be passed through a divide-by-two stage to return the original cos(ωt) signal.

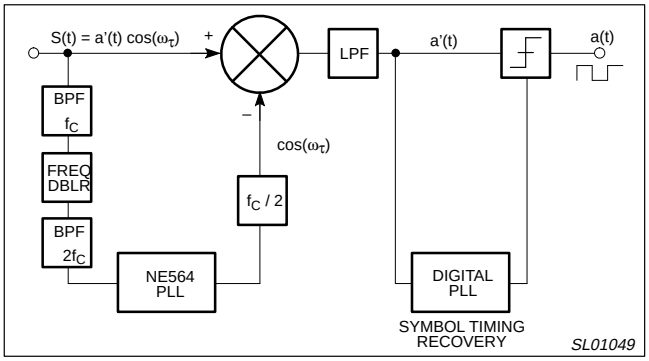

Figure 3. Coherent Demodulation Using BPSK (Binary Phase Shift Keying) and the NE564

The Use of TTL vs ECL Output Signals from the NE/SE564

Two VCO output signal stages exist within the NE564 circuit structure. Pin 9 output provides an open collector TTL compatible output port when this pin is pulled up to +5V through the proper load resistor. However, due to the lack of complimentary output drivers, the signal duty cycle suffers at higher frequencies. It is with this limitation in mind that an alternative circuit was tested using the ECL output port, Pin 11. Figure 4 below shows the modified circuit for implementing the ECL feature. A bias shifting network is required to provide proper termination for the open emitter output. This consists of a simple resistor network connected between +5V and ground which provides a low resistance potential reference of 3.9V to bias Pin 11. This equivalent to shifted ECL operation as used in standard 100kΩ and 10kΩ ECL circuit implementation (PECL).

The main advantage is evident in the VCO waveform duty cycle accuracy and excellent rise time integrity. This signal may be used to feed through a capacitive coupling network to the Phase Detector reference input, Pin 3, and provides good matching for the input signal from external signal sources. The double balanced mixer must have good duty cycle integrity for proper balanced carrier nulling, and this technique will improve this aspect markedly over the use of Pin 9 signal. There is a difference in the VCO free run frequency determination using the ECL reference. It will run at a somewhat lower frequency than stated in the data sheet, and will require a smaller capacitor on Pins 12 and 13 than predicted by the standard frequency determining equation.

FSK testing using the above ECL modification was carried out with good FSK output signals up to 1 MHz for a center frequency of 17 MHz, and a frequency deviation of ±25%.

The output signal from ECL Pin 11 may be fed through standard ECL logic buffers or can be converted to TTL with the proper converter IC. It is not necessary to convert the Pin 3 signal to TTL for proper operation of the Phase Detector. The AC coupled 700 mV_{P-P} signal is adequate for driving the Phase detector.

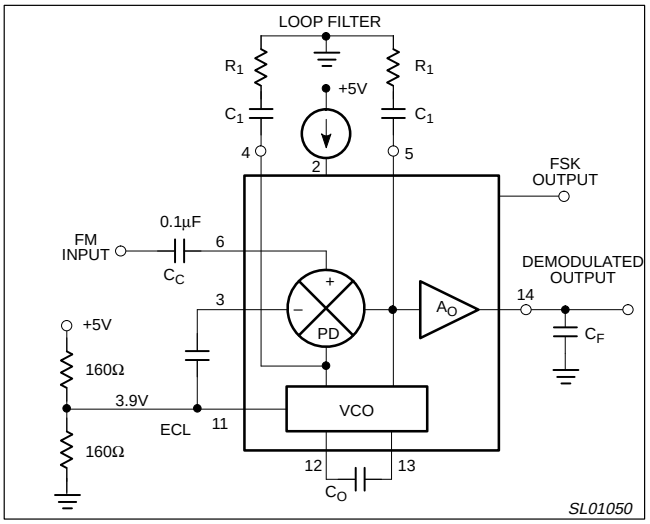

Figure 4. Using the ECL Output Signal

The Lock and Capture Range with ECL Coupled Phase Detector

The tested lock range measured for ECL coupling between Pins 11 and 3 is

10MHz f_{LOCK} 27MHz

and the capture range is

13MHz $f_{CAPTURE}$ 24MHz

For the standard TTL connection between Pins 9 and 3, the lock range measured

12MHz f_{LOCK} 27MHz

while the capture was essentially unchanged as is expected.

The ECL output waveform is shown below with no input signal into Pin 6 (Figure 5).

The FSK output signal waveform for a modulation frequency of 1MHz is shown in Figure 6.

The NE/SE564 can be connected for true ECL operation using -5.2V to the ground terminal, Pin 8, and connecting the 0V reference to Pins 1 and 10. The gain control pin must also connect with a dropping resistor between ground and Pin 2. The resistive termination is then connected between ground and - 5.2V, which results in Pin 11 having a static bias voltage of about -1.3V with respect to ground.

REFERENCES

Gardner, Floyd M., Phaselock Techniques; John Wiley & Sons, Inc.; The Wiley Monograph Series on Electronic Circuits, 1966, New York, London, Sydney.

Philips IC11, General-Purpose/Linear ICs: 1995, Philips Semiconductors, Sunnyvale, CA.

Proakis, John G., Salelhi, Masoud, Communication Systems Engineering; Prentice Hall, Englewood Cliffs, New Jersy, 1994.

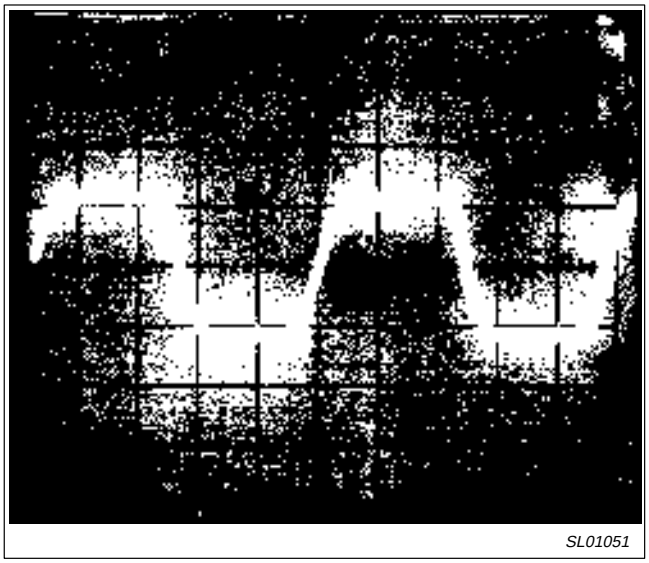

Figure 5. ECL VCO Waveform

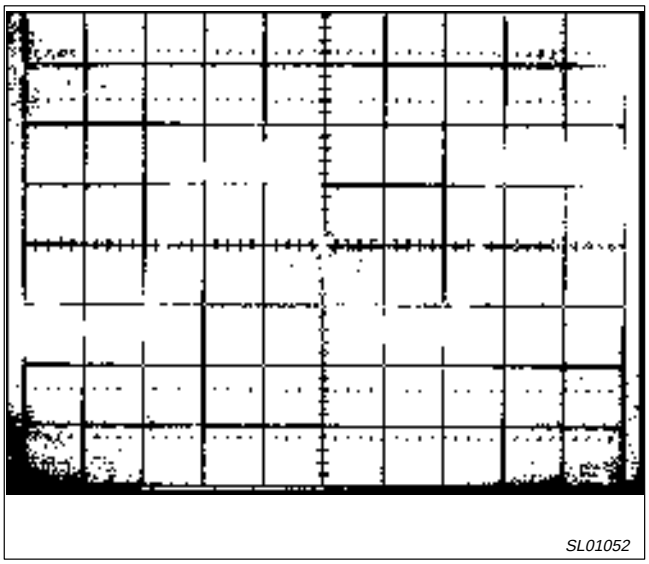

Figure 6. FSK Output Waveform from Pin 16