APPLICATION NOTE

AN179
Circuit description of the NE564

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DESCRIPTION

The NE564 contains the functional blocks shown in Figure 1. In addition to the normal PLL functions of phase comparator, VCO, amplifier and low-pass filter, the NE564 has internal circuitry for an input signal limiter, a DC retriever, and a Schmitt trigger. The complete circuit for the NE564 is shown in Figure 1.

Limiter

The input functions to produce a near constant amplitude output that serves as the input for the phase comparator. Eliminating amplitude variations in the FM input signal improves the AM rejection of the PLL. Additional features of the NE564's limiter are that it is capable of accepting TTL signals, operates at high frequencies up to 50MHz, and remains functional with variable supply voltages between 5 and 12V.*

Signal limiting is accomplished in the NE564 with a differential amplifier whose output is clipped by diodes D_1 and D_2 (see Figure 2). Schottky diodes are used because their limiting occurs between 0.3 to 0.4V instead of the 0.6 to 0.7V for regular IC diodes. This lower limiting level is helpful in biasing, especially for 5V operation. When limiting, the DC voltage across R_2 R_3 remains at the Schottky diode voltage. Good high frequency performance for Q_2 and Q_3 is achieved with current levels in the low mA range. Current-source biasing is established via the current mirror of D_5 and Q_4 (see Figure 1).

Base biasing for Q_3 is of concern because of the nature of the input signal which can be either a TTL digital signal of 0 to 5V amplitude or a low-level, AC coupled analog signal. Compatibility for either type is achieved by modifying the limiter of Figure 2 with the addition of the vertical Schottky PNP transistors Q_1 and Q_5 as shown in Figure 3. The input signal voltage appears as a collector-base voltage for Q_1, which presents no problems for either high TTL level inputs or low-level analog inputs. Q_5 is in turn diode-based by D_3 and D_4 (see Figure 1) which places the base voltages of Q_1 and Q_5 at approximately 1.0V. This same biasing network establishes a 1.3V bias at the base of Q_{13} for biasing the phase comparator section. A differential output signal from the input limiter is applied to one input of the phase comparator (Q_9 through Q_{12}) after buffering the level shifting through the Q_7 - Q_8 emitter-followers.

*Note: When operating above $5V_{DC}$, a limiting resistor must be used from V_{CC} to Pin 10 of the NE564.

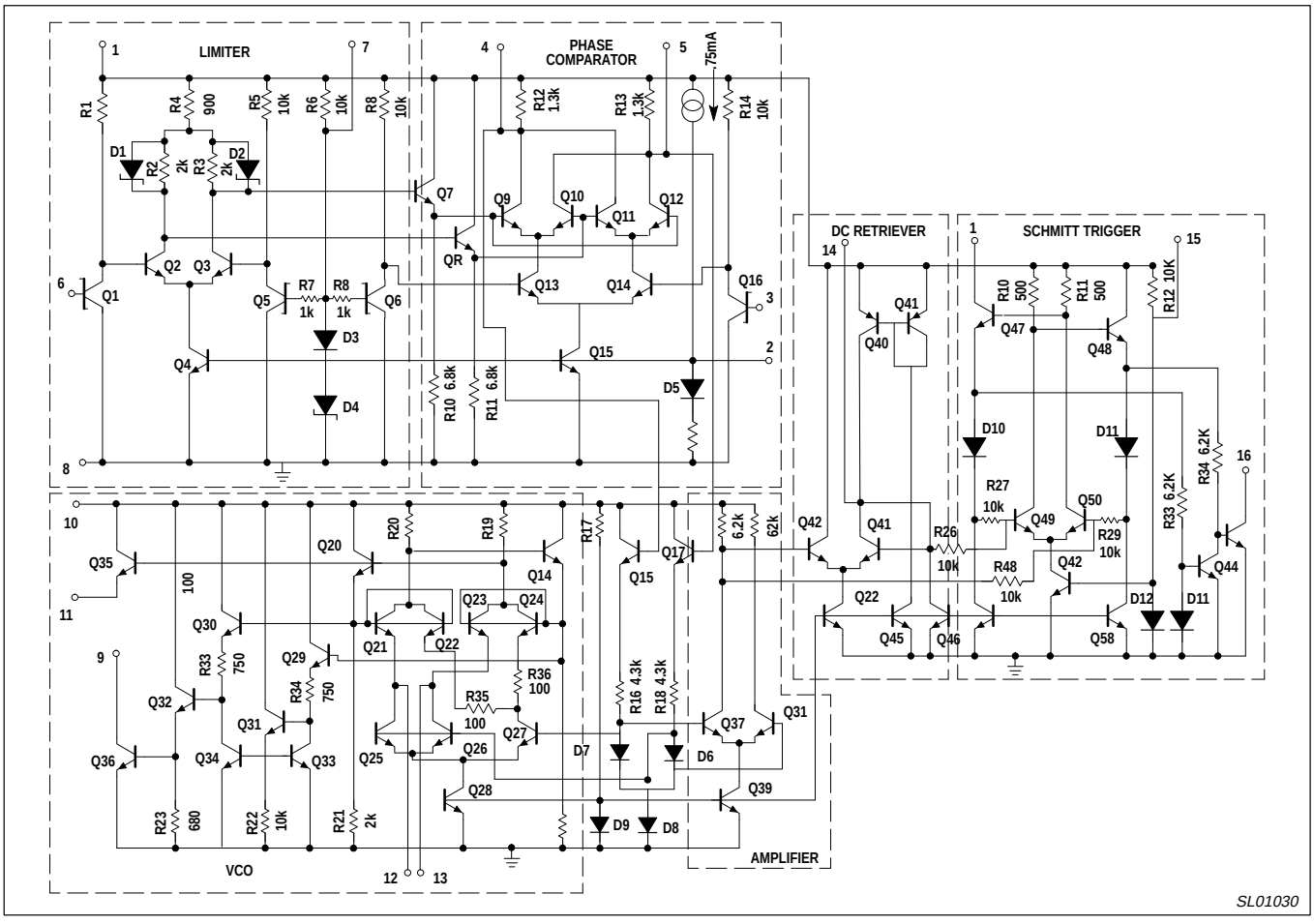


Figure 1. Schematic Diagram of NE564

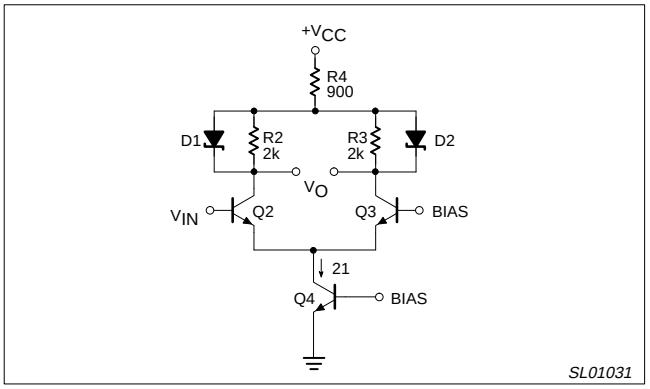


Figure 2. Basic Limiter Stage

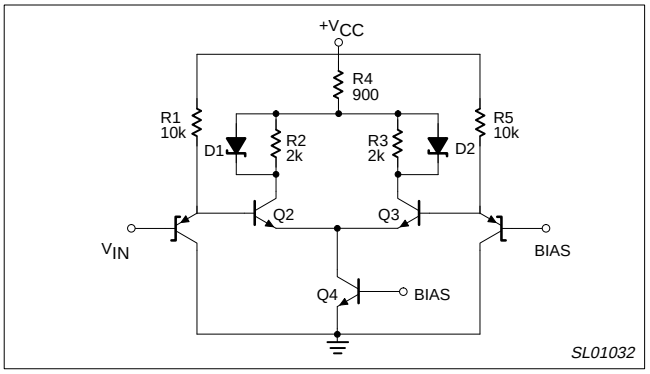


Figure 3. Limiter Stage with Input Buffering

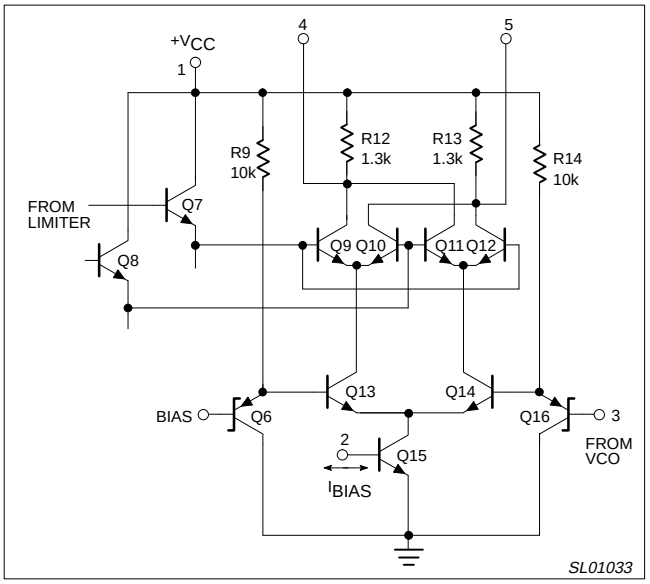


Figure 4. Phase Comparator Section

Phase Comparator

The phase comparator section of the NE564 is shown in Figure 4. It is basically the conventional, double-balanced mixer commonly used in PLL circuits, with a few exceptions. The transconductance, g_M, for the Q_{13} - Q_{14} differential amplifier is directly proportional to the mirror current in Q_{15}. Thus, by externally sinking or sourcing current at Pin 2, g_M can be changed to alter the phase comparator's conversion gain, K_d. The nominal current injected into this node by the internal current source is 0.75mA for 5V operation. If the current is externally removed by gating, the phase comparator can be disabled and the VCO will operate at its free-running frequency.

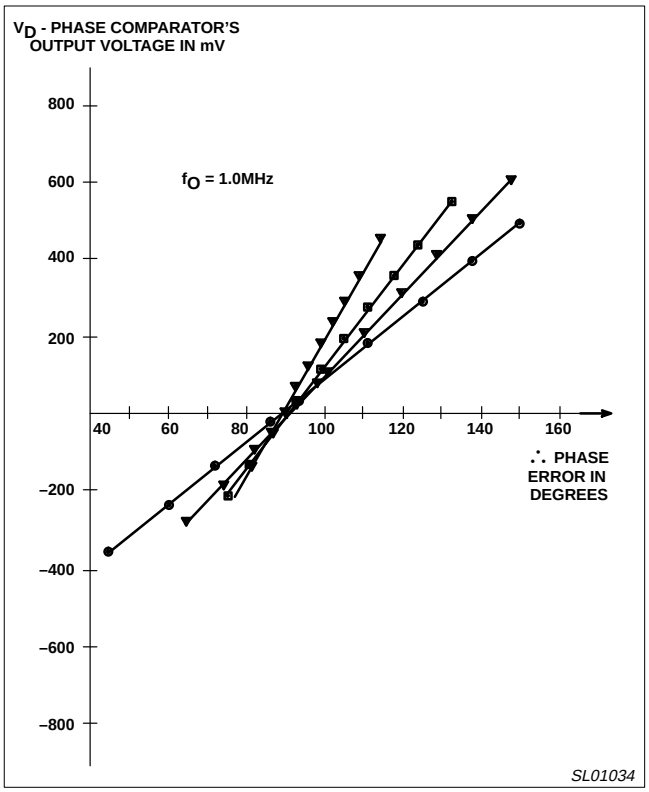


Figure 5. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

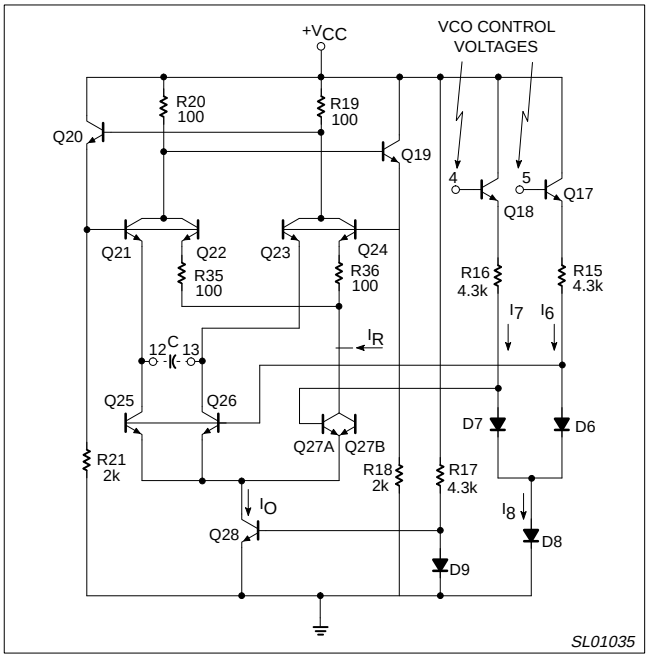


Figure 6. VCO Section of NE564

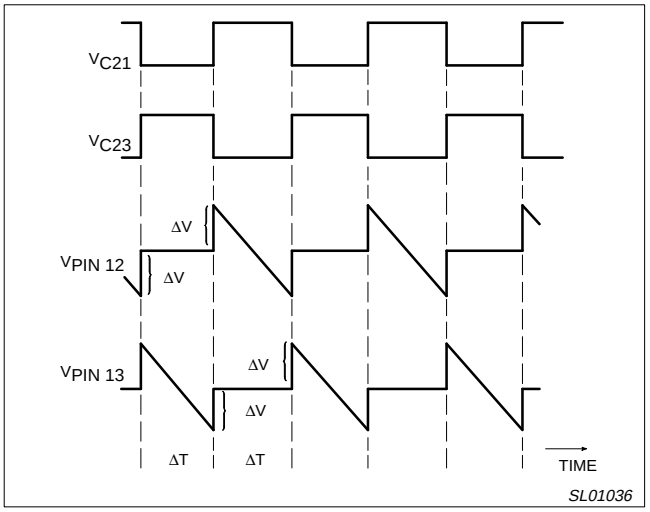


Figure 7. VCO Waveshapes

The variation of K_d with bias current at Pin 2 is shown in the experimental results of Figure 5. Note that the inherent 90o phase error in the loop produces an approximate zero-phase comparator output voltage. For any particular bias current, the slope of the line is the K_d conversion gain for the phase comparator. Numerically the data of Figure 5 can be expressed as:

$$K_d \cong 0.66 \left(\frac{\text{volts}}{\text{rad}}\right)$$

$$+ 9.2 \times 10^{-4} \left(\frac{\text{volts}}{\text{rad} \times \mu\text{A}}\right) \times I_{BIAS}\ (\mu\text{A}) \qquad (1)$$

Equation 1 is valid for bias current less than 800μA where saturation occurs within the phase comparator.

The current level established in Q_{15} of Figure 3 determines all other quiescent currents in the phase comparator (Q_9 through Q_{14}). Currents through R_{12} and R_{13} set the common-mode output voltage from the phase comparator (Pins 4 and 5). Since this common-mode voltage is applied to the VCO to establish its quiescent currents, the VCO conversion gain (K_O) also depends upon the bias current at Pin 2.

VCO

The VCO is of the basic emitter-coupled astable type with several modifications included to achieve the high frequency, TTL compatible operation while maintaining low frequency drift with temperature changes. The basic oscillator in Figure 6 consists of Q_{19}, Q_{20}, Q_{21} and Q_{23} with current sinks of Q_{25} and Q_{26}. The master current sink of Q_{28} keeps the total current constant by altering the ratio of currents in Q_{25} - Q_{26} and the dummy current sink of Q_{27}.

The input drive voltage for the VCO is made up of common-mode and difference-mode components from the phase comparator. After buffering the level shifting through Q_{17} - Q_{18} and R_{15} - R_{16}, the VCO control voltage is applied differentially to the base of Q_{27} and to the common bases of Q_{25} and Q_{26}.

The VCO control voltages from the phase comparator are the Pin 4 and Pin 5 voltages or

$$V_4 = V_{C9} = V_{B18} = V_{CM} + 1/2V_{DM} \qquad (2)$$

$$V_5 = V_{C12} = V_{B17} = V_{CM} + 1/2V_{DM} \qquad (3)$$

where V_{CM} and V_{DM} are the respective common-mode and difference-mode voltages.

Emitter-followers Q_{17} and Q_{18} convert these control voltages into control currents through D_6 and D_7 of the form

$$I_6 = \left(\frac{1}{R_{15}}\right) \left[V_{CM} - 1/2V_{DM} - 3\ V_{BE}\right] \qquad (4)$$

$$I_7 = \left(\frac{1}{R_{16}}\right) \left[V_{CM} - 1/2V_{DM} - 3\ V_{BE}\right] \qquad (5)$$

These individual currents are summed in D_8 and become with R_{15} = R_{16} = R.

$$I_8 = I = I_6 + I_7 = 2/R\ (V_{CM} - 3\ V_{BE}) \qquad (6)$$

Writing I_6 and I_7 as functions of the total I current gives

$$I_6 = \left(\frac{1}{2}\right)\left(1 - \frac{V_{DM}}{RI}\right) \qquad (7)$$

$$I_7 = \left(\frac{1}{2}\right)\left(1 + \frac{V_{DM}}{RI}\right) \qquad (8)$$

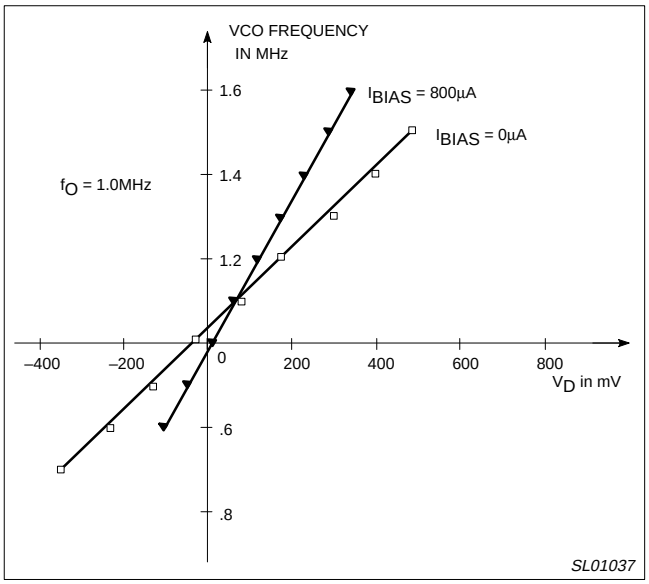


Figure 8. VCO Output as a Function of Input Voltage and Bias Current

Now consider variations in I_6 and I_7 while I remains constant

$$I_6 = (1 - x)\ I = \left(\frac{1}{2}\right)\left(1 - \frac{V_{DM}}{RI}\right) \qquad (9)$$

$$I_6 = x\ I = \left(\frac{1}{2}\right)\left(1 + \frac{V_{DM}}{RI}\right) \qquad (10)$$

where $0 \leq x \leq 1$. Thus x is defined to be

$$x = \left(\frac{1}{2}\right)\left(1 + \frac{V_{DM}}{RI}\right) \qquad (11)$$

Currents I_6 and I_7 establish proportional currents in Q_{25}, Q_{26} and Q_{27} in a manner similar to the analysis above since the current in Q_{28} is a constant, or

$$I_O = I_{C28} = I_{E25} + I_{E26} + {}_{E27A} + {}_{E27B}$$

It can be shown that the D_7 - D_8 diode pair will cause identical differential currents to be reflected in both the Q_{25} - Q_{26} and the Q_{27A} - Q_{27B} differential amplifier pairs. Consequently, the constant-current of I_O, jointly shared by the differential amplifier pairs, will divide in each pair with the same x factor imbalance as in Equation 11.

$$I_{E25} + I_{E26} = xI_O \quad (12)$$

$$I_{E25} = I_{E26} = \left(\frac{x}{2}\right) I_O \quad (13)$$

$$I_{E27A} + I_{E27B} = (1\text{-}x)\, I_O \quad (14)$$

$$I_{E27A} = I_{E27B} = \left(\frac{1-x}{2}\right) I_O \quad (15)$$

Now consider placing a capacitor between the collectors of Q_{25} and Q_{26} (Pins 12 and 13). Oscillation will occur with the capacitor alternately being charged by Q_{21} and Q_{23} and constantly discharged by Q_{25} and Q26. When the Q_{21} and Q_{22} pair conducts, Q_{23} and Q_{24} will be off, causing a negative ramp voltage to appear at Pin 13 and a constant voltage at Pin 12 as shown in Figure 7. During the next half-cycle, the transistor roles and voltages are reversed. Capacitor discharge is via Q_{25} and Q_{26}, which act as constant-current sinks with current amplitudes as in Equation 13.

During each half-cycle, the capacitor voltage changes linearity by $2\Delta V$ volts in ΔT seconds, where

$$\Delta V = 2R_{20}\, I_O \left(\frac{x}{2} + \frac{1 - x}{2}\right) = R_{20}\, I_O \quad (16)$$

and

$$\Delta T = \frac{C2\Delta V}{I_{E25}} \quad (17)$$

Combining these two equations with Equation 13 gives a half period of

$$\Delta T = \frac{4C\, R_{20}}{x} \quad (18)$$

Utilizing Equation 11 with the ΔT expression gives the desired VCO frequency expression of

$$f_O = f_O' \left(\frac{1}{R_{16}}\right) \left[\frac{V_{DM}}{2(V_{CM} - 3\, V_{BE})}\right] \quad (19)$$

where f_O' is the VCO's free-running frequency given by

$$f_O' = \frac{1}{22\, R_{20}\, C} \quad (20)$$

Equation 19 shows that the oscillator frequency is a linear function of the differential voltage from the phase

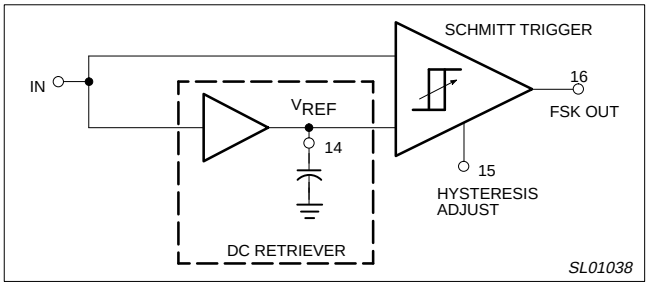


Figure 9. Post Detection Processor for FSK

comparator. Resistors R_{35} and R_{36} function to insure that an initial current imbalance exists between the Q_{25} - Q_{26} transistor pair and the dummy Q_{27}. This imbalance insures that the oscillator is self-starting when power is first applied to the circuit.

The VCO conversion gain is determined as

$$K_O = \frac{\partial f_O}{\partial V_{DM}} = \frac{f_O'}{RI} \text{ Hz/V} \quad (21)$$

which is valid as long as the transistor's V_{BE} changes are small with respect to the common-mode voltage. both f_O and K_O are inversely proportional to R, which has a strong positive temperature coefficient. An internal current I_R having an equal and opposite negative temperature coefficient is inserted into the VCO as shown in Figure 6.

Experimental determination of K_O can be found from the data of Figure 8 where K_O is the slope of either line. Numerically these results are for $I_{BIAS} = 0$.

$$K_O = 0.95 \frac{\text{MHz}}{\text{V}} = 5.9 \times 10^6 \frac{\text{rad}}{\text{volt/sec}} \quad (22)$$

and for $I_{BIAS} = 800\mu A$

$$K_O = 1.7 \frac{\text{MHz}}{\text{V}} = 10.45 \times 10^6 \frac{\text{rad}}{\text{volt/sec}} \quad (23)$$

It must be noted that the specific values obtained for K_O in the manner above are valid only for the 1.0MHz free-running frequency where the data was taken. However, good estimates for K_O at other free-running frequencies can be obtained by linearly scaling K_O to the desired f_O'. Thus, it is sometimes convenient to define a normalized K_O as

$$K_{O(norm)} = \frac{K_O}{f_O'} = 5.9 \frac{\text{rad}}{\text{V}} \ (I_{BIAS} = 0)$$
$$= 10.45 \frac{\text{rad}}{\text{V}} \ (I_{BIAS} = 800\mu A) \quad (24)$$

The K_O estimate for any bias then can be obtained by multiplying the normalized conversion gain by the desired free-running frequency, or

$$K_O \text{ (any } f_O') = K_{O(norm)}\, f_O' \quad (25)$$

The additional VCO circuitry of Q_{29} through Q_{36} functions to produce the TTL and ECL compatible outputs at Pins 9 and 11.

Amplifier

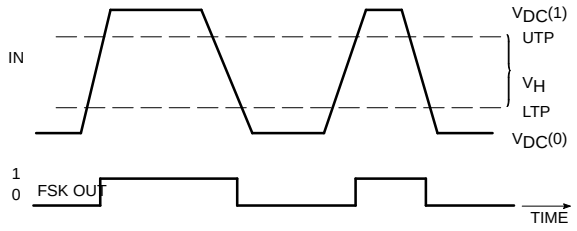
The difference-mode voltage from the phase comparator is extracted and amplified by the amplifier in Figure 1. The single-ended output from this amplifier serves as input signals for both the Schmitt Trigger and a second differential amplifier. Low-pass filtering with a large capacitance at Pin 14 produces a stable DC reference level as the second input to the Schmitt Trigger. When the PLL is locked, the voltage at Pin 14 is directly proportional to the difference between the input frequency and f_O'. thus Pin 14 provides the demodulated output for an FM input signal.

Schmitt Trigger

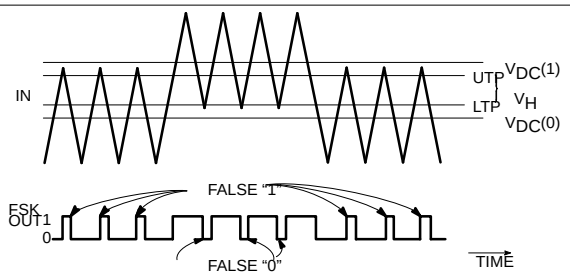
In FSK applications, the Pin 14 voltage will assume two different voltage levels corresponding to the mark and space input frequencies. A voltage comparator could be used to sense and convert these two voltage levels to logic compatible levels. However, at high data rates, V_{DM} will contain a considerable amount of carrier signal which can be removed by extensive filtering. Normally this complex filtering requires quite a few components, most all of which are external to the monolithic PLL. Also, since the control voltage for the comparator depends upon K_O and the deviations of the mark and space frequencies from f_O', the filtering has to be optimized for each different system utilized. However, the necessary DC reference level for the comparator is present in the PLL, but buried in carrier-frequency feedthrough which appears as noise in the system. A Schmitt Trigger with variable hysteresis can be used successfully to decode the FSK data without the need for extensive filtering.

Consider the system shown in Figure 9 where the input signal is the single-ended output derived from the amplifier section of the NE564. The DC retriever functions to establish a DC reference voltage for the Schmitt Trigger. The upper and lower trigger points are adjustable externally around the reference voltage giving the variable hysteresis. For very low data rates, carrier feedthrough will be negligible and the ideal situation depicted in Figure 10 results. Increased data rate produces the carrier feedthrough shown in Figure 10b, where false FSK outputs result because the feedthrough amplitude exceeds the hysteresis voltage. Having the capability to increase the hysteresis, as in Figure 10c, produces the desired FSK output in the presence of carrier feedthrough.

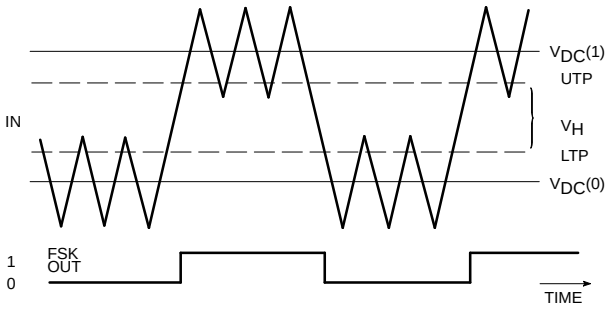
Another important factor to be considered is the temperature drift of the f_O' in the VCO. Small changes in f_O' will change the DC level of the input voltage to the Schmitt trigger. this DC voltage shift would produce errors in the FSK output in narrowband systems where the mark and space deviations in f_{IN} are less than the f_O' change with temperature. However, this effect can be eliminated if the DC or average value of the amplifier signal is retrieved and used as the reference voltage for the Schmitt trigger. In this manner, variations in the f_O' with temperature do not affect the FSK output.



a. Low Data Rates with Negligible Carrier Feedthrough



b. False FSK Outputs Due to Feedthrough and Low Hysteresis



c. Increased Hysteresis Restores Proper FSK Output In the Presence of Feedthrough

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Figure 10. Waveshapes for FSK Decoding in the Post Detection Processor