AN1568
Application Note

Interfacing Between LVDS and ECL

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Introduction

LVDS (Low Voltage Differential Signaling) signals are used to interface between today's CMOS or BiCMOS ASICs supplied with 3.3V. LVDS signals are differential signals with a swing of 250 to 400 mV and a DC offset of 1.2V. External components are required for board to board data transfer or clock distribution.

In advanced systems often only a single supply voltage (3.3V) is available. Low Voltage ECL devices work off this 3.3V supply voltage in the so called LVPECL mode. Input/Output LVPECL levels are related to V_{CC} = 3.3V – a 750 mV output swing with 2V offset. This makes them ideal as peripheral components for ASICs.

LVPECL and LVDS are both differential low voltage signals, but with different swing and different offset. The purpose of this application information is to show the interfacing between these signal levels. In addition it gives interface suggestions to and from 5V supplied PECL devices or negative supplied ECL.

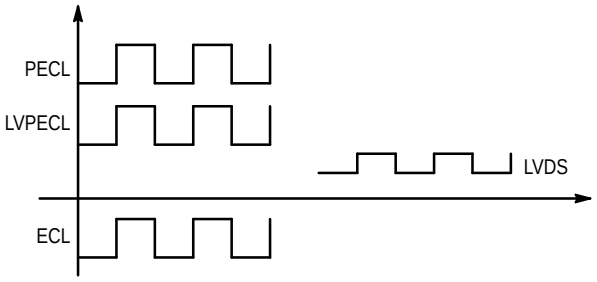

Figure 1. Voltage Levels

LVDS Levels

The LVDS levels have been specified by IEEE (IEEE un–approved Standard P1596.3). There are 2 different specifications, the general purpose specification with 250 to 400 mV swing and the super low power specification with reduced swing (150 ...250mV).

LVDS outputs require a 100Ω load between the differential outputs. This load will in addition terminate the 50Ω controlled impedance lines.

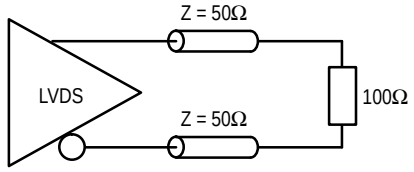

Figure 2. LVDS Output Definition

ECL levels

In ECL circuits all signal levels are related to V_{CC} supply rail. Traditional ECL designs are supplied with negative voltages with V_{CC} = GND.

Today several applications use ECL devices in the PECL mode. PECL – Positive ECL is nothing more than supplying any ECL divide with a positive power supply (+5V).

With the trend to low voltage systems a new generation of ECL circuitry has been developed. The Low Voltage ECL devices (LVECL) work from a 3.3V power supply either as negative supplied or more popular from standard V_{CC} = +3.3V and V_{EE} = GND as LVPECL.

100E(L) type output DC levels for the different supply levels are shown in Table 2 on page 5–3.

Table 1. LVDS Levels

Symbol	Parameter	General Purpose Specification		Super Low Power Specification		Unit	Condition
		Min	Max	Min	Max		
Transmitter							
V_{OH}	Output HIGH Voltage		1474		1374	mV	R_L = 100Ω
V_{OL}	Output LOW Voltage	925		1025		mV	R_L = 100Ω
V_{PP}	Output Differential Voltage	250	400	150	250	mV	R_L = 100Ω
V_{OS}	Output Offset Voltage	1125	1275			mV	
Receiver							
	Input Voltage Range	0	2400	0	2000	mV	V_{gpd} < 950mV
	Differential HIGH Input Threshold		+100		+100	mV	V_{gpd} < 950mV
	Differential LOW Input Threshold	–100		–100		mV	V_{gpd} < 950mV

Table 2. MC100Exxx/MC100ELxx (T_A = 0°–85°C)

Symbol	Parameter	LVPECL[1]	PECL[2]	ECL	Unit
V_{CC}		+3.3	+5.0	GND	V
V_{EE}		GND	GND	–5.2, –4.5 or –3.3	V
V_{OH}	Minimum Output HIGH Level	2.275	3.975	–1.030	V
V_{OH}	Typical Output HIGH Level	2.345	4.045	–0.955	V
V_{OH}	Maximum Output HIGH Level	2.420	4.120	–0.880	V
V_{OL}	Minimum Output LOW Level	1.490	3.190	–1.810	V
V_{OL}	Typical Output LOW Level	1.595	3.295	–1.705	V
V_{OL}	Maximum Output LOW Level	1.680	3.380	–1.620	V

1. V_{CC} assumed 3.3V. All levels vary 1:1 with V_{CC}.
2. V_{CC} assumed 5V. All levels vary 1:1 with V_{CC}.

ECL outputs are open emitter outputs, requiring a DC path to a more negative supply than V_{OL}. This pull down resistor termination can be used to terminate transmission lines application specific.

ECL standard DC input levels are related to V_{CC}. Several devices are available with so called common mode range inputs. These inputs allow to process signals with small swings down to 200 mV, 150 mV or even 50 mV signal levels within an offset range.

Interfacing

Common mode range inputs are capable to process differential signals with 150 to 400 mV swing. The LVDS input processes signals up to 950 mV swing. The DC voltage levels should be within the input voltage range.

To interface between these 2 voltage levels capacitive coupling can be used. Only clock or coded signals should be capacitive coupled.

A capacitive coupling of NRZ signals will cause problems. Then passive or active interfacing is necessary.

Capacitive Coupling LVDS to ECL

Capacitive Coupling LVDS to ECL using V_{BB}

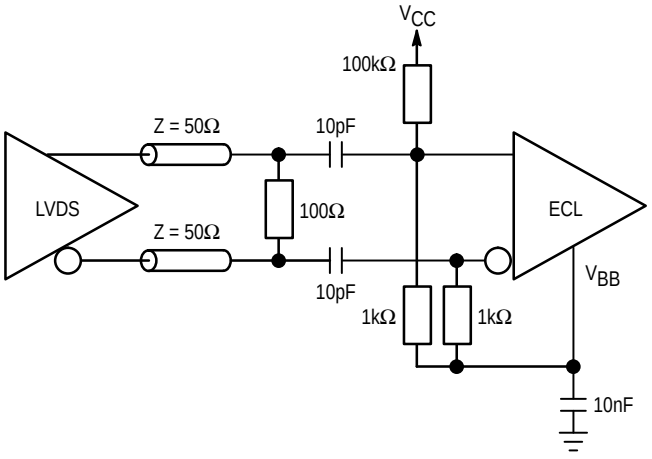

Figure 3. Capacitive Coupling LVDS to ECL Using V_{BB}

Several ECLinPS/ECLinPS Lite devices supply a V_{BB} ($V_{BB} \approx V_{CC}$–1.3V) reference voltage. It can been used for differential capacitive coupling. V_{BB} needs to be decoupled to GND via a 10 nF capacitance.

The 100kΩ gives stable known behavior for all signal conditions.

Capacitive Coupling LVDS to ECL with external biasing

If V_{BB} reference voltage is not available a similar DC voltage can be generated with a resistor divider. The resistor values depend on V_{CC}/V_{EE} voltages.

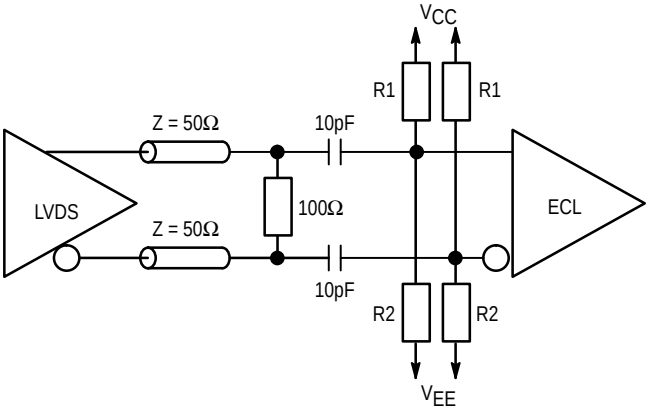

Figure 4. Capacitive Coupling LVDS to ECL with External Biasing

Examples:

V_{CC} = 5V, V_{EE} = GND: R1 = 1.2 kΩ R2 = 3.4 kΩ

V_{CC} = 3.3V, V_{EE} = GND: R1 = 680 Ω R2 = 1 kΩ.

In the layout for both interfaces the resistors and the capacitors should be located as close as possible to the ECL input.

Capacitive Coupling ECL to LVDS

The ECL output requires a DC path. The pulldown resistors are connected to V_{EE}.

The thevenin resistor pair represent the termination of the transmission line Z = R1 || R2 and generates a DC level of 1.2V.

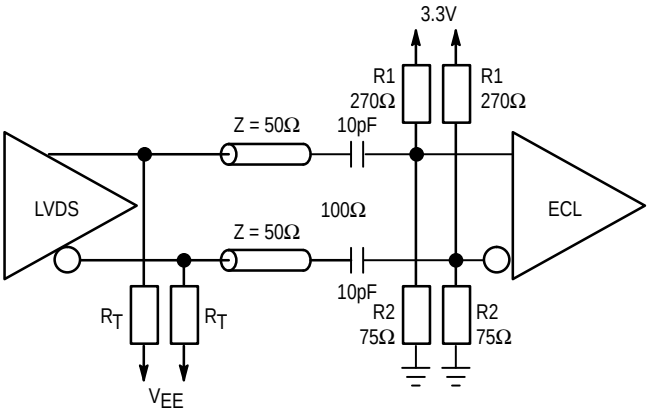

Figure 5. Capacitive Coupling LVDS to ECL

Capacitive Coupling ECL to LVDS using V_{OS} reference voltage

Some devices with LVDS interfaces supply V_{OS} reference voltage. This can be used for capacitive coupling. Beside the transmission line length is very short, a parallel termination should be used and placed as close as possible to the coupling capacitors.

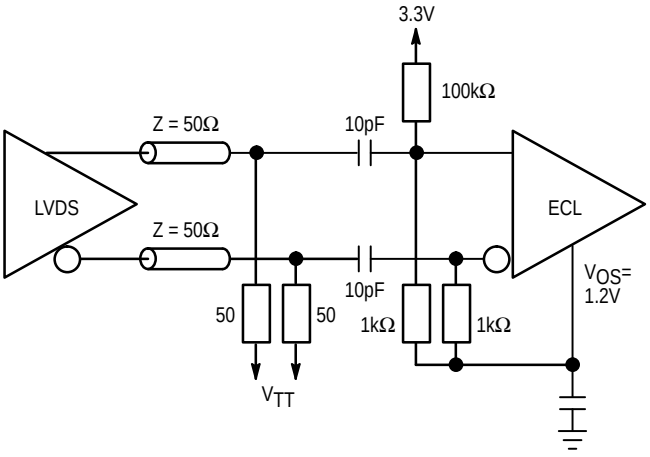

Figure 6. Capacitive Coupling LVDS to ECL Using V_{OS} Reference Voltage

Interfacing from LVPECL to LVDS

The DC output level of LVPECL is more positive than the input range of LVDS. All ECL devices need pulldown resistors. The pulldown resistors in a thevenin equation or pulldown resistors to GND can be split up into a resistor divider to generate LVDS levels.

Dependent on the application one of the following interfaces should be used:

Interfacing LVPECL to LVDS in thevenin equation

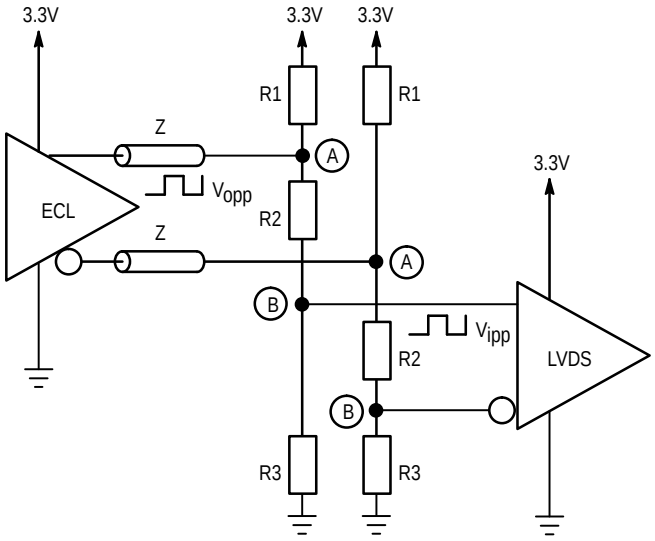

Figure 7. Interfacing LVPECL to LVDS in Thevenin Equation

The thevenin equation resistors terminate the transmission line Z near the receiver (parallel termination). Instead of a resistor to V_{EE}, a resistive path to V_{CC} and to V_{EE} (GND) build the termination of the transmission line. In transmission line theory these resistors are in parallel for high frequency signals. They match the line characteristic impedance.

$$R1 \parallel (R2 + R3) = Z \qquad \text{Equation 1}$$

The DC condition for point A is V_{CC} – 2V. The DC levels at the LVDS input (B) are located within the LVDS input common mode range.

$$\text{A:} \quad R1/(R1 + R2 + R3) = 2\ V/V_{CC} \qquad \text{Equation 2}$$

$$\text{B:} \quad R3/(R1 + R2 + R3) = V_{IL}/V_{CC} \qquad \text{Equation 3}$$

The swing at the LVDS input is decreased dependent on R2 and R3

$$V_{ipp} = R3/(R2 + R3) * V_{opp}$$

$$V_{IH} < 2.0\ V\ (2.4\ V)$$

$$V_{IL} > 0\ V$$

Calculations give non–standard resistor values. When choosing resistors off the shelf it should be considered to avoid a cutoff condition also under worst case supply voltage.

Example:

For 50Ω controlled impedance lines R1 = 120Ω, R2 =33Ω and R3=51Ω.

For any other controlled impedance line the calculation of the resistive divider is done according to Equation 1, Equation 2 and Equation 3.

Interfacing LVPECL to LVDS with unterminated transmission line

Unterminated lines can be used for very short interconnects. For details about recommended maximum unterminated line length, see Motorola's *High Performance ECL Data Book* (DL140/D), chapter 4 "System Interconnects".

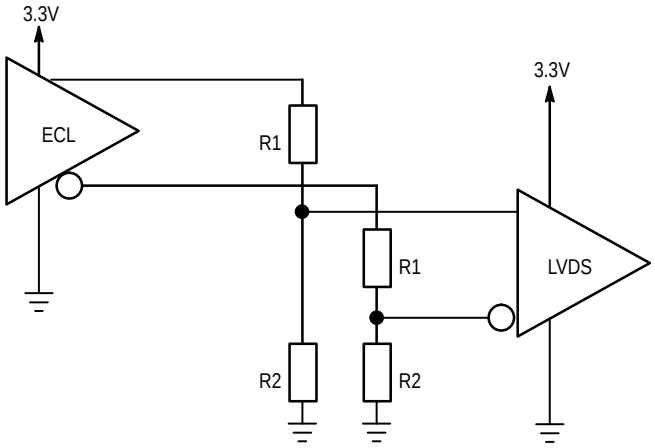

Figure 8. Interfacing LVPECL to LVDS with Unterminated Transmission Lines

The resistive divider reduces the offset of the signal to be processed by LVDS.

For example the following resistor values can be used:

R1 = 56Ω

R2 = 82Ω

Parallel termination to GND is possible with a impedance matching resistor pair (R1 + R2 = Z) using the Figure 8. Unfortunately this low impedance path causes a high output current. This will increase the device's power consumption. The increased die temperature has a negative impact on the statistic life time of the device.

Please Note: The maximum ratings of the output current may not be violated.

Interfacing from LVDS to LVPECL

The common mode range inputs of the low voltage ECL line receivers are defined wide enough to process LVDS signals.

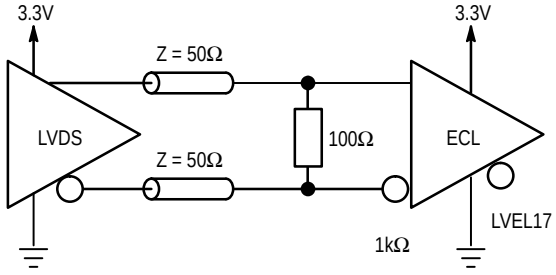

Figure 9. Interfacing LVDS to LVPECL

This direct interface is possible for all LVELxx devices with differential common mode range inputs, e.g. MC100LVEL17, MC100LVEL13, MC100LVEL14, MC100LVEL29, MC100LVEL39.

Interfacing from PECL to LVDS

Interfacing from PECL to LVDS using thevenin parallel termination

As described for LVPECL to interface from PECL to LVDS a thevenin equation termination is used.

Near the receiver a +5V power supply connection is required.

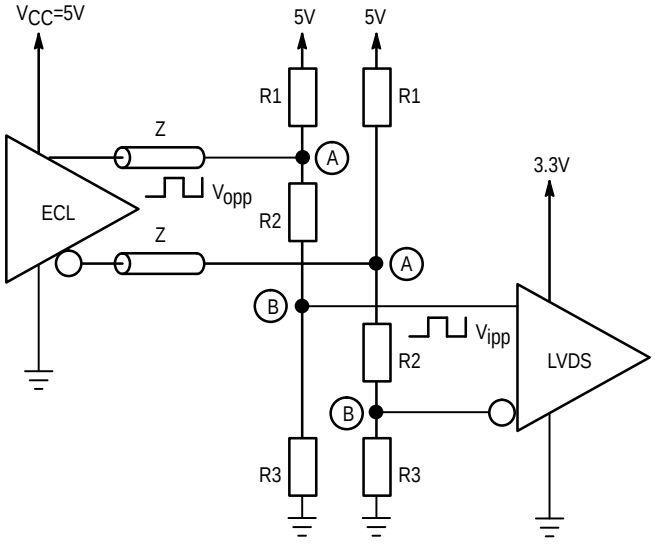

Figure 10. Interfacing from PECL to LVDS Using Thevenin Equivalent Parallel Termination

$$R1 \parallel (R2 + R3) = Z \qquad \text{Equation 4}$$

The DC termination level at A is V_{CC} – 2V. The DC level of B should be within the LVDS input common mode range.

$$R1/(R1 + R2 + R3) = 2\ V/V_{CC} \qquad \text{Equation 5}$$

$$R3/(R1 + R2 + R3) = V_{IL}/V_{CC} \qquad \text{Equation 6}$$

The swing at the LVDS input is decreased dependent on R2 and R3

$V_{ipp} = R3/(R2 + R3) * V_{opp}$

$V_{IH} < 2.0\ V\ (2.4\ V)$

$V_{IL} > 0\ V$

Calculations give non standard resistor values. When choosing resistors off the shelf it should be considered to avoid a cutoff condition also under worst case condition.

If a 50Ω controlled impedance line is used the following resistor values are useful:

Examples:

Z= 50Ω	R1 = 82Ω	R2 = 100Ω	R3 = 33Ω
or			
Z= 50Ω	R1 = 82Ω	R2 = 82Ω	R3 = 47Ω

For any other controlled impedance line the calculation of the resistive divider is done according to Equation 4, Equation 5 and Equation 6.

Interfacing from PECL to LVDS with unterminated lines

As described in LVPECL interfacing unterminated lines can be used for very short interconnections.

E.g. the resistors can be R1 = 330Ω, R2 = 150Ω.

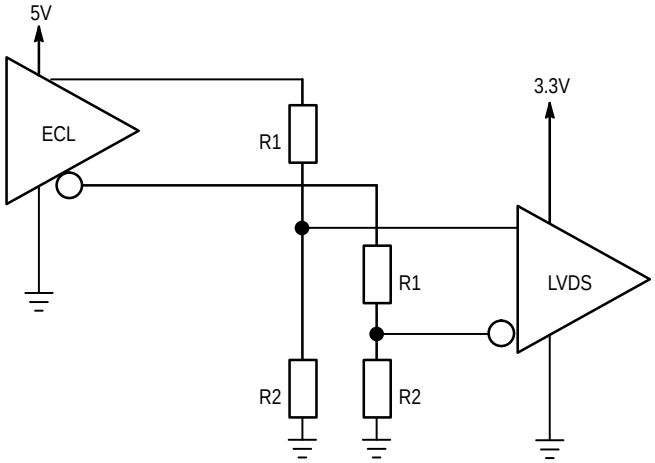

Figure 11. Interfacing from PECL to LVDS with Unterminated Lines

Interfacing from LVDS to PECL

To translate LVDS signals to PECL a differential LVE Lite device with extended common mode range inputs (e.g. MC100EL17) can be used to process and translate LVDS signals when supplied with 5V ± 5% supply voltage.

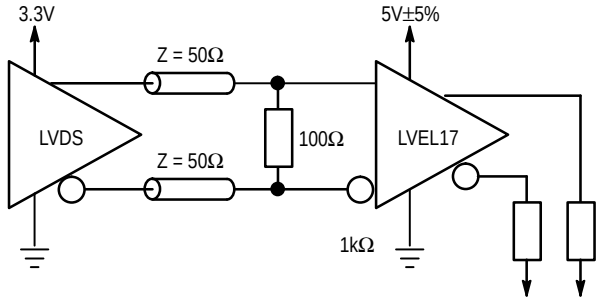

Figure 12. Interfacing from LVDS to PECL

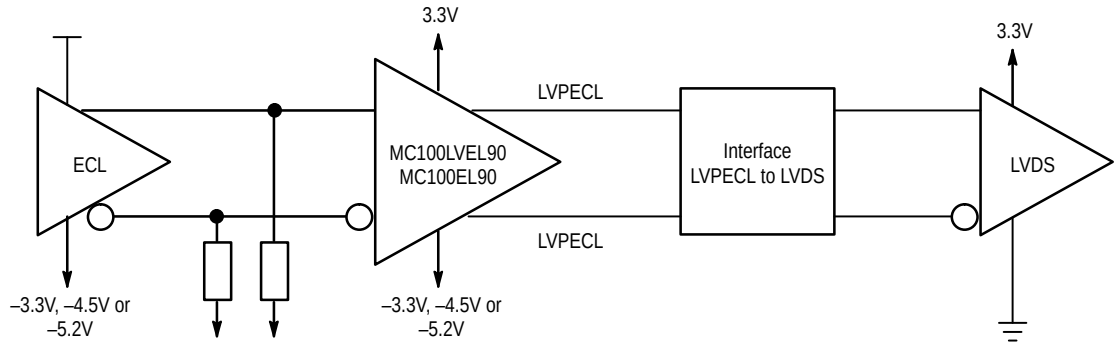

Figure 13. Interfacing from Negative Supplied ECL to LVDS

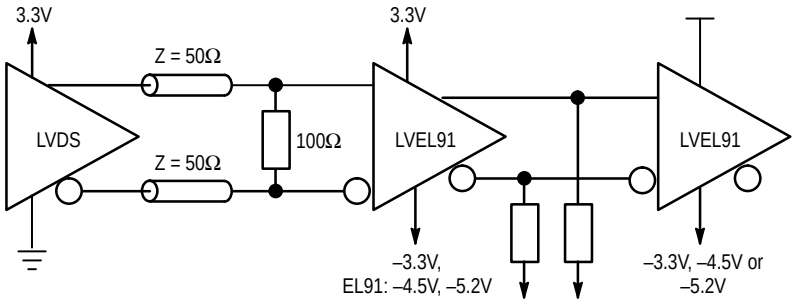

Figure 14. Interfacing from LVDS to Negative Supplied ECL

Interfacing Between Negative Supplied ECL and LVDS

Motorola has developed level translators to interface between the different ECL levels. The MC100LVEL/EL90 translates from negative supplied ECL to LVPECL. The interface from LVPECL to LVDS inputs is done as described above. For –4.5/–5.2V power supplies the MC100EL90 is used, for –3.3V supplies the MC100LVEL90.

To interface from LVDS to negative supplied ECL the common mode range of the MC100LVEL91 for –3.3V supply and the MC100EL91 for –4.5/–5.2V supply is wide enough to process LVDS signals.

If a +5V supply and a V_{EE} = –5.2V ± 5% supply is available the MC10E1651 can be used.

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