AN1560
Application Note

Low Voltage ECLinPS™ SPICE Modeling Kit

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Low Voltage ECLinPS SPICE Modeling Kit

Objective

The Objective of this kit is to extend the information given in the applications note AN1503 for ECLinPS and ECLinPS Lite™ I/O spice modeling kit to the low voltage family of ECLinPS and ECLinPS Lite devices. The kit will provide enough circuit schematic and SPICE parameter information to allow a system level interconnect simulation to be performed using the Low Voltage ECLinPS and ECLinPS Lite device families. The Low Voltage ECLinPS and ECLinPS Lite are the newest additions to Motorola's highest performance ECL/PECL family of products. The families have packaged gate delays of 300 ps and output edge rates as low as 175 ps like the standard ECLinPS and ECLinPS Lite families, only at power supply levels of 3.3V. The addition of these families extends the capabilities of the state–of–the–art in ECL/PECL to low voltage applications with no decrease in AC performance. The kit is not intended to provide information necessary to perform circuit level modeling on individual Low Voltage ECLinPS and ECLinPS Lite devices. If additional information is necessary, contact the factory application engineers.

Schematic Information

The kit contains all the input and output schematics used for the Low Voltage ECLinPS and ECLinPS Lite devices available at the writing of this note. This application note will be modified as new devices are added. If it is not clear a particular device is included, Contact the Motorola Logic Applications group. A worst case model for various package types is included to improve the accuracy of the system model. The package model represents the parasitics as they are measured a sizable distance from an AC ground pin. If typical values are desired, reduce the inductance and capacitance parameters of the package model by 20%. The package models should be placed on all external inputs to a input model, all external outputs for a output model and the V_{CC} line. A model can be used at the V_{EE} pin: but is not necessary since the current in the V_{EE} pin is a constant.

At this time there are 23 schematics for the input structures of the families, representing all the inputs used on the existing devices. Some of the structures are special and are only used for one device. The schematics require the addition of ESD and package models to be accurate; but are otherwise functionally correct. It is unnecessary to include an ESD or Package model for the V_{BB} pins of the models because V_{BB} is intended as an internal node for most applications. If V_{BB} is modeled as an external node it is usually bypassed because it is a constant voltage, and adding ESD and Package parameters provide no additional benefit. A table outlining which input models are used in a particular input is included in this note (See Table 3).

There are two basic output structures and three special output structures for the families. One is a simple standard 50Ω drive ECL output used in the standard ECLinPS device and has about 3.5mA of switch current. The second is the bandwidth enhanced ECLinPS Lite structure used to allow the bandwidth of the devices to be increased. Because the bandwidth of standard ECLinPS devices is limited by their rise and fall times, the limitation can be minimized by simply increasing switch current in the output buffer. The increased current charges and discharges parasitic capacitances rapidly and the current density is set to allow the device to perform at peak Fτ, thus the structure bandwidth is optimized. The enhanced output draws 7.0mA of switch current. The rest of the output buffers are special structures designed to meet a particular device requirement.

The LVE and LVEL families are only offered in a 100K, temperature and voltage compensated format. The output buffer schematics and netlists contain the temperature compensation structure, and only the ESD and package models need to be added. Any input or output that is driving or being driven by an off chip signal should include the ESD and package models. The output buffers show differential inputs and outputs. If it is necessary to simulate a single ended output; the load resistor, package model, ESD structure and output emitter follower, of the unused output, may be eliminated to simplify the system model. If an output is driven directly, instead of with an input cell there are two ways to do so, either differentially or single ended. Table 1 shows the necessary parameters to be met.

Table 1.

Mode	Structure	In	I_{NB}	t_r/t_f (20–80%)	LV_{CC}	LV_{EE}
LVPECL	Differential	+1.1V → +0.7V	+0.7V → +1.1V	180ps	+3.3V	0V
	S.E.	+1.3V → +0.7V	+2.0V	180ps		
LVECL	Differential	–1.2V → –1.6V	–1.6V → –1.2V	180ps	0V	–3.3V
	S.E.	–1.0V → –1.6V	–1.3V	180ps		

SPICE Parameter Information

In addition to the schematics and netlists is a listing of the SPICE parameters for the transistors referenced in the schematics and netlists. These parameters represent a typical device of a given transistor. Varying the typical parameters will affect the DC and AC performance of the structures; but for the type of modeling intended by this note, the actual delay times are not necessary and are not modeled, as a result variation of the device parameters are meaningless. The performance levels are more easily varied by other methods and will be discussed in the next section. The resistors referenced in the schematics are polysilicon and have no parasitic capacitance in the real circuit and none is required in the model. The schematics display the only devices needed in the SPICE netlists.

Modeling Information

The bias drivers for the devices are not included as they are unnecessary for interconnect simulations and their use results in a large increase in model complexity and simulation time. The internal reference voltages (V_{BB}, VCS, Etc.) should be driven with ideal constant voltage sources. Table 2 summarizes the levels required as well as some typical input parameters, and since the LVE/LVEL families are 100K type the levels are the same for all temperatures and power supplies if the power supply is negative. If LVPECL mode is used the levels vary one to one with the power supply; but are constant as a function of temperature.

Table 2.

Parameter	Typical	Worst Case
V_{BB}	V_{CC}–1.295V	V_{CC}–(1.295±50mV)
LVCS	V_{EE}+0.9V	V_{EE}+(0.9V±20mV)
VCS	V_{EE}+1.3V	V_{EE}+(1.3V±50mV)
V_{IH}	V_{CC}–0.89V	V_{CC}–($V_{IHmin,max}$) Data Book
V_{IL}	V_{CC}–1.75V	V_{CC}–($V_{ILmin,max}$) Data Book
t_r/t_f	400ps (20–80%)	Use Data Book Specifications

The schematics and SPICE parameters will provide a typical output waveshape that may not represent the worst case situation. There are simple adjustments that can be made to the system and models to allow output characteristics to simulate conditions at or near the corner of the data book specifications. First the V_{OH} level can be adjusted at a 1:1 rate by moving LV_{CC} the necessary amount of mV's to get the required level. The adjustment will also move the V_{OL} level by the same amount. To adjust the V_{OL} level independently of the V_{OH} level, the collector load resistors can be increased or decreased. Note that the V_{OH} level will also change slightly due to a IbRL drop across the collector load resistor or V_{OL} can be changed by varying the gate current through the current source resistor. The rise and fall times can be adjusted by varying the collector load resistors and adjusting the gate current. To adjust the model to a corner specification the following sequence is recommended:

1) Adjust the gate current to produce the desired output slew rate.

2) Adjust the LV_{CC} for the desired V_{OH} level.

3) Adjust the load resistor for the desired V_{OL}.

Summary

The information included in this kit should provide the customer with adequate information to run a SPICE level system interconnect simulation. The block diagram in Figure 2 illustrates a typical situation which can be modeled using the information in this kit. The schematic information provided in this kit is available in netlist form through EMAIL or on a floppy disk in DOS or Macintosh® format. If the netlist, clarification, or additional information is needed, please contact any Motorola Logic Applications Engineer for assistance.

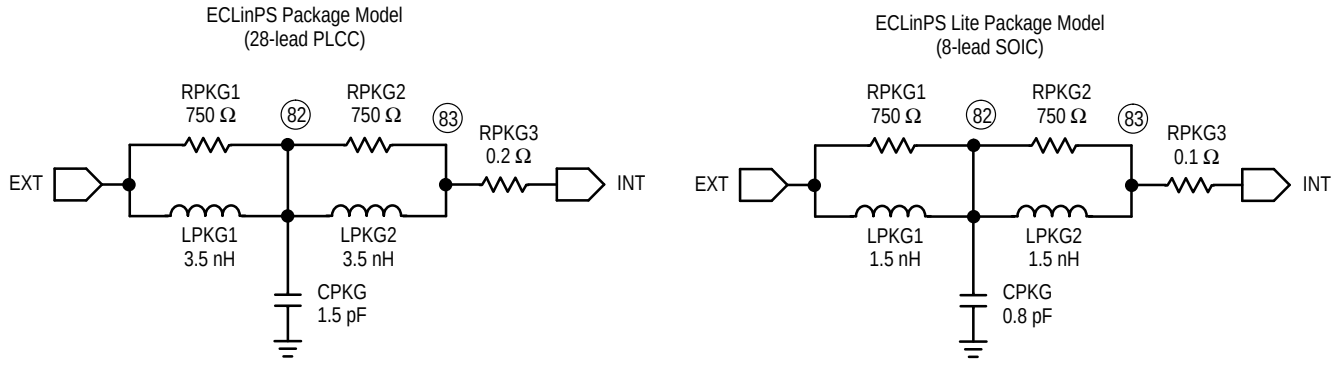


Figure 1a. Package Model Schematics

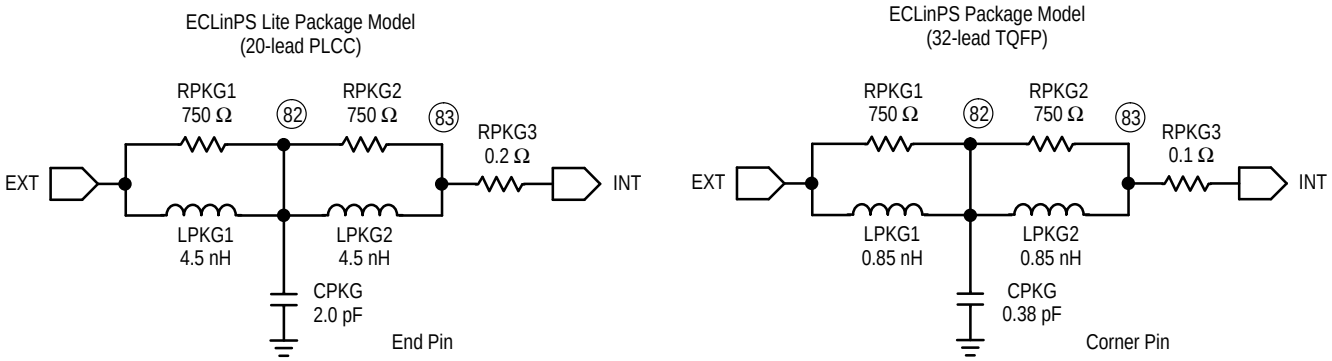


Figure 1b. Package Model Schematics (continued)

Table 3. LVEL/LVE I/O SEL

Device	Function	Input	Clock Input	Data Input	S/R Input	Enable Input	Select Input	Output
LVEL01	4–Input OR/NOR Gate	inBUF01						OBUF7.5
LVEL11	1:2 Clock Buffer		inBUF02					OBUF7.5
LVEL13	Dual 1:3 Clock Buffer		inBUF03					OBUF3.5
LVEL14	1:5 Clock Buffer	inBUF04				inBUF05		OBUF3.5
LVEL16	Differential Line Receiver	inBUF02						OBUF7.5
LVEL17	Quad Diff Line Receiver	inBUF06						OBUF3.5
LVEL29	Dual Diff D Flip–Flop		inBUF07	inBUF06	inBUF08			OBUF3.5
LVEL30	3–Bit D Flip–Flop		inBUF07	inBUF06	inBUF08			OBUF3.5
LVEL32	÷2 Divider		inBUF09		inBUF10			OBUF7.5
LVEL33	÷4 Divider		inBUF09		inBUF10			OBUF7.5
LVEL38	2/4/6 Clock Generator		inBUF11		inBUF13	inBUF12	inBUF06	OBUF3.5
LVEL39	2/4–4/6 Clock Generator		inBUF11		inBUF13	inBUF12	inBUF12	OBUF3.5
LVEL51	Diff D Flip–Flop Single		inBUF09	inBUF14	inBUF10			OBUF7.5
LVEL56	Dual 2:1 Multiplexer			inBUF06			inBUF05	OMUX3.5
LVEL59	3–Bit 2:1 Multiplexer			inBUF06			inBUF05	OMUX3.5
LVEL90	LVECL to LVPECL Trans	inBUF17						OBUF3.5
LVEL91	LVPECL to LVECL Trans	inBUF19						OBUF3.5
LVEL92	PECL to LVPECL Trans	inBUF21						OBUF3.5
LVE111	1:9 Clock Buffer	inBUFxxx						OBUFxxx
LVE164	16:1 Multiplexer			inBUF06			S0=inBUF04 S1:2=inBUF15 S3=inBUF05	OBUF3.5
LVE210	1:4 & 1:5 Clock Buffer	IN4=inBUF16 IN5=inBUF03						OBUF3.5
LVE222	1:15 Clock Buffer		inBUF22		inBUF24		inBUF23	OBUF3.5
LVE310	Diff 2:8 Clock Buffer		inBUF06				inBUF07	OBUF3.5

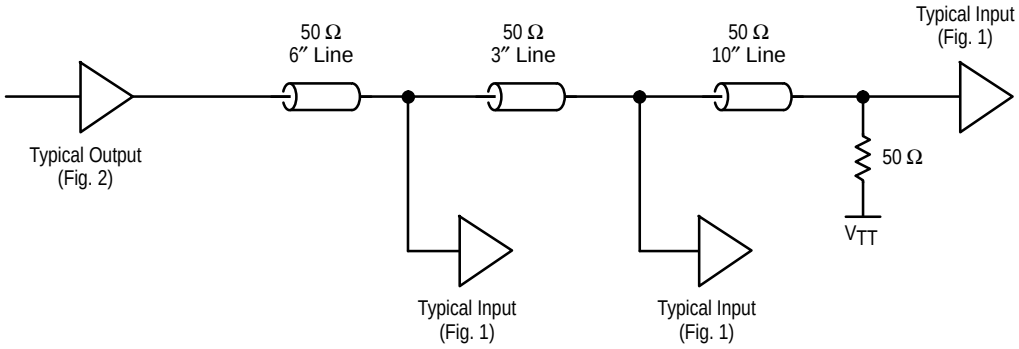


Figure 2. Typical Application for I/O SPICE Modeling Kit

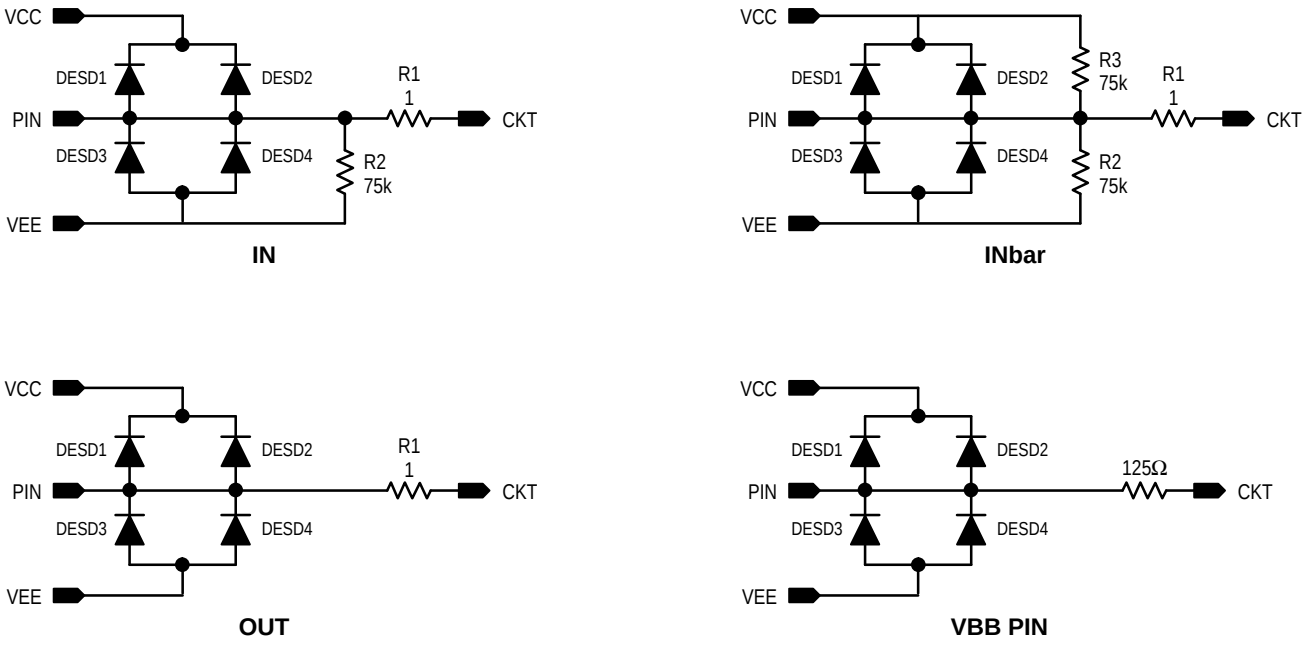


Figure 3. New ESD Structures for EL, LVE and LVEL

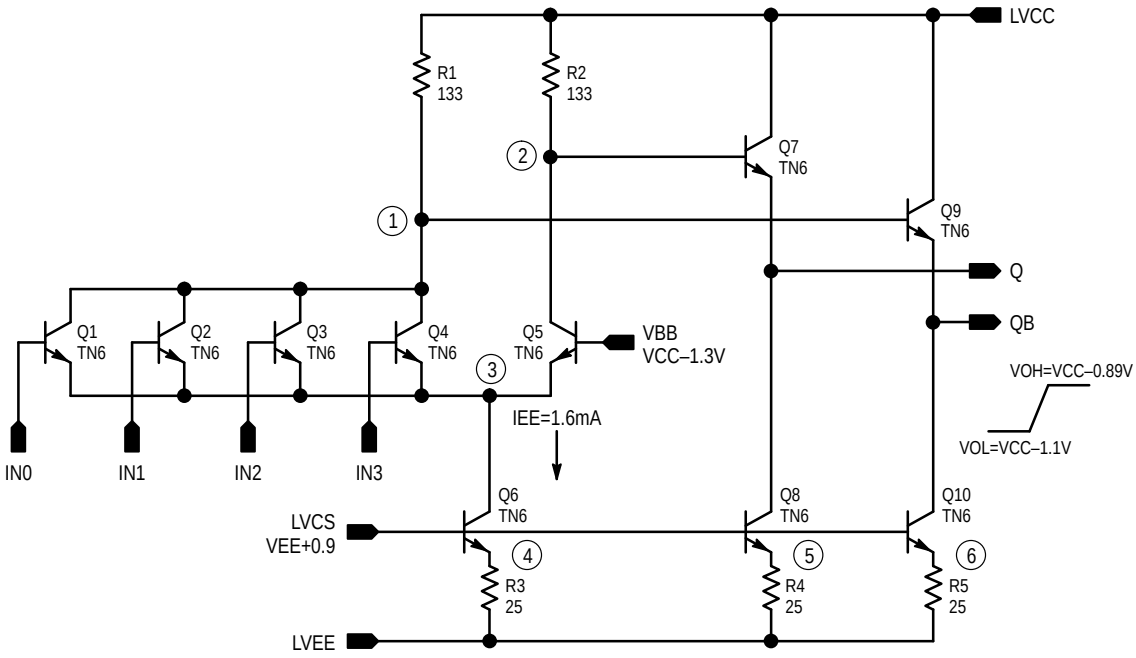


Figure 4. inBUF01 for LVEL

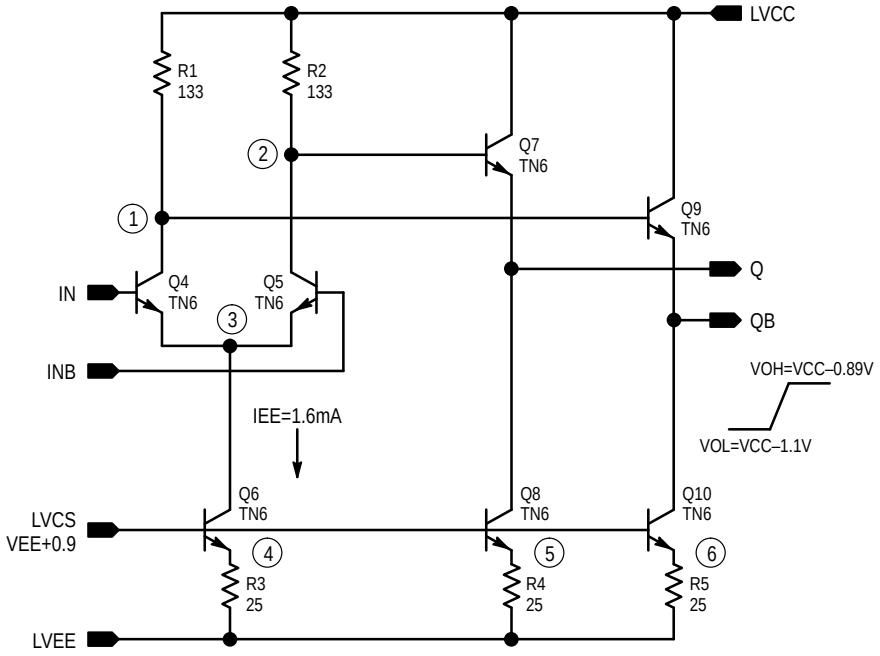


Figure 5. inBUF02 for LVEL

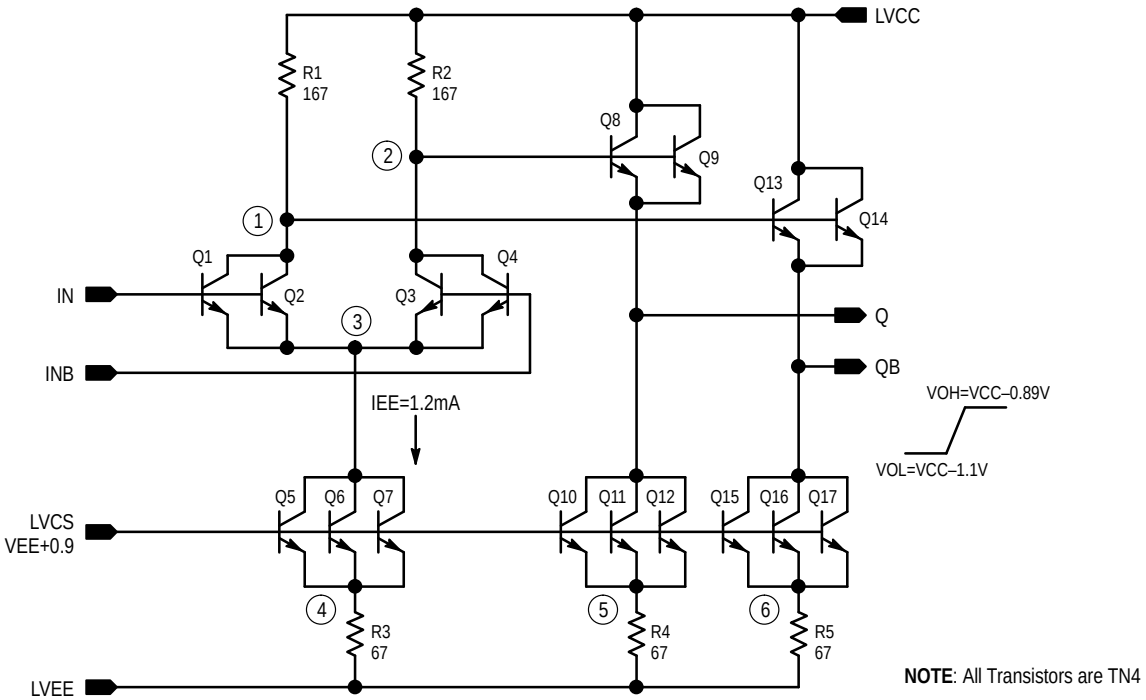


Figure 6. inBUF03 for LVEL

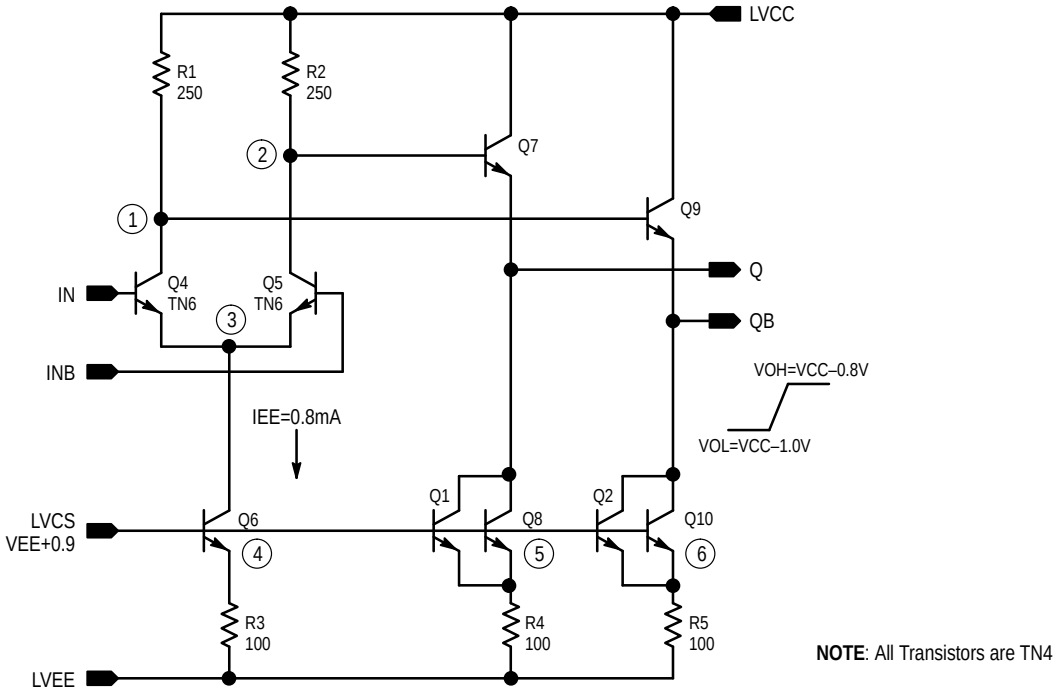


Figure 7. inBUF04 for LVEL

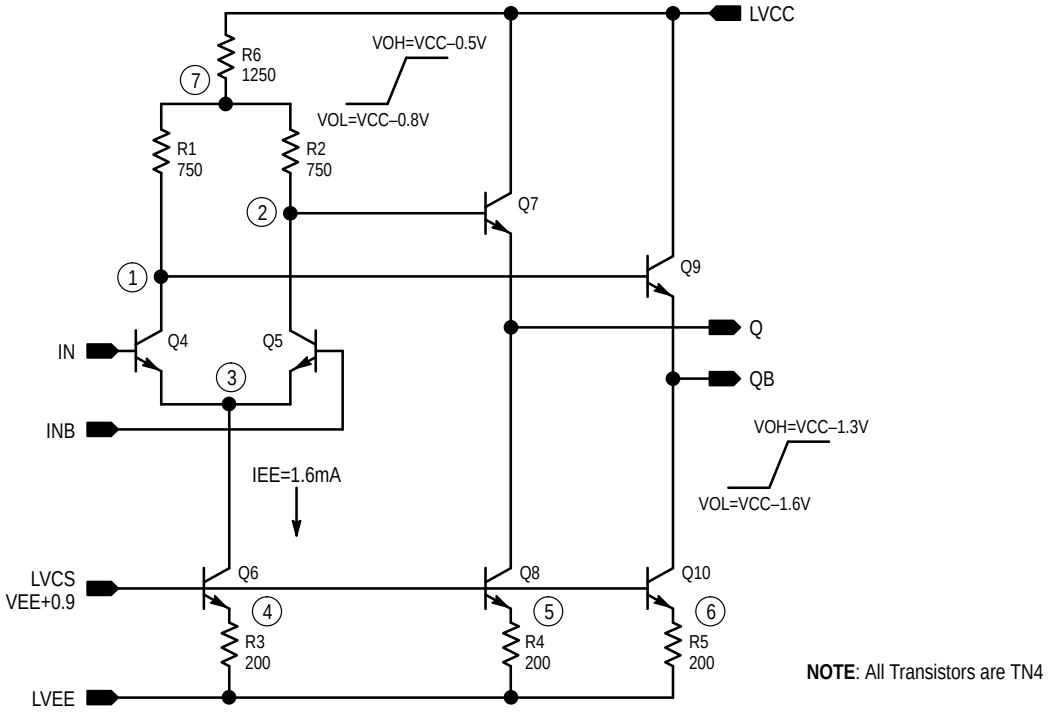


Figure 8. inBUF05 for LVEL

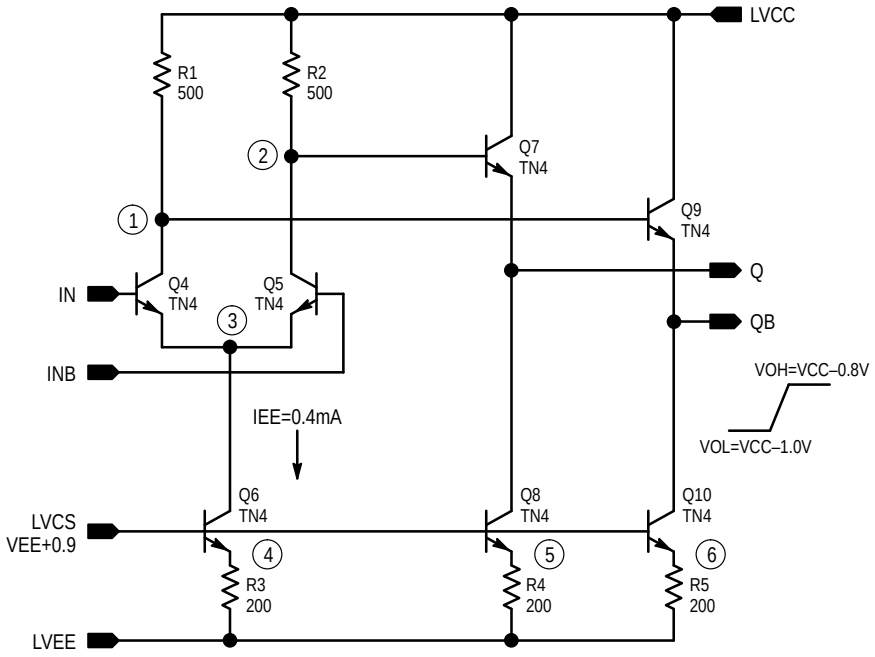


Figure 9. inBUF06 for LVEL

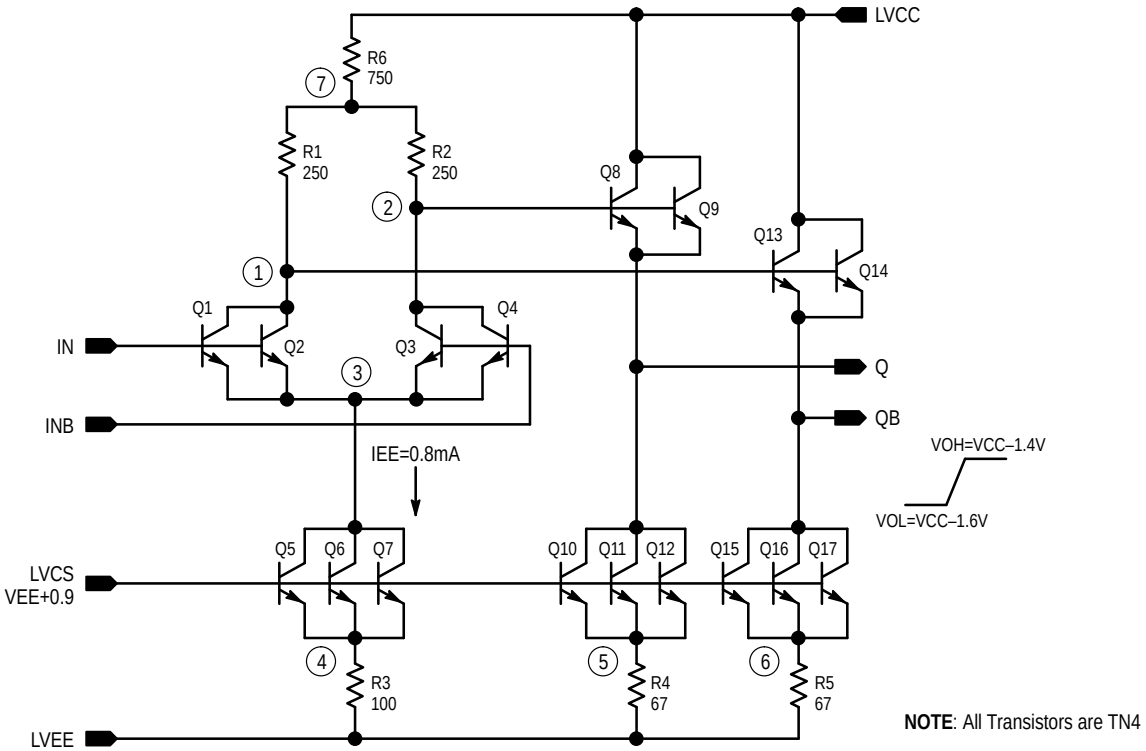


Figure 10. inBUF07 for LVEL

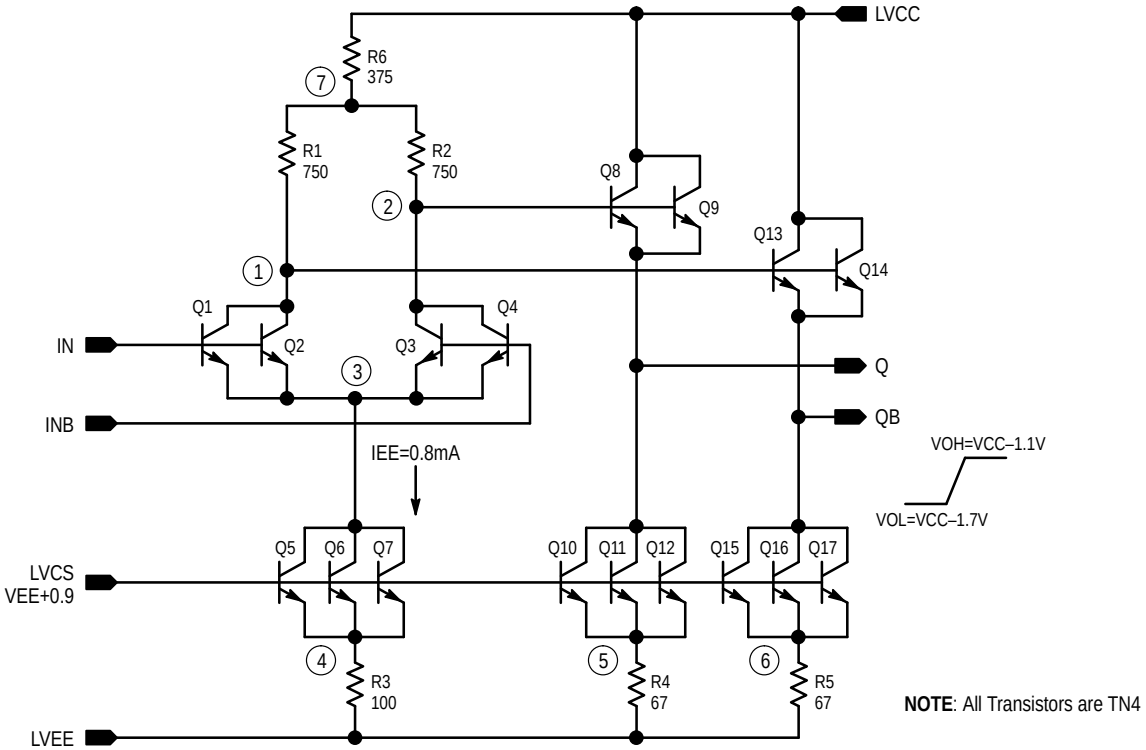


Figure 11. inBUF08 for LVEL

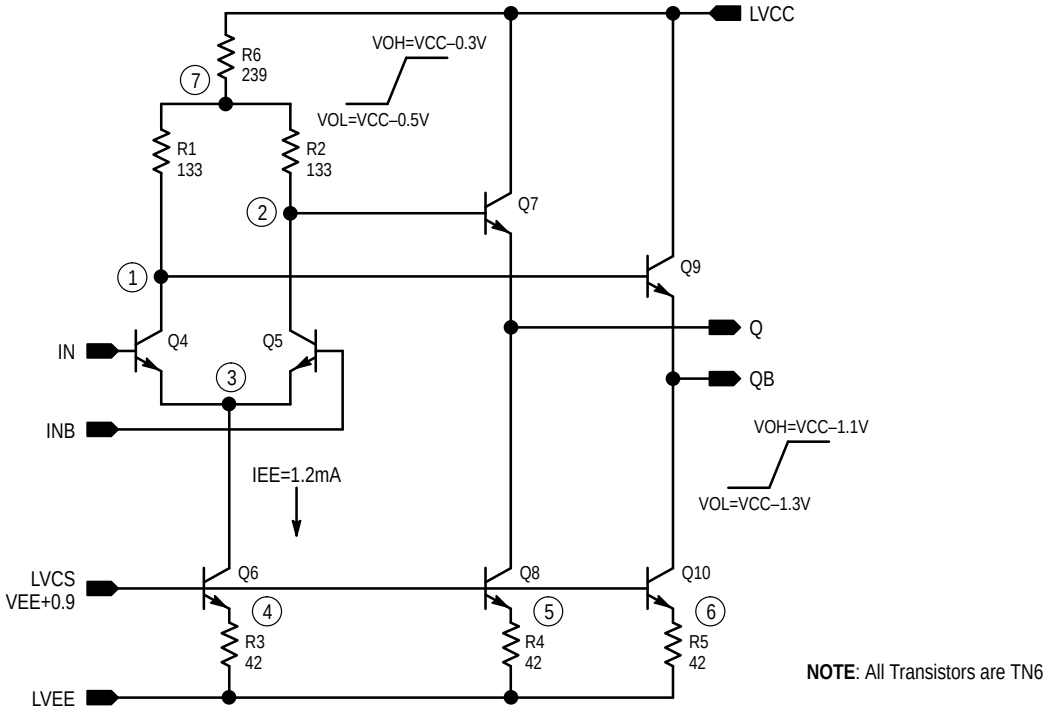


Figure 12. inBUF09 for LVEL

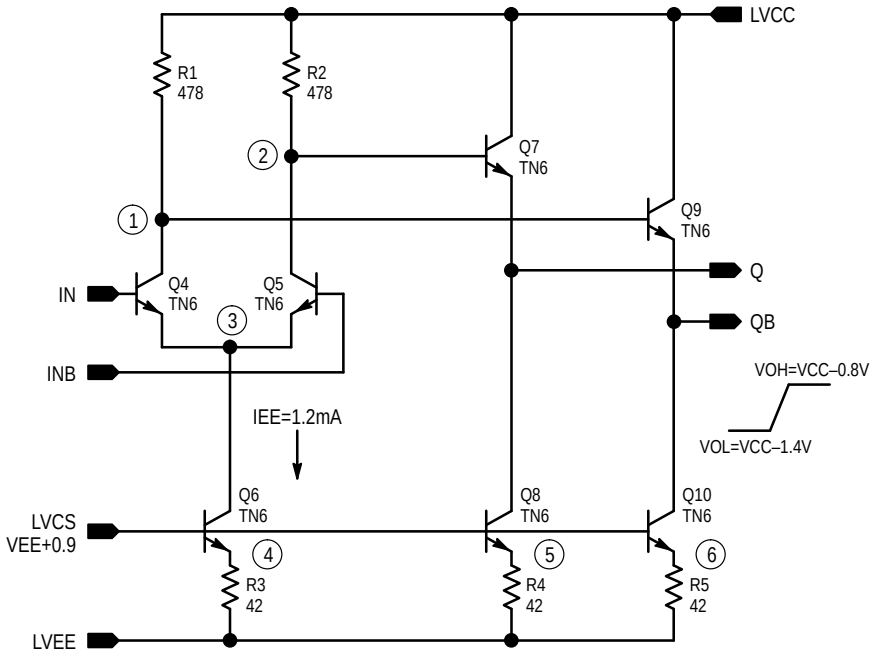


Figure 13. inBUF10 for LVEL

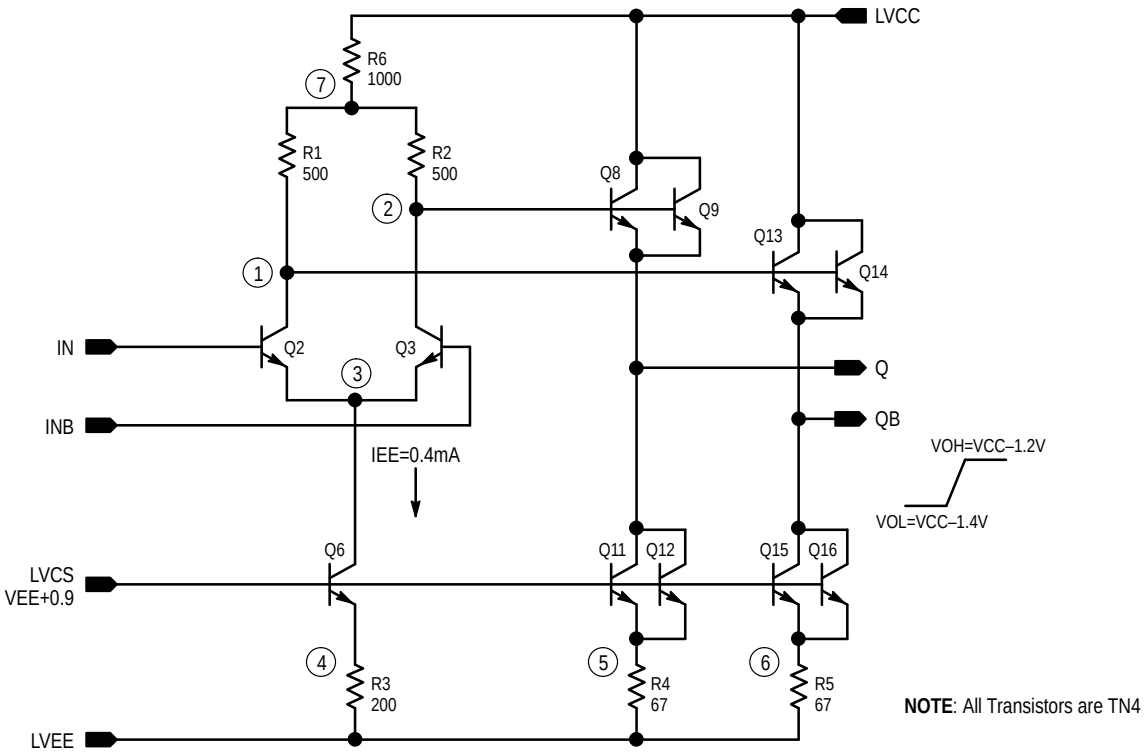


Figure 14. inBUF11 for LVEL

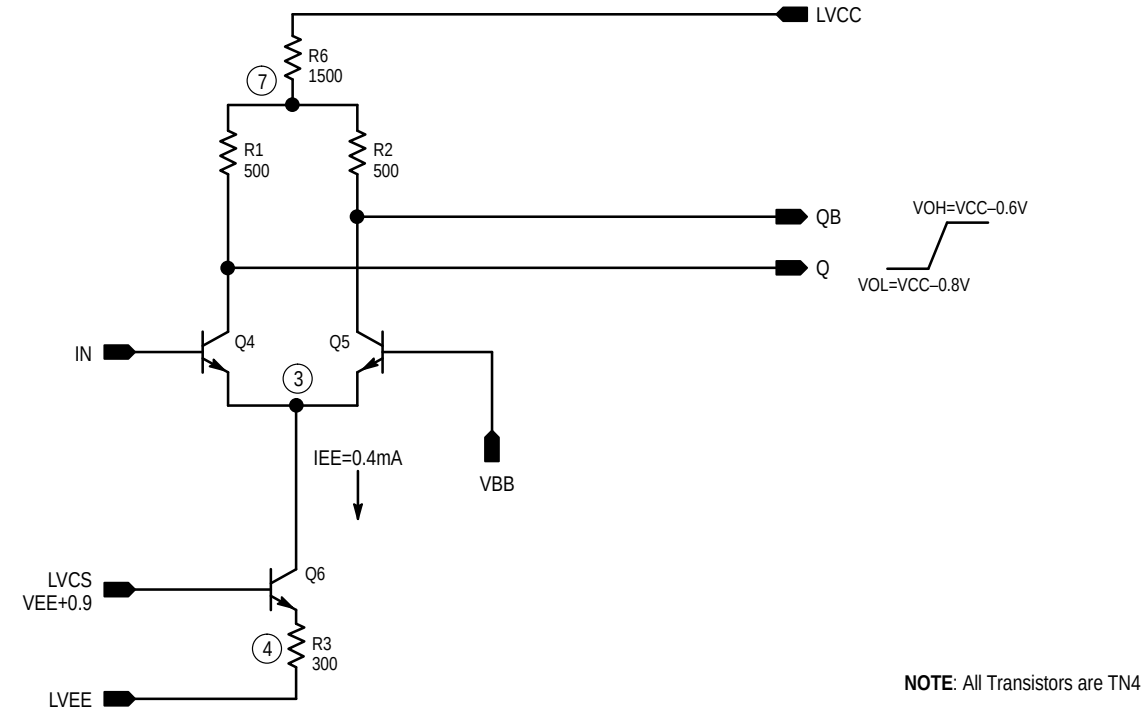


Figure 15. inBUF12 for LVEL

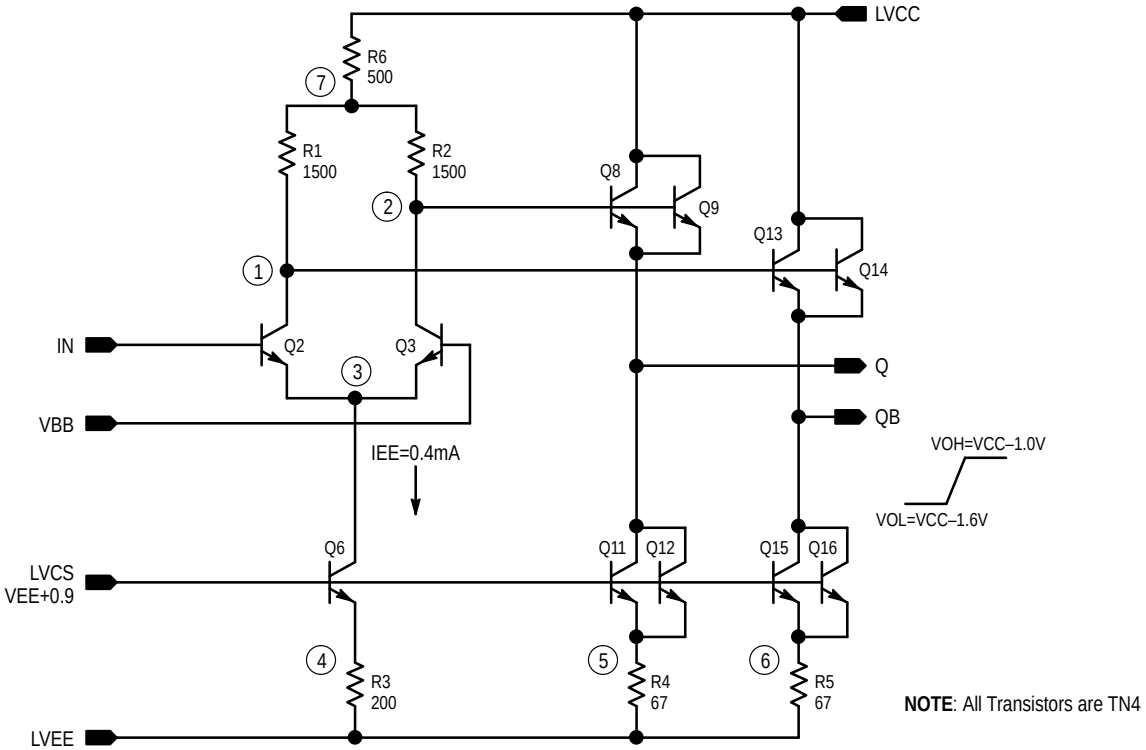


Figure 16. inBUF13 for LVEL

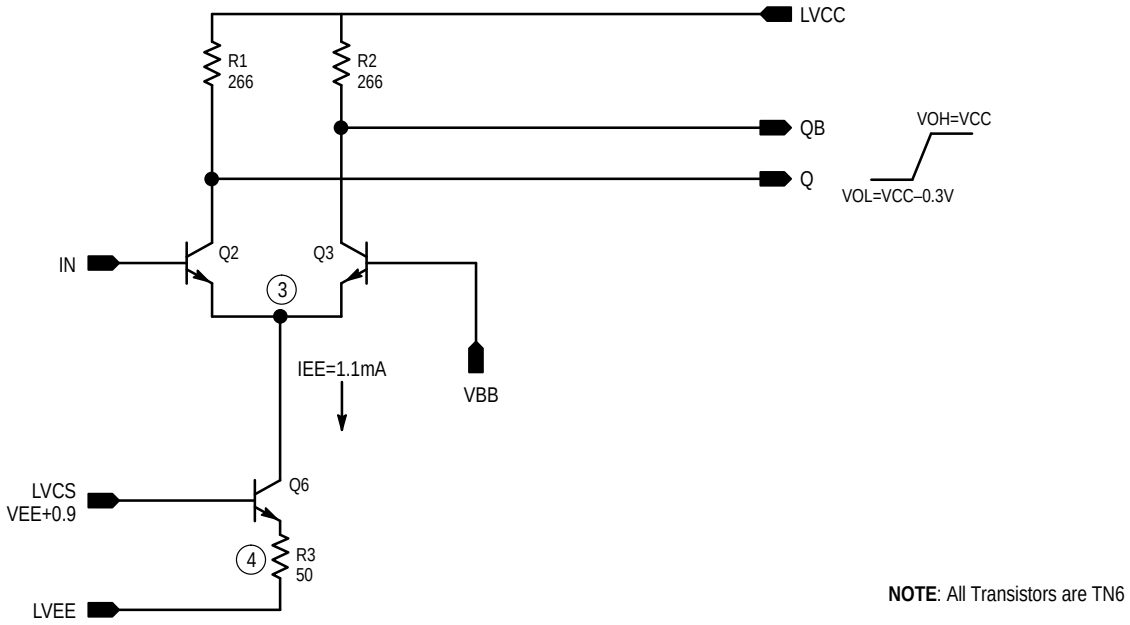


Figure 17. inBUF14 for LVEL

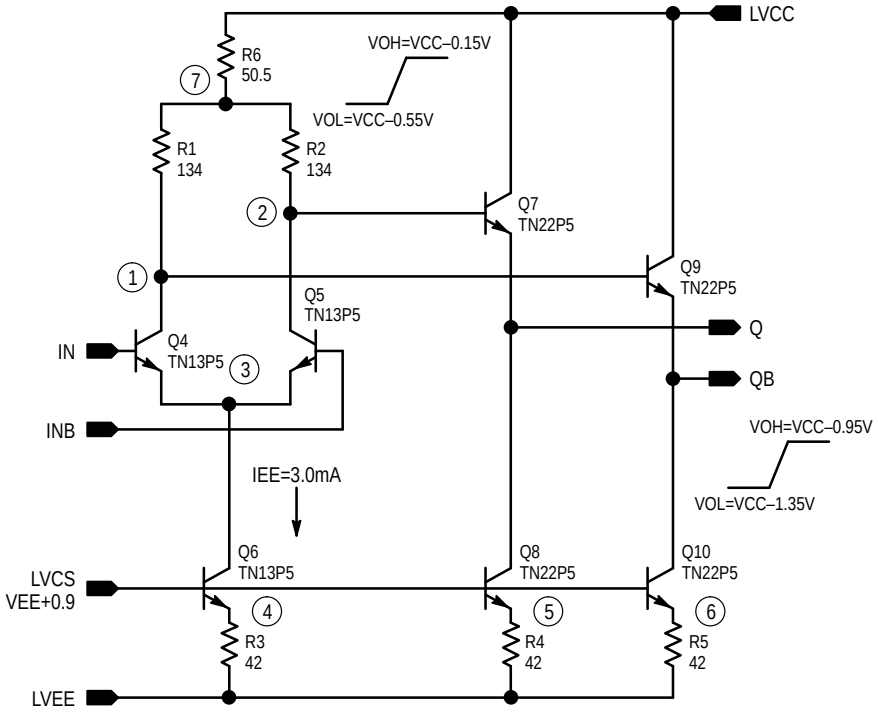
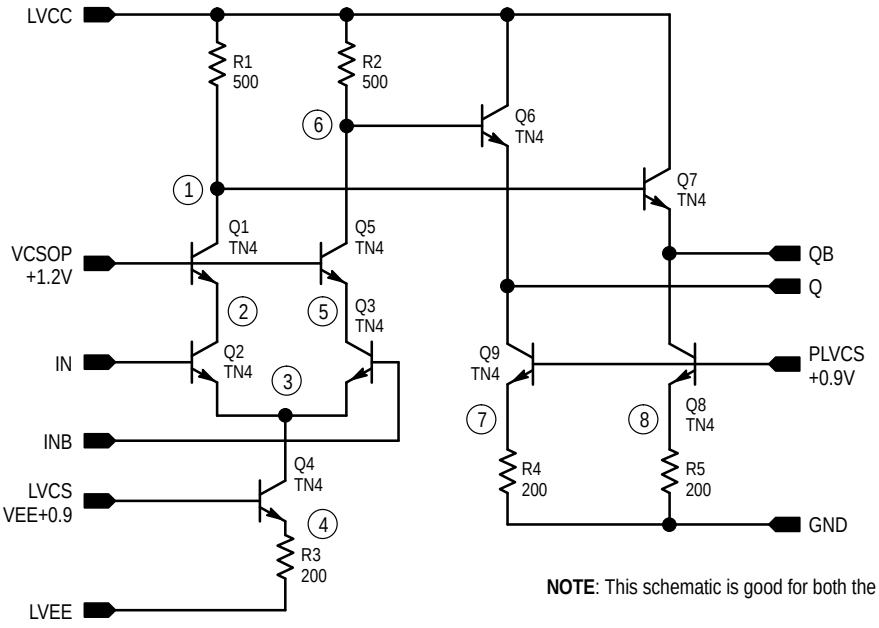


Figure 18. inBUFxxx for LVE



NOTE: This schematic is good for both the LVEL and EL90 devices.

Figure 19. MC100LVEL90 Input inBUF17

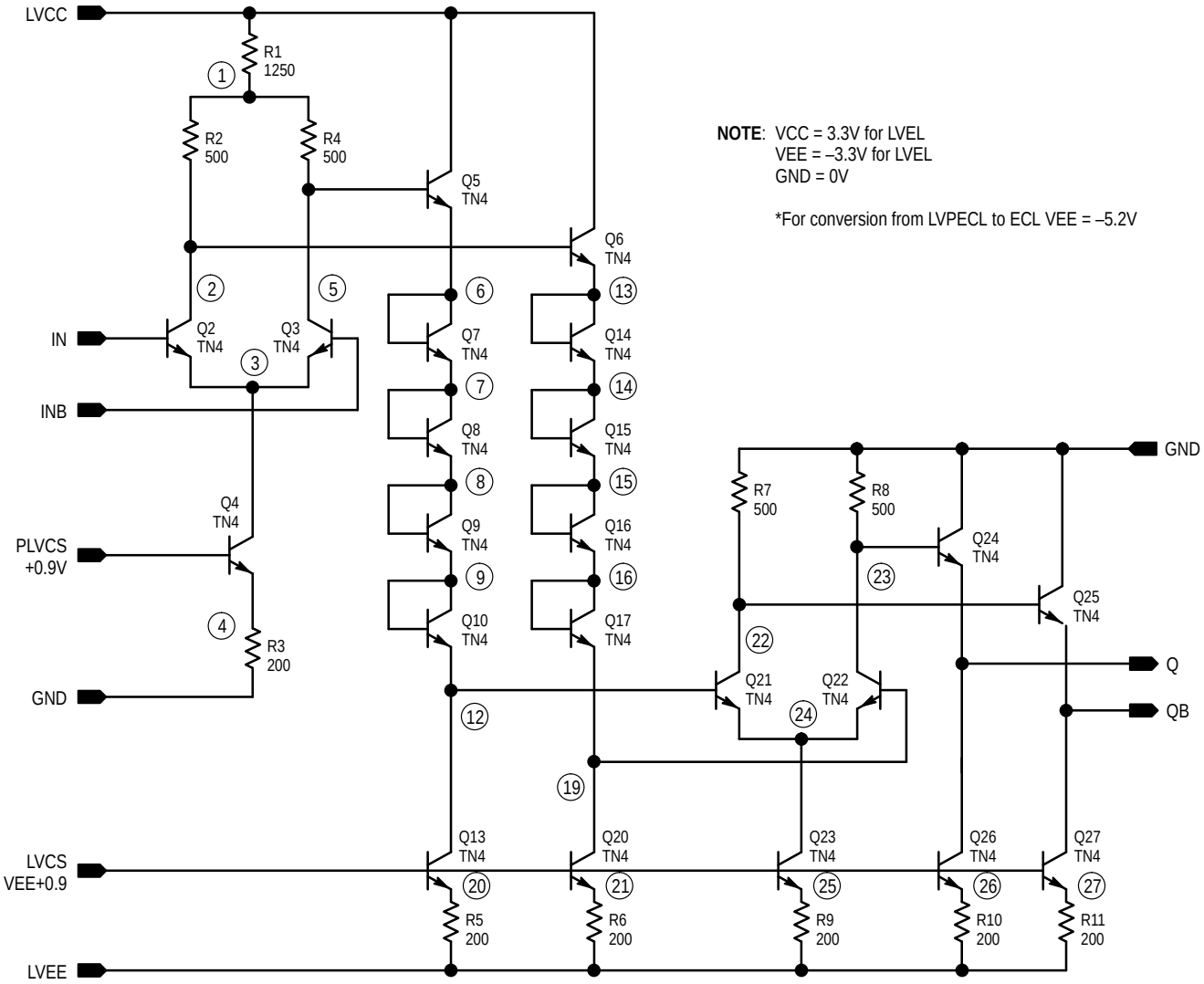


Figure 20. MC100LVEL91 Input inBUF19

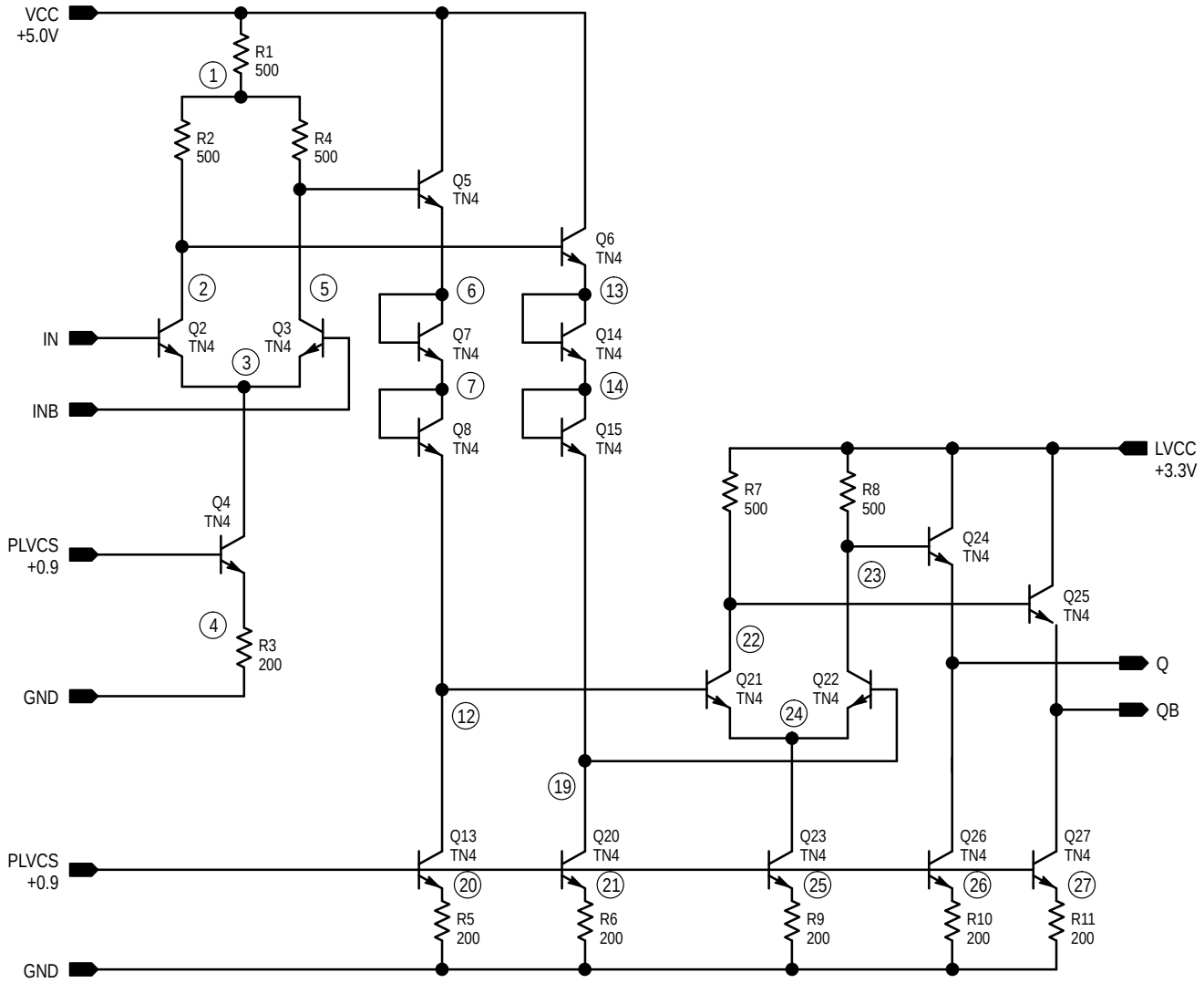


Figure 21. MC100LVEL92 Input inBUF21

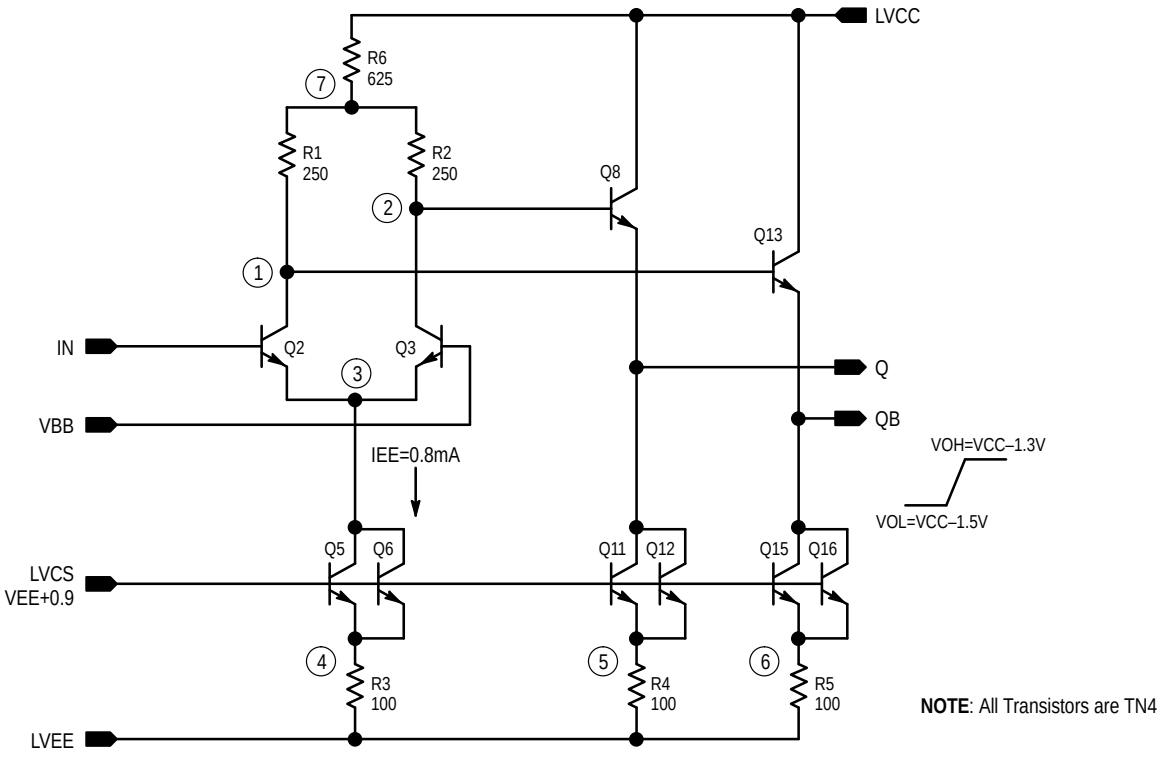


Figure 22. inBUF15 for LVE

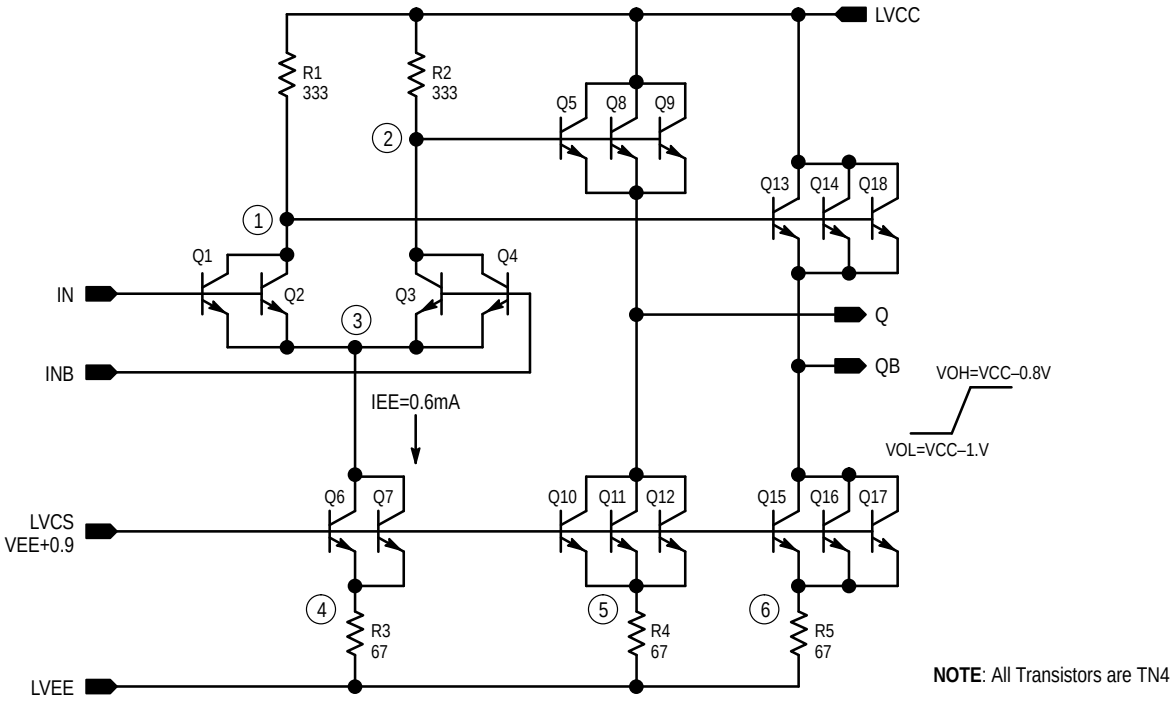


Figure 23. inBUF16 for LVE

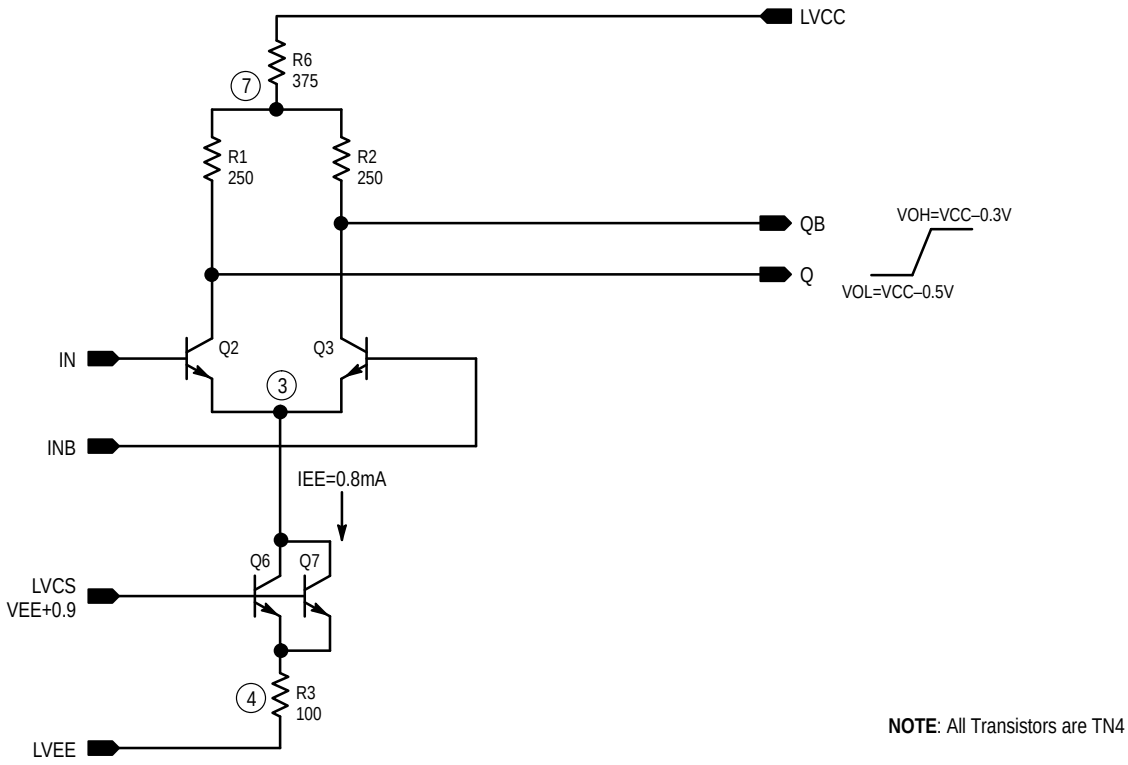


Figure 24. inBUF22 for LVE

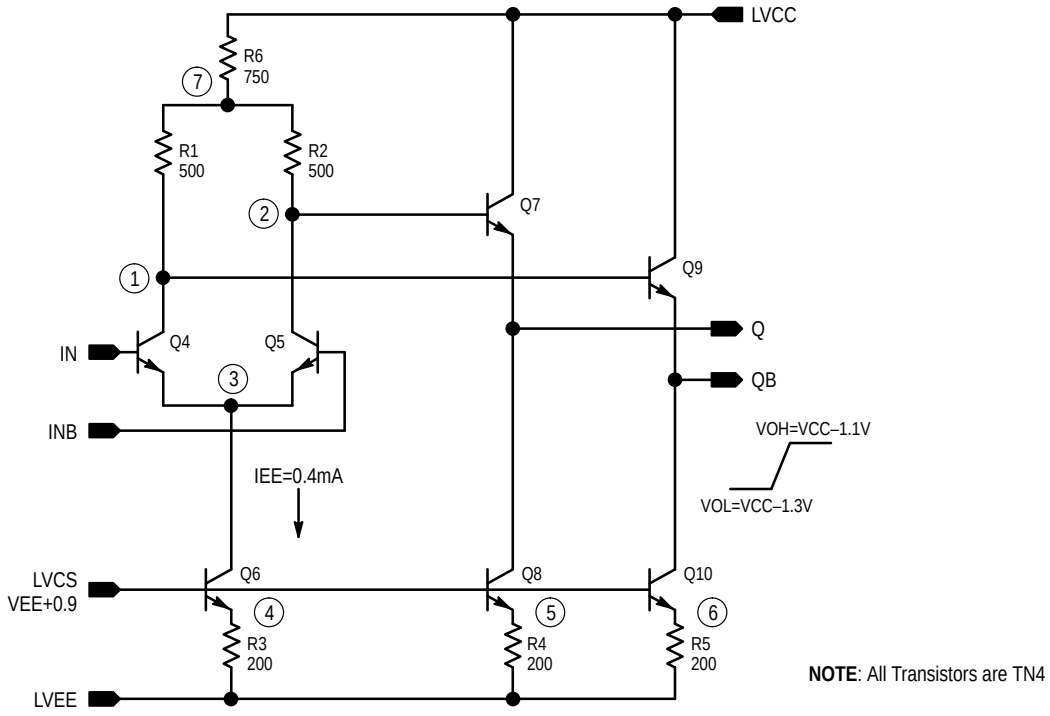


Figure 25. inBUF23 for LVE

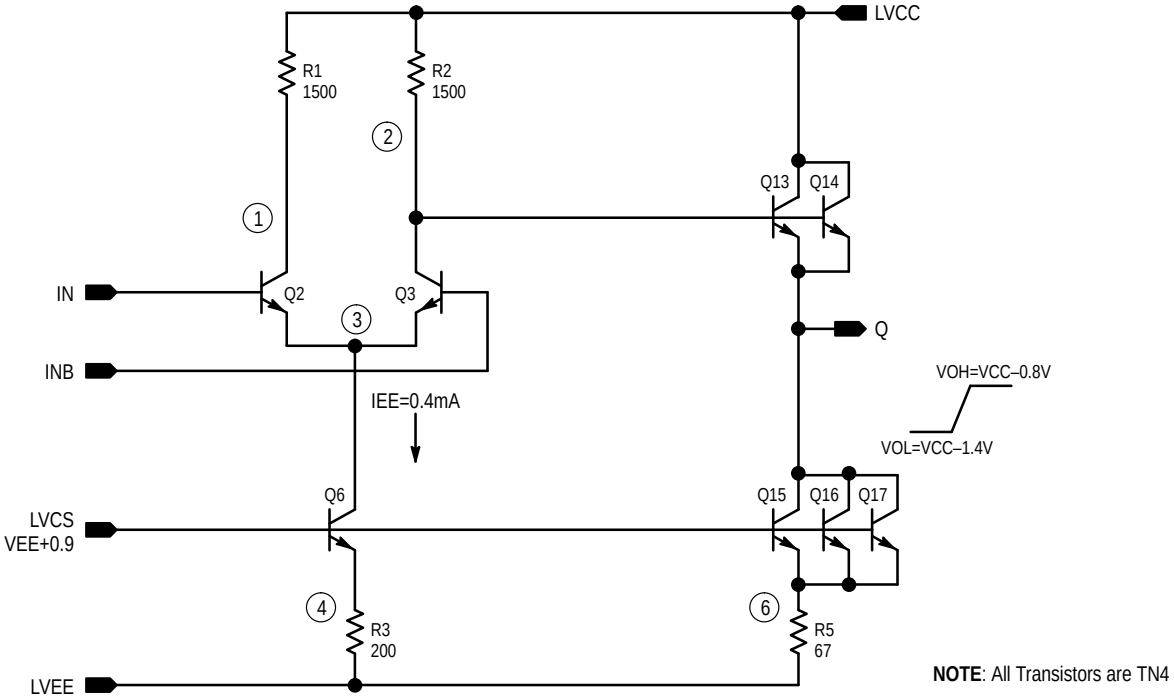


Figure 26. inBUF24 for LVE

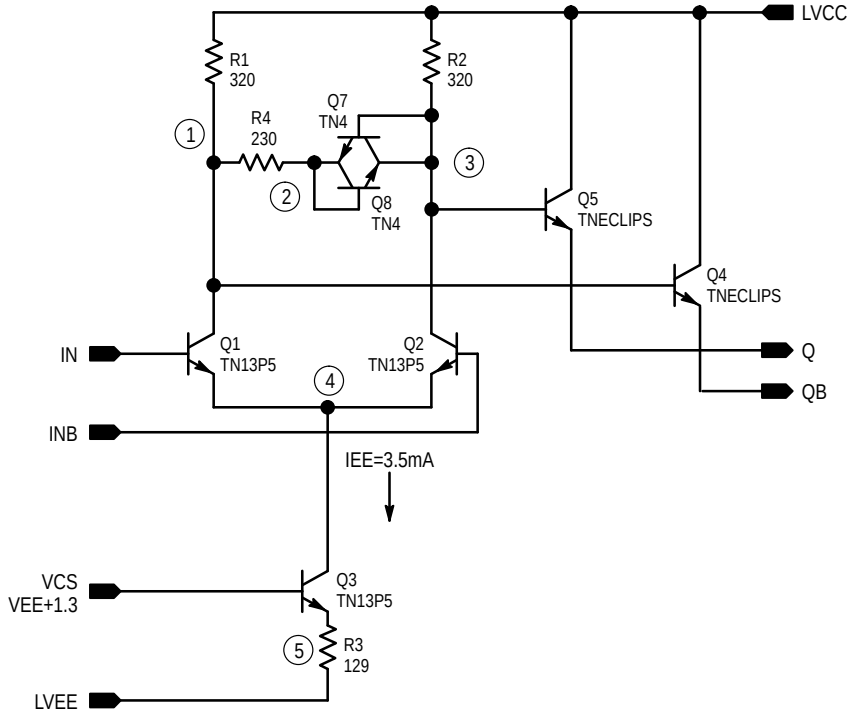


Figure 27. OBUF3.5

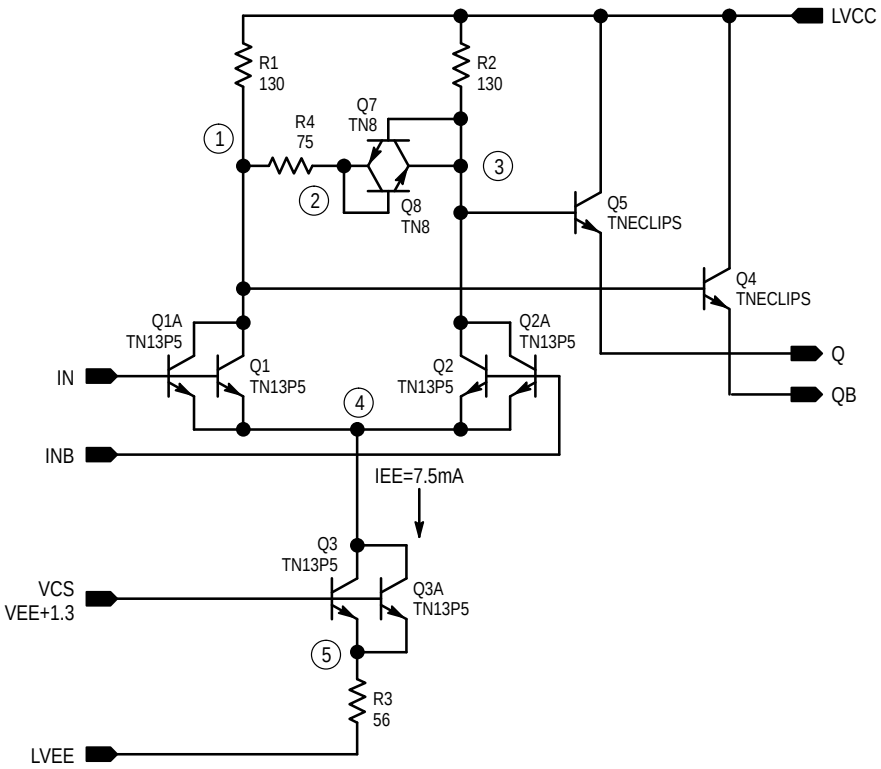


Figure 28. OBUF7.5

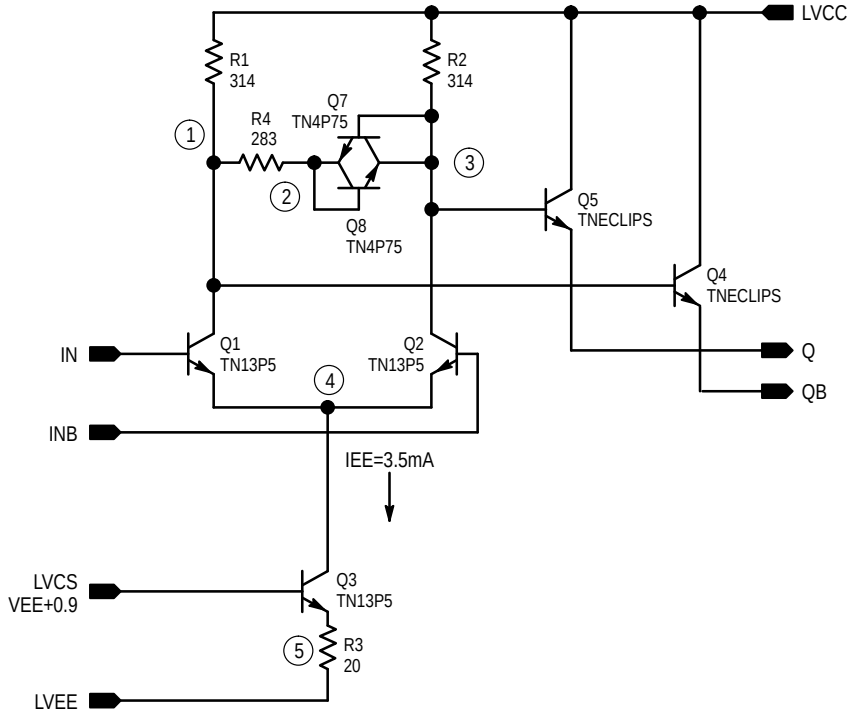


Figure 29. OBUFxxx

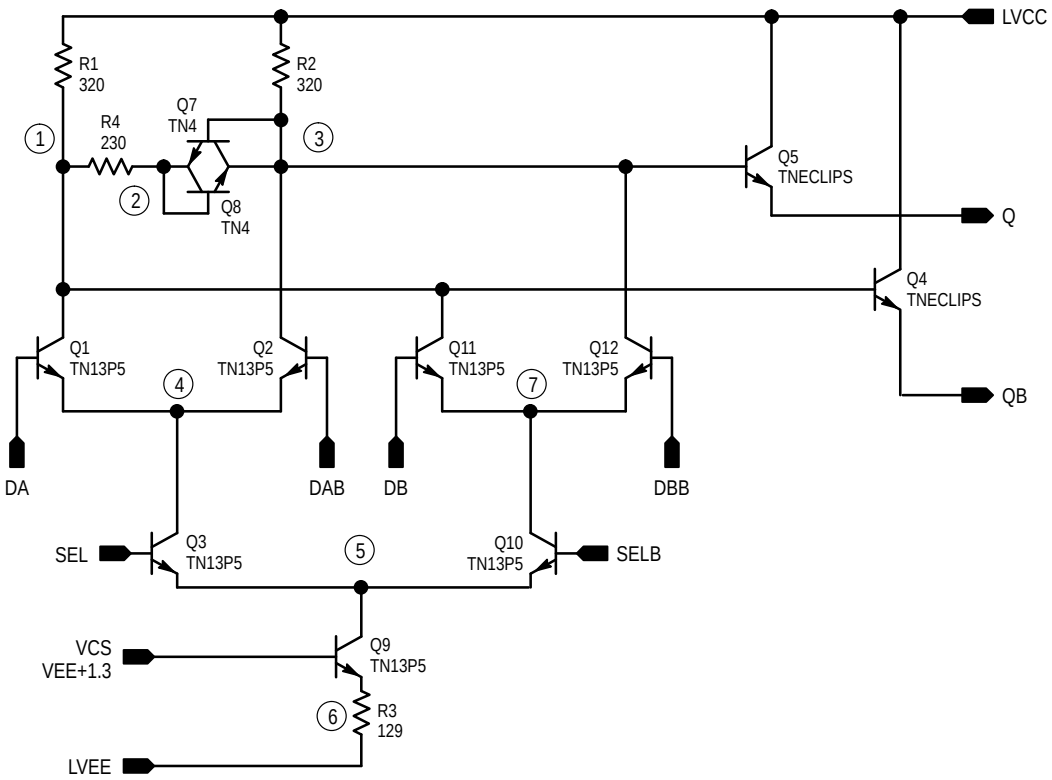


Figure 30. OMUX3.5

Spice Netlists for the MC100LVE/LVEL Devices

```
*********************************************************
*       ECLinPS I/O Modelling Kit – Netlist Schematics        *
*                                                             *
*     The purpose of this document is to provide the netlists  *
* for the various schematics supplied in the Low Voltage ECLinPS I/O SPICE *
* Modelling Kit Application Note.  This information will save  *
* design engineers who have no schematic capture tools        *
* at their disposal the task of producing the SPICE netlists   *
* for the schematics. To use these netlists it will require    *
* a copy of the Low Voltage ECLinPS I/O SPICE Modelling Kit application    *
* note.  This note is required to identify the appropriate     *
* input and output models for a specific device as well as the *
* appropriate package model and ESD structure.  In addition a  *
* copy of this note will help visualize the netlists and ease  *
* the building of the simulation circuits.  The note also      *
* provides suggestions on simulating the various Low Voltage ECLinPS and   *
* ECLinPS Lite devices.                                       *
*                                                             *
*                 Netlist Organization                        *
*                                                             *
*     The netlists are organized as a group of subcircuits so  *
* that the user can simply build a simulation netlist by       *
* calling the appropriate subcircuit models.  In this way any  *
* problems associated with commonality in node numbering       *
* or component naming due to the use of multiple copies of a   *
* schematic will be eliminated.                               *
```

```
*     There are a group of GLOBAL nodes for the schematics,    *
* they are as follows:

*               Global nodes will be:
*               LVCC =  (3.3V) FOR LVPECL AND (0V) FOR LVECL
*               LVEE = (–3.3V) FOR LVECL AND (0V) FOR LVPECL
*               VCC = (5.0V)
*               VEE = (–5.2V OR –5.0V)
*               GND = (0V)
*               VBB = ( LVCC–1.3V)
*               VCS = (VEE OR LVEE + 1.3V)
*               LVCS = (VEE OR LVEE +.9V)
*               PLVCS  = (GND +.9V)
*               VCSOP  = (GND +1.2V) USED IN THE LVEL90 INPUT
*               IN  = INPUT TO CKT
*               INB = INPUT BAR OF CKT.
*               Q = TRUE OUTPUT OF CKT.
*               QB = INVERTED OUTPUT OF CKT.

*  Notice that the subcircuit models all      *
* list these nodes in the external node list parameters.       *
* This will serve to simplify building the individual netlists *
* into interconnect simulation netlists.                       *
*     All of the subcircuits are named as to which schematic they rep–  *
* represent (ie. inBUF01) and are cross referen–    *
* ced to devices in which they are used in table (3) in the application note.  In       *
* addition all of the subcircuits list input and output nodes for    *
* the cell.  This will ease the task of interconnecting the simulation netlist.   *
* The component labels used in the netlists are identical to   *
* those on the schematics in the application note.  With the   *
* simplicity of the models this should allow the user to trace *
* the netlists back to the schematics.                         *
*     The output netlists all include the temperature compen–  *
* sation network circuitry for the 100E style in the output buffers.   *
* There will be no 10E style device in Low Voltage ECLinPS or E–Lite.
*   The user may notice that there are four terminals on       *
* the transistor models.  The fouth terminal represents the    *
* the connection to the substrate and is always biased to VEE. *
*This set of netlists are for the MC100LVE/LVEL low voltage devices and will include input and output models for both groups.*
*******************************
.SUBCKT inBUF01 LVCC LVEE LVCS VBB  IN0 IN1 IN2 IN3 Q QB
Q1 1 IN0 3 LVEE TN6
Q2 1 IN1 3 LVEE TN6
Q3 1 IN2 3 LVEE TN6
Q4 1 IN3 3 LVEE TN6
Q5 2 VBB 3 LVEE TN6
Q6 3 LVCS 4 LVEE TN6
Q7 LVCC 2 Q LVEE TN6
Q8 Q LVCS 5 LVEE TN6
Q9 LVCC 1 QB LVEE TN6
Q10 QB LVCS 6 LVEE TN6
R1 LVCC 1 133
R2 LVCC 2 133
R3 4 LVEE 25
R4 5 LVEE 25
R5 6 LVEE 25
.END inBUF01
*********************************************
.SUBCKT inBUF02 LVCC LVEE LVCS IN INB Q QB
Q4 1 IN 3 LVEE TN6
Q5 2 INB 3 LVEE TN6
```

```
Q6 3 LVCS 4 LVEE TN6
Q7 LVCC 2 Q LVEE TN6
Q8 Q LVCS 5 LVEE TN6
Q9 LVCC 1 QB LVEE TN6
Q10 QB LVCS 6 LVEE TN6
R1 LVCC 1 133
R2 LVCC 2 133
R3 4 LVEE 25
R5 5 LVEE 25
R5 6 LVEE 25
.END inBUF02
*****************************************
.SUBCKT inBUF03 LVCC LVEE LVCS IN INB Q QB
Q1 1 IN 3 LVEE TN4
Q2 1 IN 3 LVEE TN4
Q3 2 INB 3 LVEE TN4
Q4 2 INB 3 LVEE TN4
Q5 3 LVCS 4 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 3 LVCS 3 LVEE TN4
Q8 LVCC 2 Q LVEE TN4
Q9 LVCC 2 Q LVEE TN4
Q10 Q LVCS 5 LVEE TN4
Q11 Q LVCS 5 LVEE TN4
Q12 Q LVCS 5 LVEE TN4
Q13 LVCC 1 QB LVEE TN4
Q14 LVCC 1 QB LVEE TN4
Q15 QB LVCS 6 LVEE TN4
Q16 QB LVCS 6 LVEE TN4
Q17 QB LVCS 6 LVEE TN4
R1 LVCC 1 167
R2 LVCC 2 167
R3 4 LVEE 67
R4 5 LVEE 67
R5 6 LVEE 67
.END inBUF03
*****************************************************
.SUBCKT inBUF04 LVCC LVEE LVCS IN INB Q QB
Q1 Q LVCS 5 LVEE TN4
Q2 QB LVCS 6 LVEE TN4
Q4 1 IN 3 LVEE TN4
Q5 2 INB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 LVCC 2 Q LVEE TN4
Q8 Q LVCS 5 LVEE TN4
Q9 LVCC 1 QB LVEE TN4
Q10 QB LVCS 6 LVEE TN4
R1 LVCC 1 250
R2 LVCC 2 250
R3 4 LVEE 100
R4 5 LVEE 100
R5 6 LVEE 100
.END inBUF04
*****************************************************
.SUBCKT inBUF05 LVCC LVEE LVCS IN INB Q QB
Q4 1 IN 3 LVEE TN4
Q5 2 INB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 LVCC 2 Q LVEE TN4
Q8 Q LVCS 5 LVEE TN4
Q9 LVCC 1 QB LVEE TN4
```

```
Q10 QB LVCS 6 LVEE TN4
R1 7 1 750
R2 7 2 750
R3 4 LVEE 200
R4 5 LVEE 200
R5 6 LVEE 200
R6 LVCC 7 1250
.END inBUF05
************************************************
.SUBCKT inBUF06 LVCC LVEE LVCS IN INB Q QB
Q4 1 IN 3 LVEE TN4
Q5 2 INB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 LVCC 2 Q LVEE TN4
Q8 Q LVCS 5 LVEE TN4
Q9 LVCC 1 QB LVEE TN4
Q10 QB LVCS 6 LVEE TN4
R1 LVCC 1 500
R2 LVCC 2 500
R3 4 LVEE 200
R4 5 LVEE 200
R5 6 LVEE 200
.END inBUF06
**********************************
.SUBCKT inBUF07 LVCC  LVEE LVCS IN INB Q QB
Q1 1 IN 3 LVEE TN4
Q2 1 IN 3 LVEE TN4
Q3 2 INB 3 LVEE TN4
Q4 2 INB 3 LVEE TN4
Q5 3 LVCS 4 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 3 LVCS 4 LVEE TN4
Q8 LVCC 2 Q LVEE TN4
Q9 LVCC 2 Q LVEE TN4
Q10 Q LVCS 5 LVEE TN4
Q11 Q LVCS 5 LVEE TN4
Q12 Q LVCS 5 LVEE TN4
Q13 LVCC 1 QB LVEE TN4
Q14 LVCC 1 QB LVEE TN4
Q15 QB LVCS 6 LVEE TN4
Q16 QB LVCS 6 LVEE TN4
Q17 QB LVCS 6 LVEE TN4
R1 7 1 250
R2 7 2 250
R3 4 LVEE 100
R4 5 LVEE 67
R5 6 LVEE 67
R6 LVCC 7 750
.END inBUF07
*****************************************
.SUBCKT inBUF08 LVCC LVEE LVCS IN INB Q QB
Q1 1 IN 3 LVEE TN4
Q2 1 IN 3 LVEE TN4
Q3 2 INB 3 LVEE TN4
Q4 2 INB 3 LVEE TN4
Q5 3 LVCS 4 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 3 LVCS 4 LVEE TN4
Q8 LVCC 2 Q LVEE TN4
Q9 LVCC 2 Q LVEE TN4
Q10 Q LVCS 5 LVEE TN4
```

```
Q11 Q LVCS 5 LVEE TN4
Q12 Q LVCS 5 LVEE TN4
Q13 LVCC 1 QB LVEE TN4
Q14 LVCC 1 QB LVEE TN4
Q15 QB LVCS 6 LVEE TN4
Q16 QB LVCS 6 LVEE TN4
Q17 QB LVCS 6 LVEE TN4
R1 7 1 750
R2 7 2 750
R3 4 LVEE 100
R4 5 LVEE 67
R5 6 LVEE 67
R6 LVCC 7 375
.END inBUF08
*****************************************************
.SUBCKT inBUF09 LVCC LVEE LVCS IN INB Q QB
Q4 1 IN 3 LVEE TN6
Q5 2 INB 3 LVEE TN6
Q6 3 LVCS 4 LVEE TN6
Q7 LVCC 2 Q LVEE TN6
Q8 Q LVCS 5 LVEE TN6
Q9 LVCC 1 QB LVEE TN6
Q10 QB LVCS 6 LVEE TN6
R1 7 1 133
R2 7 2 133
R3 4 LVEE 42
R4 5 LVEE 42
R5 6 LVEE 42
R6 LVCC 7 239
.END inBUF09
*****************************************************
.SUBCKT inBUF10 LVCC LVEE LVCS IN INB Q QB
Q4 1 IN 3 LVEE TN6
Q5 2 INB 3 LVEE TN6
Q6 3 LVCS 4 LVEE TN6
Q7 LVCC 2 Q LVEE TN6
Q8 Q LVCS 5 LVEE TN6
Q9 LVCC 1 QB LVEE TN6
Q10 QB LVCS 6 LVEE TN6
R1 LVCC 1 478
R2 LVCC 2 478
R3 4 LVEE 42
R4 5 LVEE 42
R5 6 LVEE 42
.END inBUF10
***********************************
.SUBCKT inBUF11 LVCC LVEE LVCS IN INB Q QB
Q2 1 IN 3 LVEE TN4
Q3 2 INB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q8 LVCC 2 Q LVEE TN4
Q9 LVCC 2 Q LVEE TN4
Q11 Q LVCS 5 LVEE TN4
Q12 Q LVCS 5 LVEE TN4
Q13 LVCC 1 QB LVEE TN4
Q14 LVCC 1 QB LVEE TN4
Q15 QB LVCS 6 LVEE TN4
Q16 QB LVCS 6 LVEE TN4
R1 7 1 500
R2 7 2 500
R3 4 LVEE 200
```

```
R4 5 LVEE 67
R5 6 LVEE 67
R6 LVCC 7 1000
.END inBUF11
*******************************************************
.SUBCKT inBUF12 LVCC LVEE LVCS IN VBB Q QB
Q2 Q IN 3 LVEE TN4
Q3 QB VBB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
R1 7 Q 500
R2 7 QB 500
R3 4 LVEE 200
R6 LVCC 7 1500
.END inBUF12
*******************************************************
.SUBCKT inBUF13 LVCC LVEE LVCS IN VBB Q QB
Q2 1 IN 3 LVEE TN4
Q3 2 VBB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q8 LVCC 2 Q LVEE TN4
Q9 LVCC 2 Q LVEE TN4
Q11 Q LVCS 5 LVEE TN4
Q12 Q LVCS 5 LVEE TN4
Q13 LVCC 1 QB LVEE TN4
Q14 LVCC 1 QB LVEE TN4
Q15 QB LVCS 6 LVEE TN4
Q16 QB LVCS 6 LVEE TN4
R1 7 1 1500
R2 7 2 1500
R3 4 LVEE 200
R4 5 LVEE 67
R5 6 LVEE 67
R6 LVCC 7 500
.END inBUF13
*******************************************************
.SUBCKT inBUF14 LVCC LVEE LVCS VBB IN  Q QB
Q2 Q IN 3 LVEE TN6
Q3 QB VBB 3 LVEE TN6
Q6 3 LVCS 4 LVEE TN6
R1 LVCC Q 266
R2 LVCC QB 266
R3 4 LVEE 50
.END inBUF14
*******************************************************
.SUBCKT inBUF15 LVCC LVEE LVCS IN VBB Q QB
Q2 1 IN 3 LVEE TN4
Q3 2 VBB 3 LVEE TN4
Q5 3 LVCS 4 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q8 LVCC 2 Q LVEE TN4
Q11 Q LVCS 5 LVEE TN4
Q12 Q LVCS 5 LVEE TN4
Q13 LVCC 1 QB LVEE TN4
Q15 QB LVCS 6 LVEE TN4
Q16 QB LVCS 6 LVEE TN4
R1 7 1 250
R2 7 2 250
R3 4 LVEE 100
R4 5 LVEE 100
R5 6 LVEE 100
```

```
R6 LVCC 7 625
.END inBUF15
************************************************
.SUBCKT inBUF16 LVCC LVEE LVCS IN INB Q QB
Q1 1 IN 3 LVEE TN4
Q2 1 IN 3 LVEE TN4
Q3 2 INB 3 LVEE TN4
Q4 2 INB 3 LVEE TN4
Q5 LVCC 2 Q LVEE TN4
Q8 LVCC 2 Q LVEE TN4
Q9 LVCC 2 Q LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 3 LVCS 4 LVEE TN4
Q10 Q LVCS 5 LVEE TN4
Q11 Q LVCS 5 LVEE TN4
Q12 Q LVCS 5 LVEE TN4
Q13 LVCC 1 QB LVEE TN4
Q14 LVCC 1 QB LVEE TN4
Q18 LVCC 1 QB LVEE TN4
Q15 QB LVCS 6 LVEE TN4
Q16 QB LVCS 6 LVEE TN4
Q17 QB LVCS 6 LVEE TN4
R1 LVCC 1 333
R2 LVCC 2 333
R3 4 LVEE 67
R4 5 LVEE 67
R5 6 LVEE 67
.END inBUF16
************************************************
.SUBCKT inBUF22 LVCC LVEE LVCS IN INB Q QB
Q2 Q IN 3 LVEE TN4
Q3 QB INB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 3 LVCS 4 LVEE TN4
R1 7 Q 250
R2 7 QB 250
R3 4 LVEE 100
R6 LVCC 7 375
.END inBUF22
************************************************
.SUBCKT inBUF23 LVCC LVEE LVCS IN INB Q QB
Q4 1 IN 3 LVEE TN4
Q5 2 INB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q7 LVCC 2 Q LVEE TN4
Q8 Q LVCS 5 LVEE TN4
Q9 LVCC 1 QB LVEE TN4
Q10 QB LVCS 6 LVEE TN4
R1 7 1 500
R2 7 2 500
R3 4 LVEE 200
R4 5 LVEE 200
R5 6 LVEE 200
R6 LVCC 7 750
.END inBUF23
************************************************
.SUBCKT inBUF24 LVCC LVEE LVCS IN INB Q
Q2 1 IN 3 LVEE TN4
Q3 2 INB 3 LVEE TN4
Q6 3 LVCS 4 LVEE TN4
Q13 LVCC 2 Q LVEE TN4
```

```
Q14 LVCC 2 Q LVEE TN4
Q15 Q LVCS 6 LVEE TN4
Q16 Q LVCS 6 LVEE TN4
Q17 Q LVCS 6 LVEE TN4
R1 LVCC 1 1500
R2 LVCC 2 1500
R3 4 LVEE 200
R5 6 LVEE 67
.END inBUF24
*****************************************************
** THE FOLLOWING IS THE INPUT FOR THE MC10/100EL/LVEL90 AND IS USEFUL AT 5V VCC, –5.2V VEE FOR ECL TO PECL. AT 3.3V VCC , –5.2 VEE,  FOR ECL TO LVPECL. AT 5V VCC, –3.3V VEE FOR LVECL TO PECL AND 3.3V VCC, –3.3V VEE FOR LVECL TO LVPECL.
.SUBCKT inBUF17 LVCC LVEE GND LVCS PLVCS VCSOP IN INB Q QB
Q1 1 VCSOP 2 LVEE TN4
Q2 2 IN 3 LVEE TN4
Q3 5 INB 3 LVEE TN4
Q4 3 LVCS 4 LVEE TN4
Q5 6 VCSOP 5 LVEE TN4
Q6 LVCC 6 Q LVEE TN4
Q7 LVCC 1 QB LVEE TN4
Q8 QB PLVCS 8 LVEE TN4
Q9 Q PLVCS 7 LVEE TN4
R1 LVCC 1 500
R2 LVCC 6 500
R3 4 LVEE 200
R4 7 GND 200
R5 8 GND 200
.END inBUF17
*********************************************************
** THE FOLLOWING IS THE INPUT FOR THE MC100LVEL91 AND IS USEFUL AT 3.3V VCC, –3.3V, VEE FOR LVPECL TO LVECL *AND 3.3V VCC, –5.2V VEE FOR LVPECL TO ECL.
.SUBCKT inBUF19 LVCC LVEE GND LVCS PLVCS IN INB Q QB
Q2 2 IN 3 LVEE TN4
Q3 5 INB 3 LVEE TN4
Q4 3 PLVCS 4 LVEE TN4
Q5 LVCC 5 6 LVEE TN4
Q6 LVCC 2 13 LVEE TN4
Q7 6 6 7 LVEE TN4
Q8 7 7 8 LVEE TN4
Q9 8 8 9 LVEE TN4
Q10 9 9 12 LVEE TN4
Q13 12 LVCS 20 LVEE TN4
Q14 13 13 14 LVEE TN4
Q15 14 14 15 LVEE TN4
Q16 15 15 16 LVEE TN4
Q17 16 16 19 LVEE TN4
Q20 19 LVCS 21 LVEE TN4
Q21 22 12 24 LVEE TN4
Q22 23 19 24 LVEE TN4
Q23 24 LVCS 25 LVEE TN4
Q24 GND 23 Q LVEE TN4
Q25 GND 22 QB LVEE TN4
Q26 Q LVCS 26 LVEE TN4
Q27 QB LVCS 27 LVEE TN4
R1 LVCC 1 1250
R2 1 2 500
R3 4 GND 200
R4 1 5 500
R5 20 LVEE 200
R6 21 LVEE 200
```

```
R7 GND 22 500
R8 GND 23 500
R9 25 LVEE 200
R10 26 LVEE 200
R11 27 LVEE 200
.END inBUF19
************************************************************
**** THE FOLLOWING IS USED FOR THE INPUT OF THE MC100EL92 AND IT CONVERTS A PECL INPUT TO A LVPECL
*OUTPUT (5V PECL TO A 3.3V LVPECL). IT REQUIRES A 5V VCC, GND AND A 3.3V LVCC.
.SUBCKT inBUF21 VCC LVCC GND PLVCS IN INB Q QB
Q2 2 IN 3 GND TN4
Q3 5 INB 3 GND TN4
Q4 3 PLVCS 4 GND TN4
Q5 VCC 5 6 GND TN4
Q6 VCC 2 13 GND TN4
Q7 6 6 7 GND TN4
Q8 7 7 12 GND TN4
Q13 12 PLVCS 20 GND TN4
Q14 13 13 14 GND TN4
Q15 14 14 19 GND TN4
Q20 19 PLVCS 21 GND TN4
Q21 22 12 24 GND TN4
Q22 23 19 24 GND TN4
Q23 24 PLVCS 25 GND TN4
Q24 LVCC 23 Q GND TN4
Q25 LVCC 22 QB GND TN4
Q26 Q PLVCS 26 GND TN4
Q27 QB PLVCS 27 GND TN4
R1 VCC 1 500
R2 1 2 500
R3 4 GND 200
R4 1 5 500
R5 20 GND 200
R6 21 GND 200
R7 LVCC 22 500
R8 LVCC 23 500
R9 25 GND 200
R10 26 GND 200
R11 27 GND 200
.END inBUF21
************************************************
.SUBCKT inBUFXXX LVCC LVEE LVCS IN INB Q QB
Q4 1 IN 3 LVEE TN13P5
Q5 2 INB 3 LVEE TN13P5
Q6 3 LVCS 4 LVEE TN13P5
Q7 LVCC 2 Q LVEE TN22P5
Q8 Q LVCS 5 LVEE TN22P5
Q9 LVCC 1 QB LVEE TN22P5
Q10 QB LVCS 6 LVEE TN22P5
R1 7 1 134
R2 7 2 134
R3 4 LVEE 20
R4 5 LVEE 42
R5 6 LVEE 42
R6 LVCC 7 50.5
.END inBUFXXX
************************************************
.SUBCKT OBUFF3.5 LVCC LVEE VCS IN INB Q QB
Q1 1 IN 4 LVEE TN13P5
Q2 3 INB 4 LVEE TN13P5
Q3 4 VCS 5 LVEE TN13P5
```

```
Q4 LVCC 1 QB LVEE TNECLIPS
Q5 LVCC 3 Q LVEE TNECLIPS
Q7 3 3 2 LVEE TN4
Q8 2 2 3 LVEE TN4
R1 LVCC 1 320
R2 LVCC 3 320
R3 5 LVEE 129
R4 1 2 230
.END OBUFF3.5
************************************************
.SUBCKT OBUFF7.5 LVCC LVEE VCS IN INB Q QB
Q1 1 IN 4 LVEE TN13P5
Q1A 1 IN 4 LVEE TN13P5
Q2 3 INB 4 LVEE TN13P5
Q2A 3 INB 4 LVEE TN1EP5
Q3 4 VCS 5 LVEE TN13P5
Q3A 4 VCS 5 LVEE TN13P5
Q4 LVCC 1 QB LVEE TNECLIPS
Q5 LVCC 3 Q LVEE TNECLIPS
Q7 3 3 2 LVEE TN8
Q8 2 2 3 LVEE TN8
R1 LVCC 1 130
R2 LVCC 3 130
R3 5 LVEE 56
R4 1 2 75
.END OBUFF7.5
************************************************************
.SUBCKT OBUFFXXX LVCC LVEE LVCS IN INB Q QB
Q1 1 IN 4 LVEE TN13P5
Q2 3 INB 4 LVEE TN13P5
Q3 4 LVCS 5 LVEE TN13P5
Q4 LVCC 1 QB LVEE TNECLIPS
Q5 LVCC 3 Q LVEE TNECLIPS
R1 LVCC 1 314
R2 LVCC 3 314
R3 5 LVEE 20
R4 1 2 283
.END OBUFFXXX
************************************************
.SUBCKT OMUX3.5 LVCC LVEE VCS DA DAB DB DBB SEL SELB Q QB
Q1 1 DA 4 LVEE TN13P5
Q2 3 DAB 4 LVEE TN13P5
Q3 4 SEL 5 LVEE TN13P5
Q4 LVCC 1 QB LVEE TNECLIPS
Q5 LVCC 3 Q LVEE TNECLIPS
Q7 3 3 2 LVEE TN4
Q8 2 2 3 LVEE TN4
Q9 5 VCS 6 LVEE TN13P5
Q10 7 SELB 5 LVEE TN13P5
Q11 1 DB 7 LVEE TN13P5
Q12 3 DBB 7 LVEE TN13P5
R1 LVCC 1 320
R2 LVCC 3 320
R3 6 LVEE 129
R4 1 2 230
.END OMUX3.5
************************************************
* ESD STRUCTURES
***NODES
*PIN –end attached to the package
*CKT–end attached to ckt input
```

```
*VEE –is attached to most negative power rail
*VCC–is attached to most positive power rail
**************************************************
**USE for the IN pin of a differential pair
.SUBCKT IN_ESD VCC VEE PIN CKT
DESD1 PIN VCC CBVCC
DESD2 PIN VCC CBVCC
DESD3 VEE PIN CBSUB
DESD4 VEE PIN CBSUB
R1 PIN CKT 1
R2 PIN VEE 75K
.END IN_ESD
**************************************************
**USE for the INB pin of a differential pair
.SUBCKT INB_ESD VCC VEE PIN CKT
DESD1 PIN VCC CBVCC
DESD2 PIN VCC CBVCC
DESD3 VEE PIN CBSUB
DESD4 VEE PIN CBSUB
R1 PIN CKT 1
R2 PIN VEE 75K
R3 VCC PIN 75K
.END INB_ESD
**************************************************
**USE for the output
.SUBCKT OUT_ESD VCC VEE PIN CKT
DESD1 PIN VCC CBVCC
DESD2 PIN VCC CBVCC
DESD3 VEE PIN CBSUB
DESD4 VEE PIN CBSUB
R1 PIN CKT 1
.END OUT_ESD
**************************************************
**USE for VBB pins
.SUBCKT VBB_ESD VCC VEE PIN CKT
DESD1 PIN VCC CBVCC
DESD2 PIN VCC CBVCC
DESD3 VEE PIN CBSUB
DESD4 VEE PIN CBSUB
R1 PIN CKT 125
.END VBB_ESD
**************************************************
**********          Package Models         **********
*                                          *
*                                          *
* Package Model (28–lead PLCC)                    *
* EXT = (External Input to Pin) INT = (Internal Output of the Pin) GND = (0V)                    *
********************************************************** ********
.SUBCKT PKG28 EXT INT GND
CPKG 82 GND 1.5PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT .2
LPKG1 EXT 82 3.5NH
LPKG2 82 83 3.5NH
.ENDS PKG28
**********************************
********
* ECLinPS Lite Package Model (8–lead SOIC)                    *
*EXT = (External Input to Pin) INT = (Internal Output of the Pin) GND = (0V)                    *
********************************************************** ********
```

```
.SUBCKT PKG8 EXT INT GND
CPKG 82 GND 0.8PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.1
LPKG1 EXT 82 1.5NH
LPKG2 82 83 1.5NH
.ENDS PKG8
************************************************************
* Package Model (52–lead TQFP)                    *
EXT = (External Input to Pin) INT = (Internal Output of the Pin) GND = (0V)
************************************************************ ********
.SUBCKT PKG52 EXT INT GND
CPKG 82 GND 2.0PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.2
LPKG1 EXT 82 1.0NH
LPKG2 82 83 1.0NH
.ENDS PKG52
*********************************************************************
* Package Model (20–lead SOIC CENTER PIN)                    *
EXT = (External Input to Pin) INT = (Internal Output of the Pin) GND = (0V)
************************************************************ *******
.SUBCKT PKG20CP EXT INT GND
CPKG 82 GND 1.5PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.2
LPKG1 EXT 82 3.0NH
LPKG2 82 83 3.0NH
.ENDS PKG20CP
************************************************************
* Package Model (20–lead SOIC END PIN )                    *
* EXT = Node (84) INT = Node (81) GND = Node (0)                    *
EXT = (External Input to Pin) INT = (Internal Output of the Pin) GND = (0V)
************************************************************ ********
.SUBCKT PKG20EP EXT INT GND
CPKG 82 GND 2.0PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.2
LPKG1 EXT 82 4.5NH
LPKG2 82 83 4.5NH
.ENDS PKG20EP

**************Package model for 32 pin TQFP Conner Pin*********

.SUBCKT PKG32CNP EXT INT GND
CPKG 82 GND 0.38PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.1
LPKG1 EXT 82 0.85NH
LPKG2 82 83 0.85NH
.ENDS PKG32CNP

**************Package model for 32 pin TQFP Center Pin*********

.SUBCKT PKG32CP EXT INT GND
CPKG 82 GND 0.14PF
```

```
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.1
LPKG1 EXT 82 0.70NH
LPKG2 82 83 0.70NH
.ENDS PKG32CP
**********    SPICE Transistor/Diode Parameters   **************
*
*
***      1.75u x 4.0u emitter     C–EB
.MODEL TN4         NPN
+(IS  = 5.27E–18  BF  = 120   NF  = 1    VAF = 30   IKF = 6.48mA
+ ISE = 2.75E–16  BR  = 10    NE  = 2    VAR =  5   IKR = 567uA
+ IRB =  8.1uA    RB  = 461.6 RBM =142.5 RE  = 21.6 RC  = 83.1
+ CJE = 19.9fF    VJE = .9    MJE = .4             XTB = 0.73
+ CJC = 25.1fF    VJC = .67   MJC = .32  XCJC= .3
+ CJS = 49.6fF    VJS = .6    MJS = .4   FC  = .9
+ TF  = 8pS       TR  = 1nS   XTF = 10   VTF = 1.4V ITF = 17.0mA
+ ISC=0   EG=1.11   XTI=5.2   PTF=0   KF=0   AF=1   NR=1   NC=2)
*
***      1.75u x 4.75u emitter     C–EB
.MODEL TN4P75      NPN
+(IS  = 6.50E–18  BF  = 120   NF  = 1    VAF = 30   IKF = 8.0mA
+ ISE = 3.40E–16  BR  = 10    NE  = 2    VAR =  5   IKR = 700uA
+ IRB = 10.0uA    RB  = 378.5 RBM =120.0 RE  = 17.5 RC  = 74.0
+ CJE = 23.6fF    VJE = .9    MJE = .4             XTB = 0.73
+ CJC = 27.4fF    VJC = .67   MJC = .32  XCJC= .3
+ CJS = 53.8fF    VJS = .6    MJS = .4   FC  = .9
+ TF  = 8pS       TR  = 1nS   XTF = 10   VTF = 1.4V ITF = 21.0mA
+ ISC=0   EG=1.11   XTI=5.2   PTF=0   KF=0   AF=1   NR=1   NC=2)
*
***      1.75u x 6.0u emitter     C–EB
.MODEL TN6         NPN
+(IS  = 8.56E–18  BF  = 120   NF  = 1    VAF = 30   IKF = 10.5mA
+ ISE = 4.48E–16  BR  = 10    NE  = 2    VAR =  5   IKR = 922uA
+ IRB = 13.2uA    RB  = 291.4 RBM = 95.0 RE  = 13.3 RC  = 62.7
+ CJE = 29.9fF    VJE = .9    MJE = .4             XTB = 0.73
+ CJC = 31.2fF    VJC = .67   MJC = .32  XCJC= .3
+ CJS = 60.9fF    VJS = .6    MJS = .4   FC  = .9
+ TF  = 8pS       TR  = 1nS   XTF = 10   VTF = 1.4V ITF = 27.6mA
+ ISC=0   EG=1.11   XTI=5.2   PTF=0   KF=0   AF=1   NR=1   NC=2)
*
*** 1.75u x 8u emitter C–EB
.MODEL TN8       NPN
+(IS = 1.18E–17   BF =120     NF = 1    VAF =30      IKF =14.6mA
+ ISE = 6.20e–16  BR =10      NE = 2     VAR = 5       IKR =1.28mA
+ IRB = 18.2uA    RB = 213.1  RBM = 71.2 RE = 9.60    RC = 50.4
+ CJE = 39.9fF    VJE = .9      MJE = .4          XTB = 0.73
+ CJC = 37.2fF    VJC = .67    MJC = .32    XCJC = .3
+ CJS = 83.5fF    VJS =.6       MJS = .4      FC = .9
+ TF = 8pS          TR = 1nS     XTF = 10     VTF = 1.4V ITF = 48.9mA
+ ISC = 0   EG =1.11  XTI = 5.2 PTF = 0 KF = 0 AF = 1 NR = 1 NC =2)
*
***      1.75u x 9.0u emitter C–EB
.MODEL TN9    NPN
+(IS = 1.33E–17 BF = 120 NF = 1 VAF = 30 IKF =16.4mA
+ ISE = 4.96E–16 BR =10 NE =2 VAR = 5  IKR =1.43mA
+ IRB = 20.5uA RB = 202.9 RBM = 62.7 RE= 8.86 RC = 40.7
+ CJE = 44.8fF VJE = .9 MJE = .4 XTB = 0.73
+ CJC = 41.9fF VJC = .67 MJC = .32 XCJC = .3
+ CJS = 93.7fF VJS = .6 MJS = .4 FC = .9
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+ TF = 8pS TR= 1nS XTF = 10 VTF = 1.4V ITF = 55.1mA
+ ICS = 0 EG =1.11 XTI = 5.2 PTF = 0 KF =0 AF =1 NR=1 NC = 2)
*
***      1.75u x 13.5u emitter     C–EB
.MODEL TN13P5     NPN
+(IS  = 2.09E–17  BF  = 120   NF  = 1    VAF = 30   IKF = 25.7mA
+ ISE = 1.09E–15  BR  = 10    NE  = 2    VAR =  5   IKR = 2.25mA
+ IRB = 32.2uA    RB  = 122.6 RBM = 42.2 RE  = 5.44 RC  = 32.8
+ CJE = 67.4fF    VJE = .9    MJE = .4             XTB = 0.73
+ CJC = 53.8fF    VJC = .67   MJC = .32  XCJC= .3
+ CJS = 103fF     VJS = .6    MJS = .4   FC  = .9
+ TF  = 8pS       TR  = 1nS   XTF = 10   VTF = 1.4V ITF = 67.5mA
+ ISC=0   EG=1.11   XTI=5.2  PTF=0   KF=0   AF=1   NR=1   NC=2)
*
***   6 x 2.00u x 19.0u emitter     6 emitters, double collector
.MODEL TNECLIPS   NPN
+(IS  = 2.27E–16  BF  = 120   NF  = 1    VAF = 30   IKF = 279mA
+ ISE = 1.19E–14  BR  = 10    NE  = 2    VAR =  5   IKR = 24.4mA
+ IRB =  349uA    RB  = 15.98 RBM = 4.17 RE  = .501 RC  = 11.1
+ CJE = 611fF     VJE = .9    MJE = .4             XTB = 0.73
+ CJC = 440fF     VJC = .67   MJC = .32  XCJC= .3
+ CJS = 668fF     VJS = .6    MJS = .4   FC  = .9
+ TF  = 8pS       TR  = 1nS   XTF = 10   VTF = 1.4V ITF = 733mA
+ ISC=0   EG=1.11   XTI=4.0   PTF=0   KF=0   AF=1   NR=1   NC=2)
***  1.75u x 22.5u emitter C–EB
.MODEL TN22P5        NPN
+(IS  = 2.3E–17  BF  = 120   NF  = 1    VAF = 30   IKF = 41.4mA
+ ISE = 1.75E–15  BR  = 10    NE  = 2    VAR =  5   IKR = 26.5mA
+ IRB = 50uA    RB  = 75 RBM = 26 RE  = 3.5 RC  = 20
+ CJE = 104fF    VJE = .9    MJE = .4             XTB = 0.73
+ CJC = 80fF    VJC = .67   MJC = .32  XCJC= .3
+ CJS = 128fF     VJS = .6    MJS = .4   FC  = .9
+ TF  = 8pS       TR  = 1nS   XTF = 10   VTF = 1.4V ITF = 80mA
+ ISC=0   EG=1.11   XTI=5.2  PTF=0   KF=0   AF=1   NR=1   NC=2)
*

*** ECLinPS Lite ESD Diodes
.MODEL CBVCC D
+ ( IS = 1.00E–15  CJO = 527fF  Vj = 0.545  M = 0.32  BV = 14.5
+   IBV = 0.1E–6  XTI = 5  TT = 1nS )
.MODEL CBSUB D
+ ( IS = 1.00E–15  CJO = 453fF  TT = 1nS )
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