AN1559

Application Considerations for a Switched Capacitor Accelerometer

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INTRODUCTION

Today's low cost accelerometers are highly integrated devices employing features such as signal conditioning, filtering, offset compensation and self test. Combining this feature set with economical plastic packaging requires that the signal conditioning circuitry be as small as possible. One approach is to implement sampled data system and switched capacitor techniques as in the MMAS40G accelerometer.

As in all sampled data systems, precautions should be taken to avoid signal aliasing errors. This application note describes the MMAS40G accelerometer and how signal aliasing can be introduced and more importantly minimized.

BACKGROUND

What is aliasing? Simply put, aliasing is the effect of sampling a signal at an insufficient rate, thus creating another signal at a frequency that is the difference between the original signal frequency and the sampling rate. A graphical explanation of aliasing is offered in Figure 1. In this figure, the upper trace shows a 50 kHz sinusoidal waveform. Note that when sampled at a 45 kHz rate, denoted by the boxes, a sinusoidal pattern is formed. Lowpass filtering the sampled points, to create a continuous signal, produces the 5 kHz waveform shown in Figure 1 (lower). (The phase shift in the lower figure is due to the low–pass filter).

Aliased signals, like the one in Figure 1 (lower) are often unintentionally produced. Signal processing techniques are well understood and sampling rates are chosen appropriately (i.e. Nyquist criteria). However, the assumption is that the signals of interest are well characterized and have a limited bandwidth. This assumption is not always true, as in the case of wideband noise.

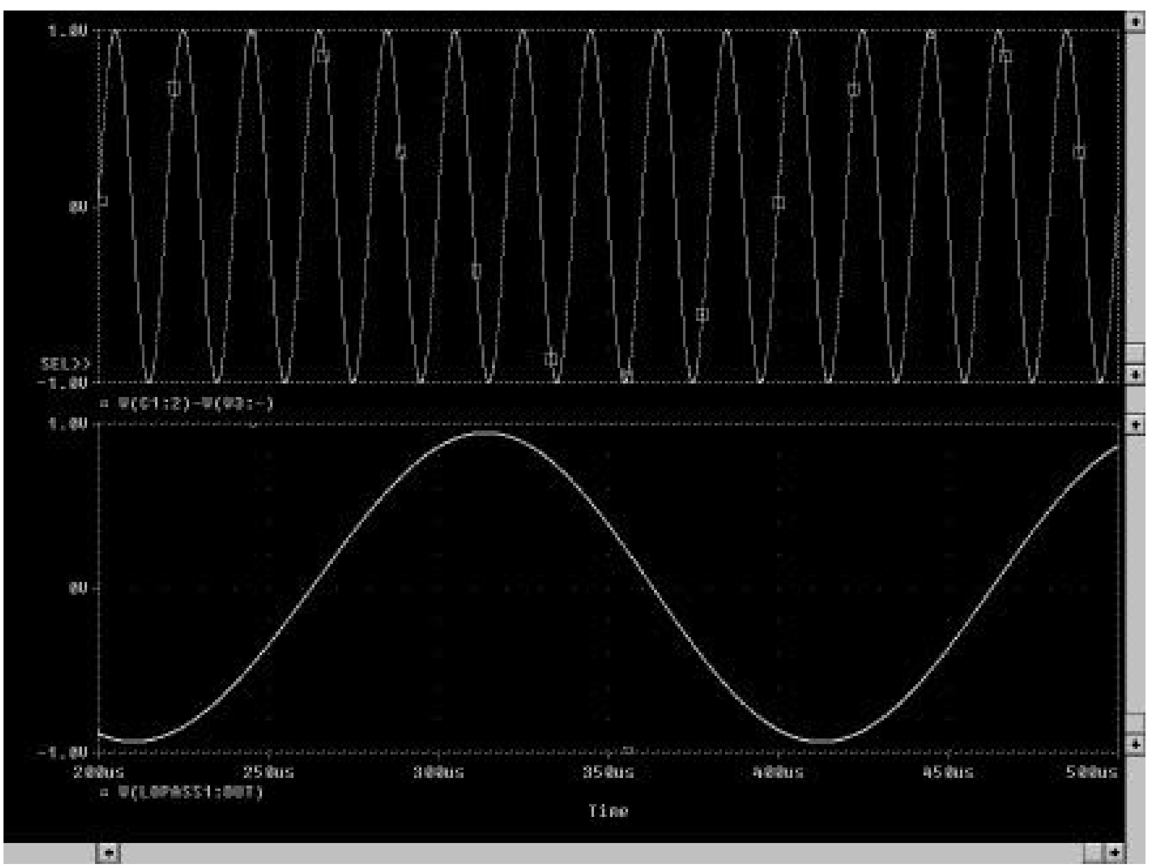


Figure 1. Aliased Signals

MOTOROLA

Given the brief example on how aliasing can occur, how does the MMAS40G accelerometer relate to aliasing? To answer this question, a brief summary on how the MMAS40G accelerometer works is in order.

The MMAS40G accelerometer is a two chip acceleration sensing solution. The first chip is the acceleration transducer, termed G–Cell, constructed by Micro Electro–Mechanical Systems (MEMS) technology. The G–Cell is a two capacitor element where the capacitors are in series and share a common center plate. The deflection in the center plate changes the capacitance of each capacitor which is measured by the second chip, termed control chip.

The control chip performs the signal conditioning (amplification, filtering, offset level shift) function in the system. This chip measures the G–Cell output using switched capacitor techniques. By the nature of switched cap techniques, the system is a sampled data system operating at sampling frequency f_S. The filter is switched capacitor, 4–pole Bessel implementation with a –3 dB frequency of 400 Hz.

As a sampled data system, the MMAS40G accelerometer is not immune to signal aliasing. However, given the accelerometer's internal filter, aliased signals will only appear in the output passband when input signals are in the range $|n \bullet f_S - f_{signal}| \leq f_{BW}$. Where f_S is the sampling rate, f_{Signal} is the input signal frequency, f_{BW} is the filter bandwidth and n is a positive integer to account for all harmonics. The graphical representation is shown in Figure 2. The bounds can be extended beyond f_{BW} to ensure an alias free output.

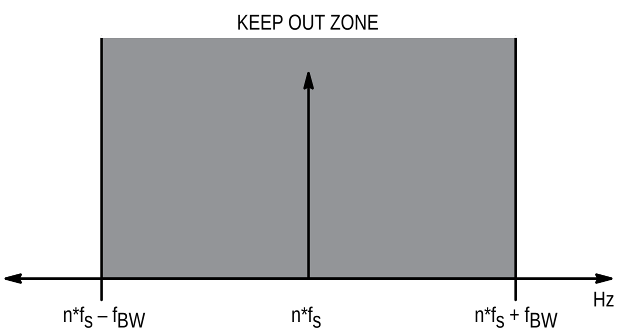


Figure 2. Input signal frequency range where a signal will be produced in the output passband.

ACCELEROMETER INPUT SIGNALS

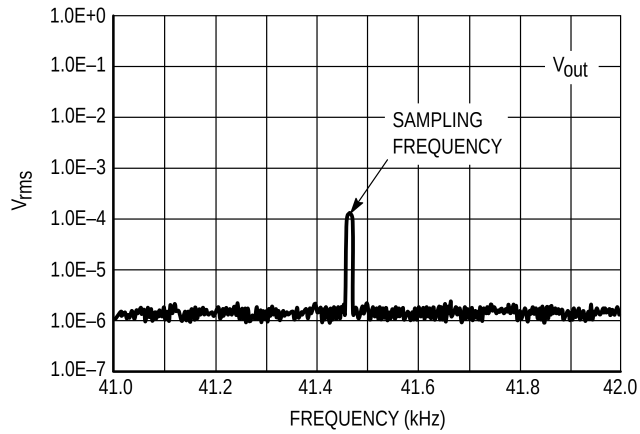
The accelerometer is a ratiometric electro–mechanical transducer. Therefore, the input signals to the device are the acceleration and the input power source.

The acceleration input is limited in frequency bandwidth by the geometry of the sensing, packaging, and mounting structures that define the resonant frequency and response. This response is in the range of 10 kHz, however, the practical range is less than 600 Hz for most mechanical systems. Therefore, aliasing an acceleration signal is unlikely.

The power input signal is ideally dc. However, depending on the application system architecture, the power supply line can be riddled with high frequency components. For example, dc to dc converters can operate with switching frequencies between 20 kHz and 200 kHz. This range encompasses the sampling rate of the accelerometer and point to the power source as the culprit in producing aliased signal.

DEMONSTRATION WITH THE MMAS40G

Under zero acceleration conditions a 100 mV_{rms} signal was injected onto the power supply line of 5.0 Vdc. The frequency of the injected signal was tuned in to produce an alias in the accelerometer's passband. Figures 3 and 4 show the difference in output when a high frequency signal is not and is present on the V_{CC} pin of the accelerometer.



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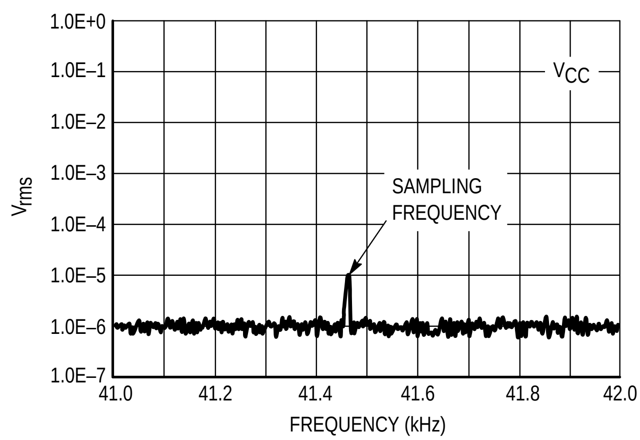

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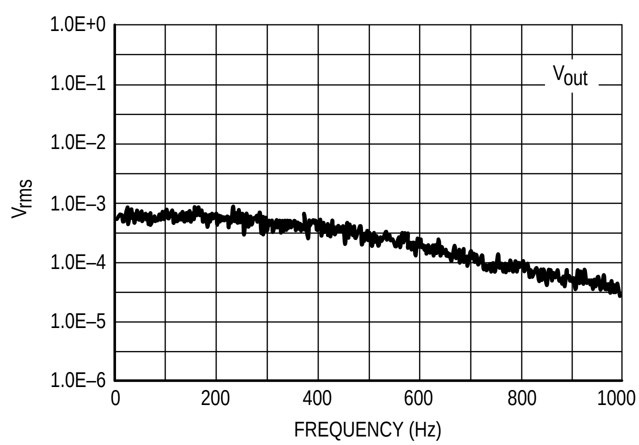
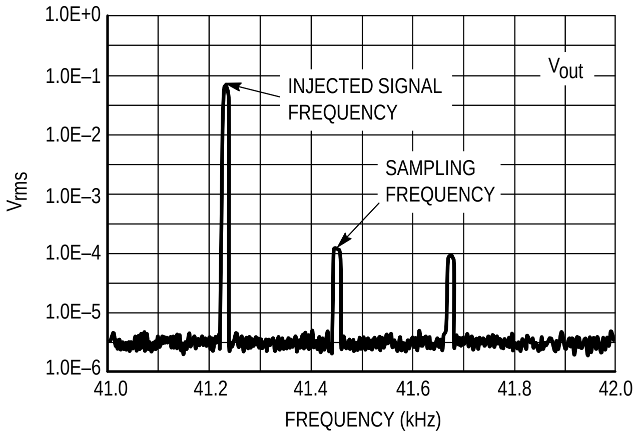


(c)

Figure 3. Normal Waveforms



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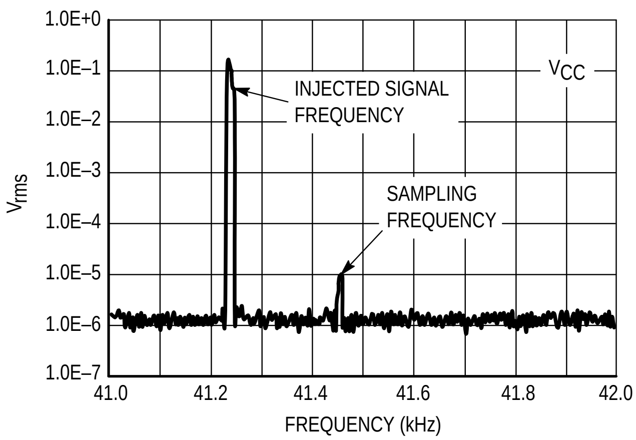

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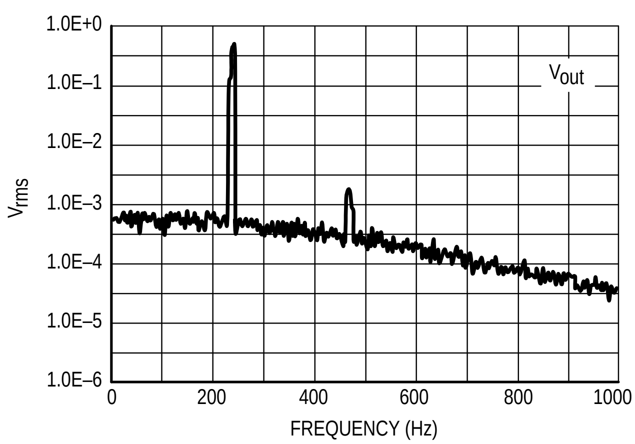

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Figure 4. Aliasing Comparison

Points to note:

- Under clean dc bias, V_{out} and V_{CC}, Figures 3a and 3b have a signal component at the sampling rate. This is due to switched capacitor currents coupling through finite power supply source impedences and PCP paracitics.
- The low frequency output spectrum, Figure 3c, displays the internal lowpass filter characteristics. (The filter and sampling characteristics are sometimes useful in system debugging.)
- When an ac component is superimposed onto V_{CC} near the sampling frequency, as shown in Figure 4b, the output will contain the original signal plus a mirrored signal about the sampling frequency, shown in Figure 4a. Signals on the V_{CC} line will appear at the output due to the ratiometric characteristic of the accelerometer and will be one half the amplitude.
- As a result of sampling, the output waveform of Figure 4c is produced where the injected high frequency signal has now produced a signal in the passband.
- Harmonics of the aliased signal in the pass band are also shown in Figure 4c.
- Aliased signals in the passband will be amplified versions of the injected signals. This is due to the signal conditioning circuitry in the accelerometer that includes gain.

ALIASING AVOIDANCE KEYS

- Use a linear regulated power source when feasible. Linear regulators have excellent power supply rejection offering a stable dc source.
- If using a switching power supply, ensure that the switching frequency is not close to the accelerometer sampling frequency or its harmonics. Noting that the accelerometer will gain the aliasing signal, it is desirable to keep frequencies at least 4 kHz away from the sampling frequency and its harmonics. 4 kHz is one decade from the –3 dB frequency, therefore any signals will be sufficiently attenuated by the internal 4–pole lowpass filter.
- Proper bias decoupling will aid in noise reduction from other sources. With dense surface mount PCB assemblies, it is often difficult to place and route decoupling components. However, the accelerometer is not like a typical logic device. A little extra effort on decoupling goes a long way.
- Good PCB layout practices should always be followed. Proper system grounding is essential. Parasitic capacitance and inductance could prove to be troublesome, particularly during EMC testing. Signal harmonics and sub–harmonics play a significant role in introducing aliased signals. Clean layouts minimize the effects of parasitics and thus signal harmonics and sub–harmonics.

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