AN1544

Design of Continuously Variable Slope Delta Modulation Communication Systems

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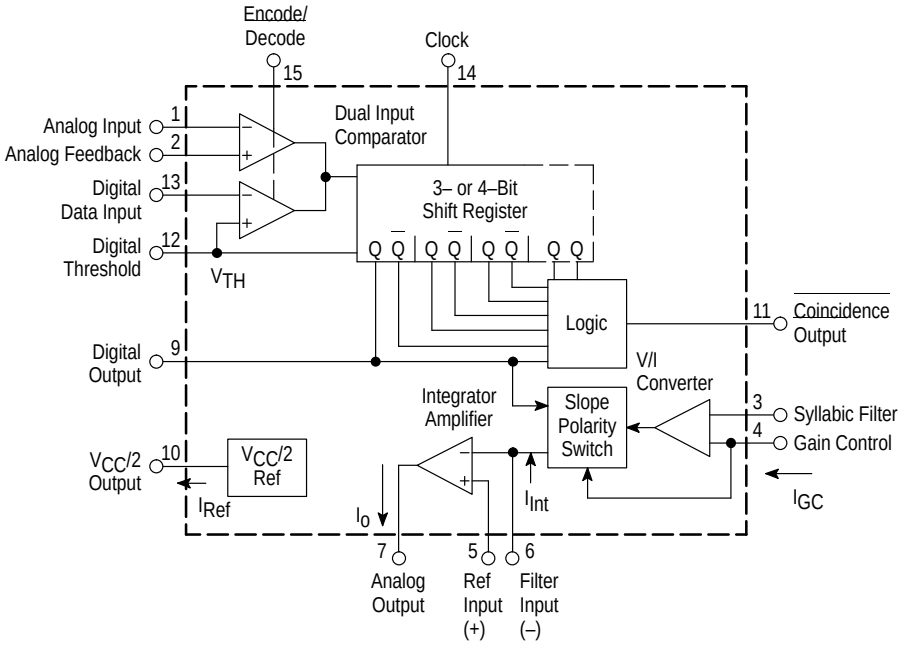
INTRODUCTION

Delta modulation is a simple and robust method of A/D conversion in systems requiring serial digital communications of analog signals. The delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. Delta modulation (DM) is limited by the analog input frequency and amplitude processed with any given circuit configuration; *i.e.,* the higher the clock frequency, the better the modulation quality. The clock frequency used should be minimally 9600 Hz and ideally 64 kHz for voice applications designed for a typical analog input frequency of 1000 Hz. DM has the advantage that signal to noise ratios do not vary with distance in digital transmission and multiplexing, and the switching and repeating hardware is more economical and easier to design than with purely analog systems. The signal to noise ratio (SNR) is defined as the ratio of signal power to the noise power.

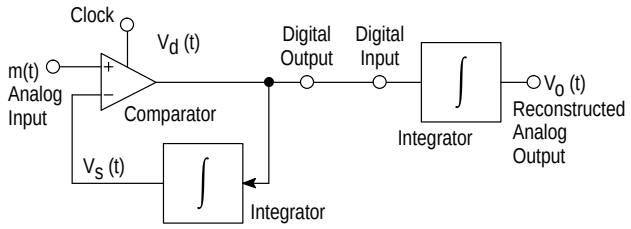
This paper is intended to give practical guidance in designing an optimum deltamod configuration for the most common voice applications using a Continuously Variable Slope Delta Modulator/Demodulator, MC34115 or MC3418, and provide some useful SNR performance information. Delta modulation theory is briefly reviewed[1], and a MathCAD® Version 3.1 model (see Appendix A) is presented[2] that provides the designer with suggested parameter values and simulates the deltamod signal, given the clock frequency, input voltage function (including amplitude and frequency), and supply voltage. It is possible to methodically design a system with limited knowledge of communications theory using simple guidelines presented in this model, which is presented as a supplement to the design guidance provided by the Continuously Variable Slope Delta Modulator/Demodulator (CVSD) data sheet[3]. The configuration derived for Figure 12 (Figure 14 of the data sheet) is demonstrated, and the results produced by the model are compared to and are consistent with those obtained experimentally.

Figure 1. CVSD Block Diagram



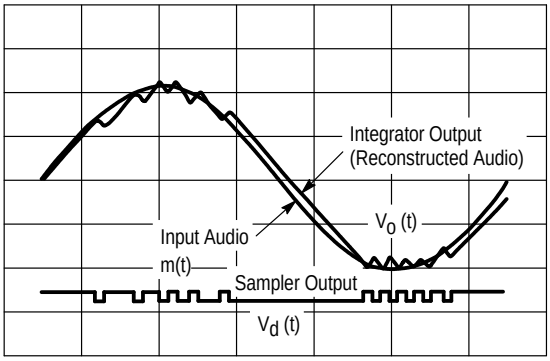
DELTA MODULATION

Figure 2. Simple Delta Modulation



The digital output, V_d, is either high or low at any given time. If V_d is high, the integrator output, V_S, will be ramping up. Conversely, if V_d is low, the integrator will be ramping down. Referring to Figure 2, the analog input, m, is compared to the integrator output voltage, V_S. If, for example (see Figure 3), the integrator is ramping up and its output is less than the input, the integrator output, V_S, will continue ramping up. When m(t) is greater than V_S, V_d is high and the integrator ramps up. When V_S is ramped to a value greater than m, V_d goes low, and V_S begins to ramp down until V_S is once again less than m and the process repeats itself. The resulting digital output, V_d, is therefore the differential of the input and is the signal to be transmitted to the destination where it is integrated to provide the reconstructed analog signal. The step size, S, is defined as absolute value of the change in integrator output voltage for one clock period. If the clocked serial bit stream is transmitted to a similar integrator at the remote destination, the integrator output, V_O, is a copy of the control loop integrator voltage, V_S.

Figure 3. Example of m(t) (Analog Input), V_d (Transmitted Sampler Output) and V_o (Modulated Integrator Output)[3]



CVSD modulation, by definition, changes the output slope to match the input slope (see Figure 4). This feature allows for continually minimized quantization noise. Note the step size of the output changes with the amplitude of the input. Figures 5 and 6 show block diagrams of the CVSD encoder and decoder.

Figure 4. Example of Continuously Variable Slope Delta Modulator/Demodulator (CVSD) Output

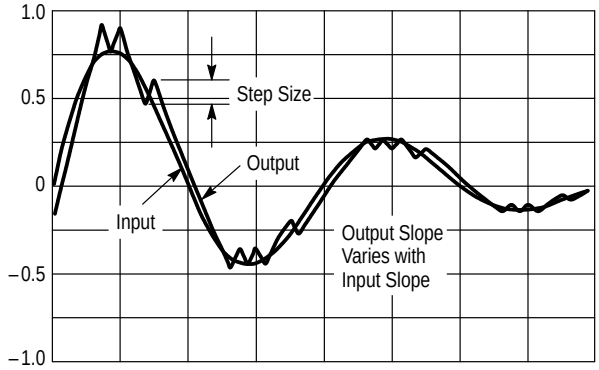


Figure 5. Block Diagram of the CVSD Encoder

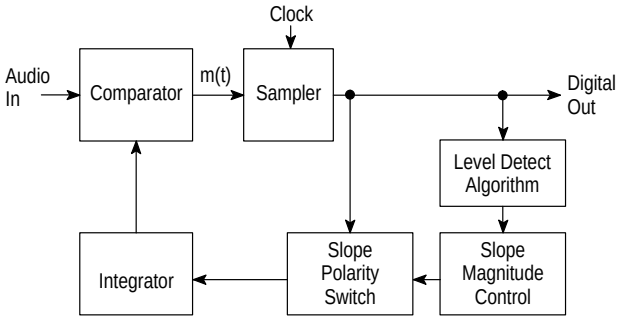
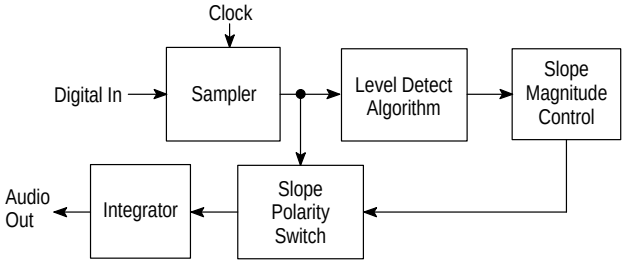
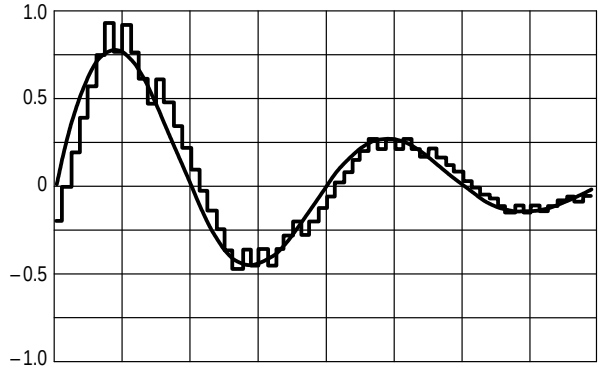


Figure 6. Block Diagram of the CVSD Decoder[3]



An ideal delta modulation system would sample the comparator output to produce a delta function pulse every clock period instead of a step function, as is the case for the CVSD discussed here. This delta function would be integrated in the feedback loop to produce a step function output, rather than a ramp function (see Figure 7).

Figure 7. Example of True Delta Modulation



COMPANDING ALGORITHM

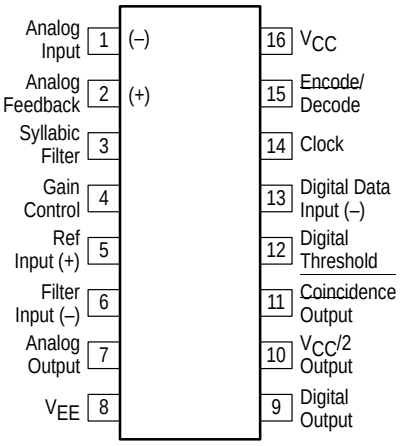
The analog input must be band and amplitude limited. The analog input frequency is limited by the nyquist rate, and the range of amplitude capabilities is limited by the gain of the integrator; *i.e.,* one specific gain will achieve an optimum noise level for a given signal level. The analog input frequency is limited on the upper end by the clock frequency. However, the amplitude limits are bounded on both upper and lower ends.

The dynamic range over which the noise level is constant for a given clock frequency and input bandwidth for a delta modulator may be optimized by adjusting the gain of the integrator with CVSD circuitry. A 3– or 4–bit shift register monitors the output and indicates when the register fills with all 1's or all 0's. This condition is called *coincidence.* The gain, or slope, of the integrator is too small when coincidence is indicated. The coincidence charges a low pass filter, called the *syllabic filter,* which controls the gain of the integrator. Therefore, the higher the frequency of coincidence, the greater the ramp amplitude. This filter provides the integrator with its continuously variable slope characteristics, and produces a reconstructed output that tracks the slope of the input. This is the basis for *companding* (compressing/expanding), where the dynamic range is increased past that which would be possible with a fixed integrator gain.

DEFINITIONS AND FUNCTION OF PINS

This provides a brief reference. The designer should refer to the data sheet for complete descriptions.

Figure 8. Pin Connections for the MC34115 and MC3418[3]



Pin 1 – Analog Input

This is the analog comparator inverting input where the voice signal is applied. A bias resistor between Pins 1 and 10 is required to level shift the voice signal to the internal reference voltage.

Pin 2 – Analog Feedback

This is the noninverting input to the analog signal comparator within the IC. This pin is connected to Pin 7, the analog output of the encoder circuit.

Pin 3 – Syllabic Filter

The syllabic filter voltage is returned to the IC to control the integrator step size. Time constant values typically range between 4.0 and 50 ms in voice codecs. A time constant between 4.0 and 10 ms is recommended for best results.

Pin 4 – Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The resistor, R_X, is varied to adjust the loop gain of the codec, but should generally be no larger than 5.0 kΩ to maintain stability.

Pin 5 – Reference Input

This is the noninverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and be tied to Pin 10.

Pin 6 – Filter Input

This inverting operational amplifier input is used to connect the integrator external components.

Pin 7 – Analog Output

This is the integrator operational amplifier output. It is capable of driving a 600 Ω load referenced to $V_{CC}/2$ to 6.0 dBm.

Pin 8 – V_{EE}

The most negative voltage supply.

Pin 9 – Digital Output

The digital output provides the results of the delta modulator's conversion.

Pin 10 – $V_{CC}/2$ Output

An internal low impedance mid–supply reference is provided for use in single supply applications. This pin must have the 1.0 kΩ resistor and 0.1 μF capacitor shown in Figure 12 to maintain stability.

Pin 11 – Coincidence Output

The duty cycle of this pin is proportional to the voltage across C_S.

Pin 12 – Digital Threshold

This input sets the switching threshold for Pins 13, 14 and 15.

Pin 13 – Digital Data Input

The digital data stream is applied to Pin 13 in a decode application.

Pin 14 – Clock Input

The clock input determines the data rate of the codec circuit.

Pin 15 – Encode/Decode

This input controls the connection of the analog input comparator to the internal shift register.

Pin 16 – V_{CC}

The power supply range is from 4.75 to 16.5 V between Pins V_{CC} and V_{EE}.

DELTA MODULATION DESIGN

A MathCAD® Version 3.1 program was developed to provide guidance to the user in designing applications for the Motorola Continuously Variable Slope Delta Modulator/ Demodulator (CVSD) MC34115 and MC3418. This program calculates the delta modulation function, given the input amplitude and frequency and sampling frequency. The most important design considerations involved in the configuration of the CVSD into a specific codec application are as follows:

1. Selection of clock rate and analog input function
2. Required number of shift register bits
3. Design of integration filter transfer function
4. Design of syllabic filter transfer function
5. Selection of minimum idle channel step size
6. Design of low pass filter at the receiver

Selection of Clock Rate and Analog Input Function

For voice applications, it is recommended the CVSD be designed for an analog input frequency of 1000 Hz and 1.0 V amplitude (2.0 V_{pp}). The higher the clock frequency that can be afforded, the better the SNR performance (up to about 64 kHz). The performance of the signal transmission will be maximized if the clock inputs of the transmitter and receiver are phase–locked to avoid the introduction of error bits. In practice, the useful dynamic range extends about 6.0 dB above the design level. The companding ratio should not exceed 30% in any system.

Required Number of Shift Register Bits

The MC34115 is designed for low bit rate systems and the MC3418 is designed for high performance, high bit rate systems. The MC34115 has a 3–bit algorithm and the MC3418 has a 4–bit algorithm. For clock rates of 16 kHz and below, the 3–bit algorithm is well suited. For clock rates of 32 kHz and above, the 4–bit algorithm is preferred.

Design of Integration Filter Transfer Function

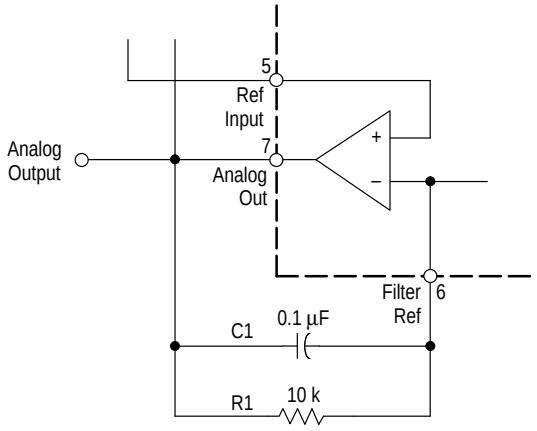
The single or double pole configuration chosen for the integrator is important in optimizing device performance. This amplifier reconstructs the transmitted digital serial signal, which as a transmitter provides the comparator feedback, or as a receiver, provides the reconstructed audio output.

The single–pole integration filter has the transfer function description:

$$\frac{V_o}{I_i} = \frac{1}{C1\left(S + \frac{1}{R1C1}\right)} \quad \textbf{(1)}$$

$$\text{and gain of } G1(s) = \frac{R_X}{C1\left(S + \frac{1}{R1C1}\right)} \quad \textbf{(2)}$$

Figure 9. Single–Pole Integration Filter (MC34115 or MC3418)



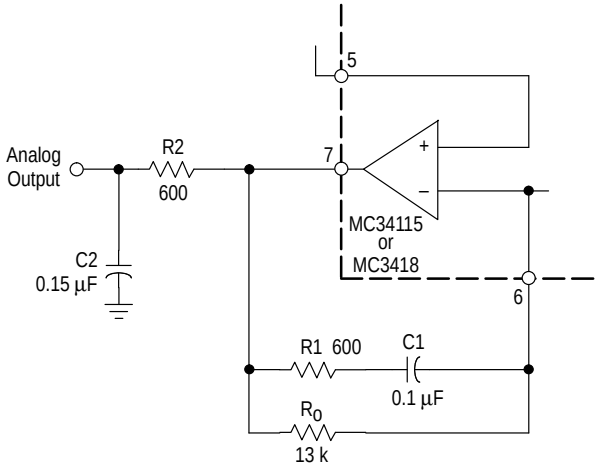
The double–pole integration filter has the transfer function description:

$$\frac{V_o}{I_i} = \frac{R0R1\left(S + \frac{1}{R1C1}\right)}{R2C2(R0 + R1)\left(S + \frac{1}{(R0+R1)C1}\right)S + \left(\frac{1}{R2C2}\right)} \quad \textbf{(3)}$$

and gain of:

$$G2(s) = \frac{R_XR0R1\left(S + \frac{1}{R1C1}\right)}{R2C2(R0 + R1)\left(S + \frac{1}{(R0+R1)C1}\right)S + \left(\frac{1}{R2C2}\right)}$$

Figure 10. Double–Pole Integration Filter (MC34115 or MC3418)



The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Design of Syllabic Filter Transfer Function

The syllabic filter is a simple single–pole (see Figure 11) or two–pole network that produces a time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the SNR performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

The gain of the circuit is set by the resistor R_X, which must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle on Pin 11 of the codec circuit. The system gain is dependent on:

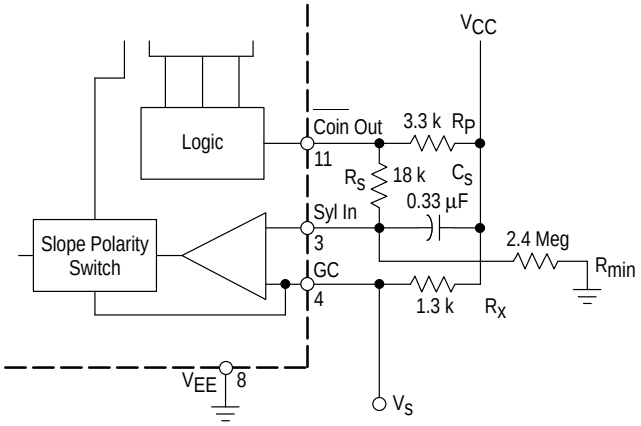
1. The maximum level and frequency of the input signal
2. The transfer function of the integration filter

The syllabic filter in Figure 11 is a simple single–pole syllabic filter network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. Typically, the syllable is between 5.0 and 10 ms, depending on the sound quality of the individual application. Note that V_S in Figure 11 is the syllabic filter voltage and not the power supply voltage, V_{SS}.

Minimum Idle Channel Step Size

The final design parameter to be selected is the idle channel step size, or the step size of the output with no analog input. The digital output becomes a one–zero alternating pattern and the analog output becomes a small triangle wave. The idle channel step size, DV_O, must be twice the specified total loop offset if a one–zero idle pattern is desired.

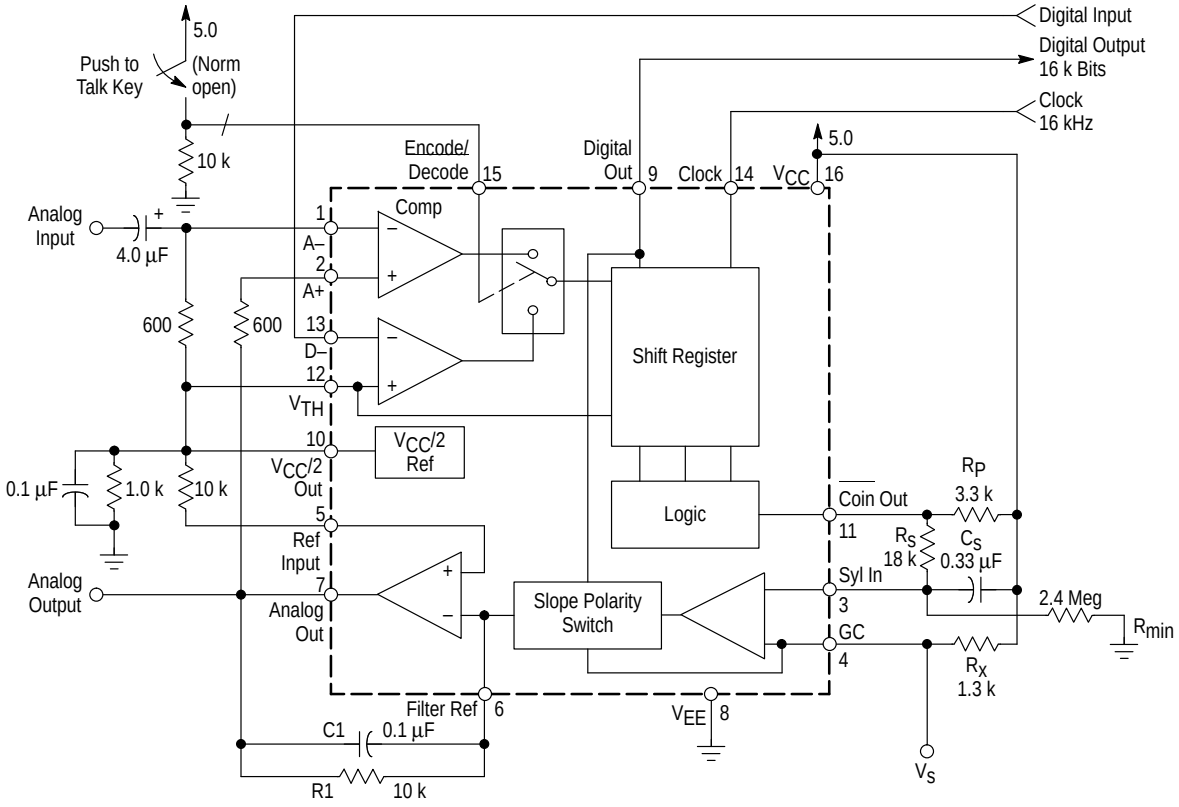
Figure 11. Syllabic Filter Circuit Diagram (MC34115 or MC3418)



The value of R_{min} must be selected to set the idle channel step size. The slope control algorithm is inactive with no input signal. A long series of ones and zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_P, R_S and R_{min} sets the minimum allowed voltage across the syllabic filter capacitor. As the input amplitude increases from zero, the step size of the output, DV, will in turn increase and its slope will continuously vary to match the slope of the input at the zero crossing. The designer should ensure these parameters are within minimum allowed tolerances to ensure proper circuit configurations are achieved.

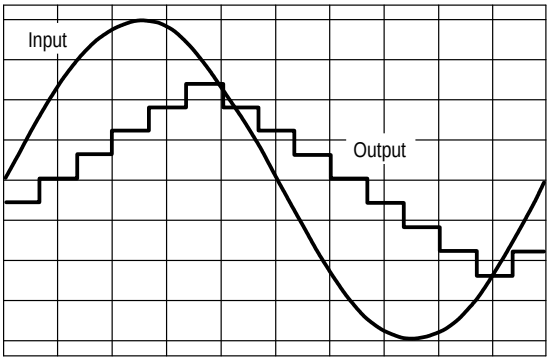
$$I_i = \frac{V_O}{R1} + C\frac{dV_O}{dt} \approx C_S\frac{\Delta V_O}{\Delta T} \quad \textbf{(4)}$$

Figure 12. Simplex Voice Codec (Using MC34115 or MC3418, Single–Pole Companding and Single Integration)



Slope–overload occurs when the modulating signal, m(t), changes faster than the step size for each clock period, S, allows (see Figure 13). The onset of overload is thus dependent on the frequency and slope of m(t) rather than the amplitude V_o2. The syllabic filter minimizes this effect by increasing the step size as required by the analog input frequency and slope.

Figure 13. Example of Slope Overload in Delta Modulation



The minimum input amplitude is step size limited such that $S < 2V_o$ and the signal is:

$$m(t) = V_o \times \sin(2\pi \times f_o t) \quad \textbf{(5)}$$

and

$$\frac{d}{dt} m(t)\Big|_{t=0} < \frac{S}{T_S} \quad \textbf{(6)}$$

where f_o is the input frequency and T_S is the sampling time. Then:

$$\frac{d}{dt} V_o \times \sin(2\pi \times f_o t)\Big|_{t=0} = V_o \times 2\pi \times f_o \cos(2\pi \times f_o t)\Big|_{t=0} < \frac{S}{T_S}$$

$$\text{and since } \frac{1}{T_S} = f_S \quad \textbf{(7)}$$

$$\text{then } V_o \times 2\pi \times f_o < S f_S \quad \text{or} \quad V_o < \frac{S f_S}{2\pi \times f_o}$$

which is the maximum signal amplitude allowed to avoid both step size limiting and slope–overload. From Equation (7):

$$S < 2 \frac{S f_S}{2\pi \times f_o}$$

$$\text{thus } f_S > \pi \times f_o \quad \textbf{(8)}$$

In practice, the step size should be adjusted for the highest frequency that will be required for transmission. Therefore, if the input signal frequency is f_o = 1.0 kHz and the sampling frequency is f_S = 50 kHz, the optimum step size is given by (referring to Equation (7)):

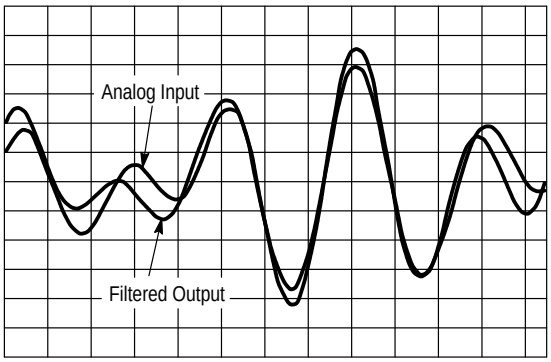
$$S \cong T_S \times f_o \times 2\pi \times V_o = \frac{2\pi \times V_o}{f_S / f_o}$$

$$= \frac{2\pi \times 1}{(50 \times 10^3 / 1 \times 10^3)} = 126 \text{ mV} \quad \textbf{(9)}$$

Design of Low Pass Filter at the Receiver

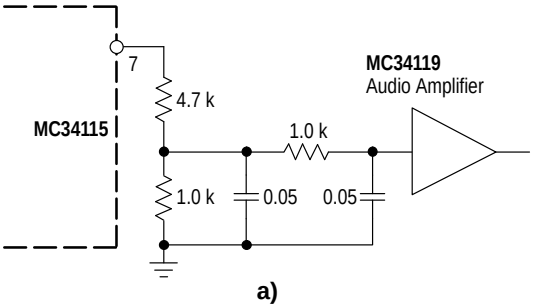
A low pass filter at the receiving circuit output will eliminate most of the quantizing noise. Generally, the lower the bit rate, the better the filter must be. Low pass filtering at the receiver output can eliminate most of the quantizing noise if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal.

Figure 14. Example of Delta Modulation Filtering

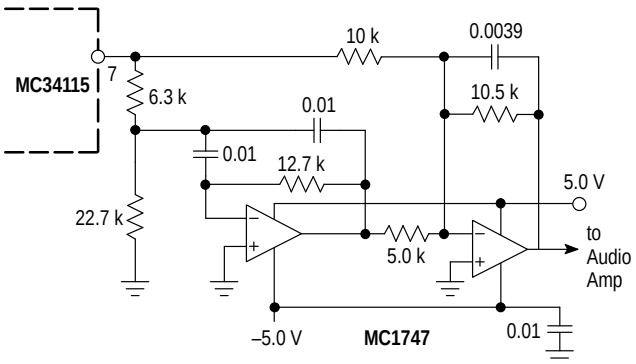


Two possible types of filters are shown. The RC filter shown in Figure 15a eliminates the quantizing noise quite well. To minimize the phase shift delay, the more elaborate elliptical filter shown in Figure 15b provides suitable results. The experimental results of filtering are illustrated in Figure 23.

Figure 15. Example of Simple RC Filtering and Elliptical Filtering for the MC34115 or MC3418



a)



b)

MODELING DELTA MODULATION

This section demonstrates numerically modeled delta modulation given the variables provided for the design configuration using MathCAD® Version 3.1. The designer must minimally provide the model with the clock frequency, analog input voltage function (including amplitude and frequency), and the supply voltage. The model provides the designer with suggested resistance and capacitance values (Figure 12), the reconstructed analog output signal (Figure 16), the gain and frequency response for single–pole (Figure 17) and double–pole (Figure 18) integration filters, the simulated continuously variable slope of input signal (dV/dt) (Figure 19), the transmitted digital signal (Figure 20), the quantizing noise (Figure 21), and a Fourier analysis of the output (Figure 22).

Figure 16. Example of 1000 Hz Analog Input and Integrator Output Signals Modeled to Show How Well the Signals May Be Reconstructed with Clock Rates a) f_S = 16 kHz, b) f_S = 32 kHz, and c) f_S = 64 kHz

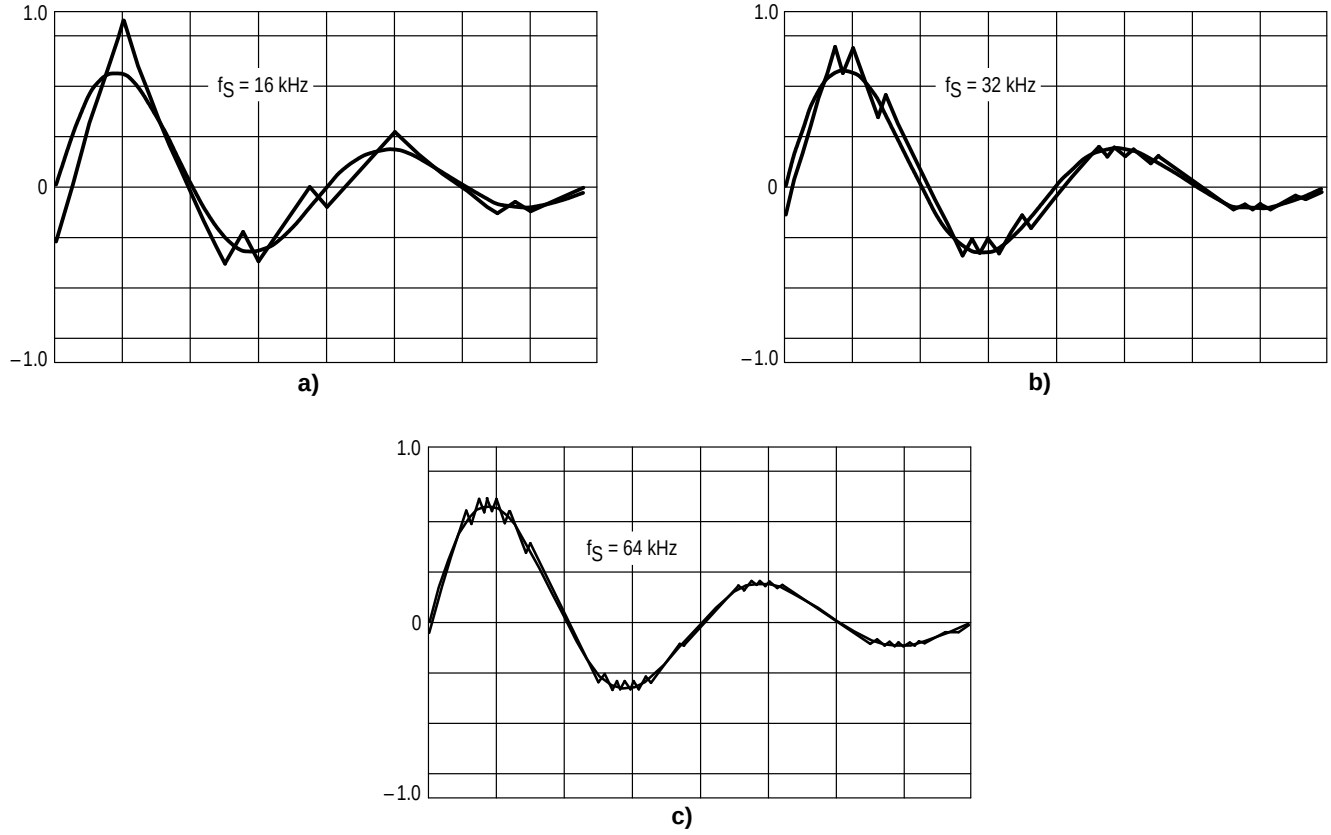


Figure 17. a) Simulated Single–Pole Bode Plot of System, and b) Simulated Phase Angle Single–Pole System

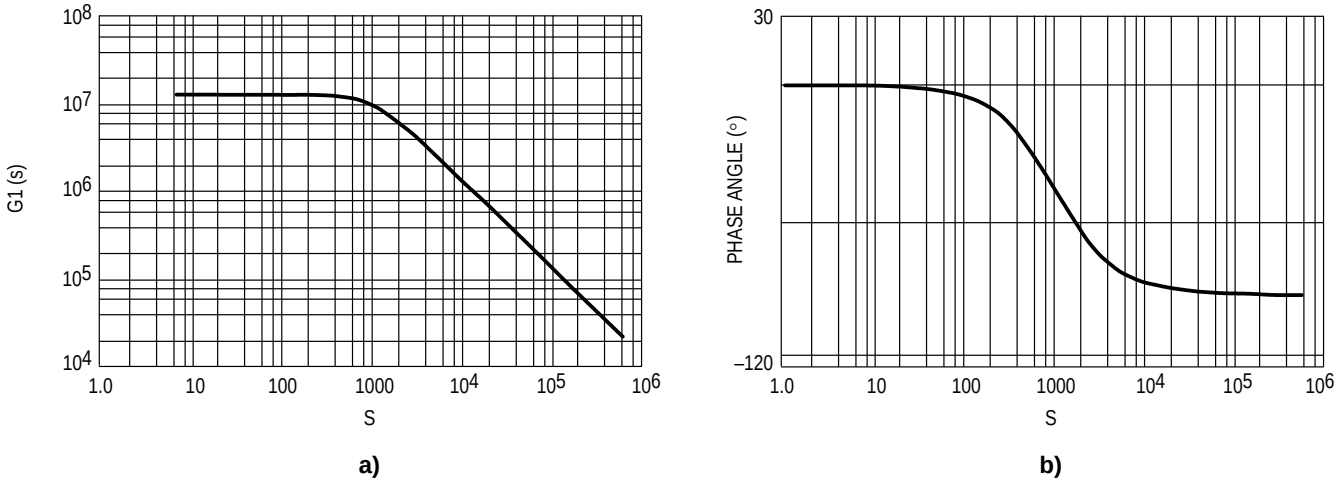


Figure 18. a) Simulated Double–Pole Bode Plot of System, and b) Simulated Phase Angle Double–Pole System

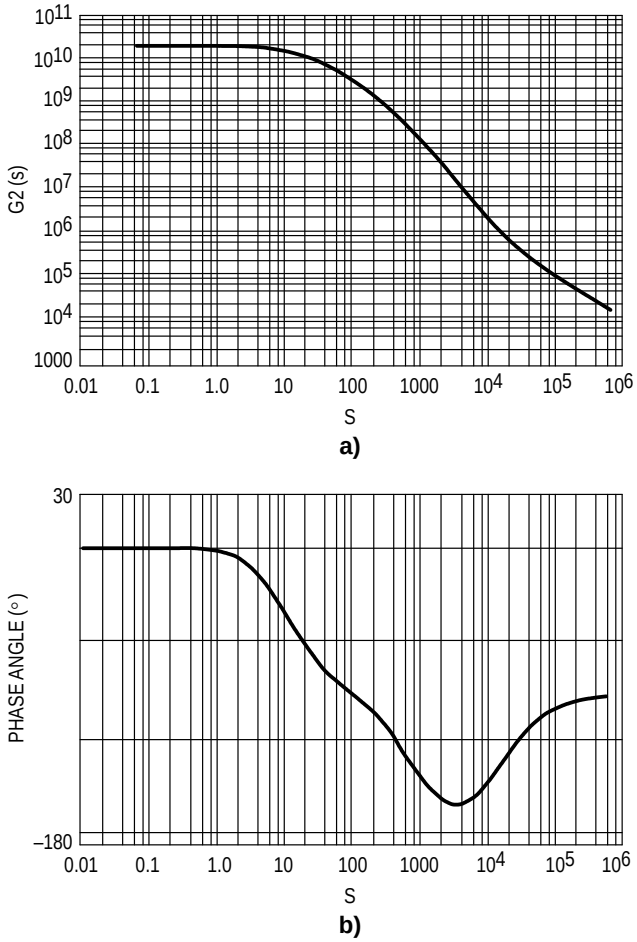
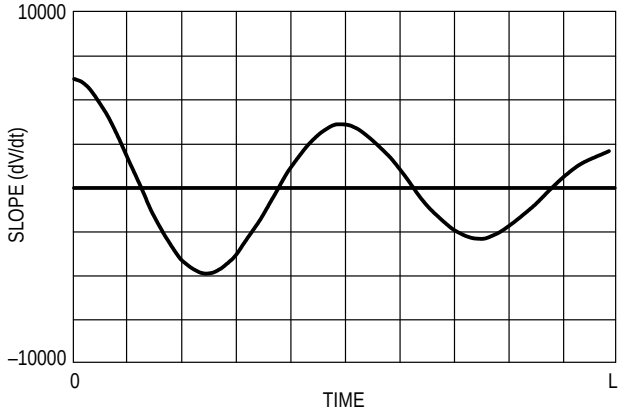
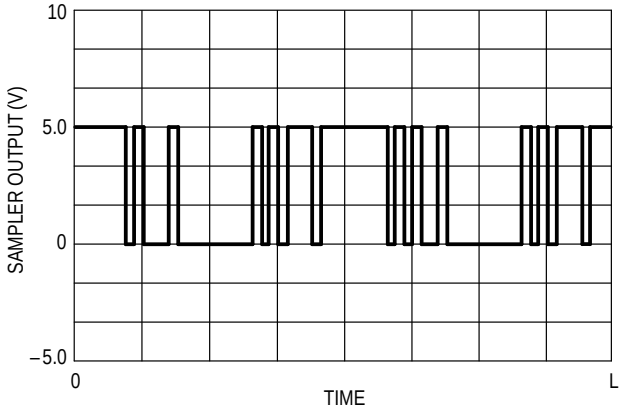


Figure 19. Simulated Continuously Variable Slope of Input Signal (dV/dt)



The quantizing noise is typically minimized if the slope of the reconstructed signal is designed to match the slope of the input function at the zero crossing. This can be accomplished by adjusting the gain resistor, R_X.

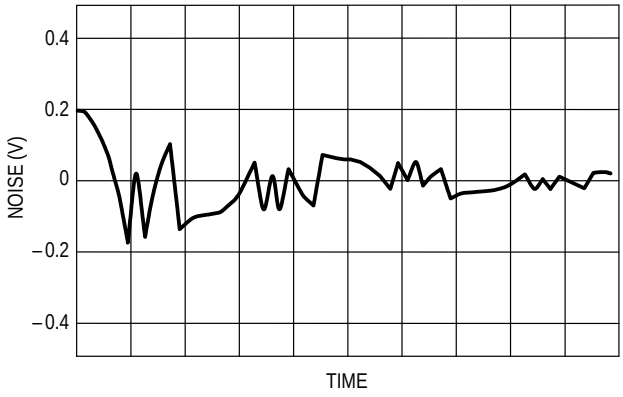
Figure 20. Simulated Transmitted Signal (Volts versus Time)



SIGNAL TO NOISE RATIO ANALYSIS

The quantizing noise is effectively the (root mean square) voltage of the output referenced to the input, and is modeled simply by subtracting the input from the output (see Figure 21).

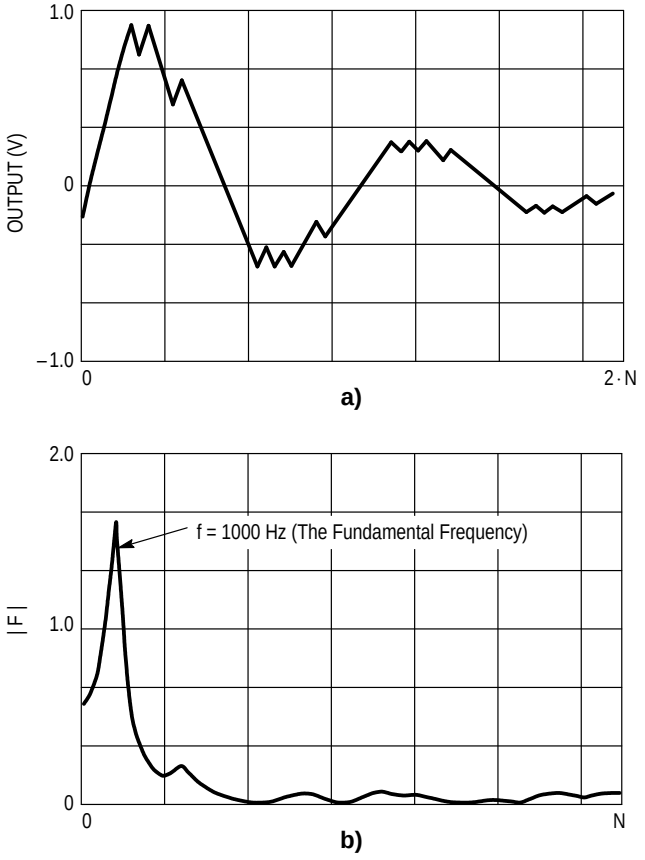
Figure 21. Simulated Quantizing Noise (Volts versus Time)



FREQUENCY ANALYSIS OF OUTPUT SIGNAL

The Fourier analysis of the modeled reconstructed output is demonstrated:

Figure 22. a) Simulated Modulated Output (Volts versus Time), and b) Simulated Spectral Analysis of Modulated Output



EXPERIMENTAL RESULTS

This section compares unfiltered noise and SNR results expected from the model to results obtained from Figure 12. The effective voltages of the input and output were compared to obtain experimental values shown in Figures 23 to 29. To find the quantizing SNR, the root mean square (RMS) voltage of the input was divided by the RMS voltage of the noise (Equation 11). The noise values were obtained by measuring the output voltage referenced to the input voltage, using an RC phase shifter to put the input and output voltages in phase with each other. The experimental and model results demonstrate a linear relationship between the SNR (dB) and the sampling frequency (clock rate). Additionally, a linear relationship between the noise (in volts) and the input voltage frequency (log(Hz)) was found both experimentally and in the model.

The root mean square value of a function is given by:

$$f(t)_{RMS} = \sqrt{\frac{1}{T} \times \int_0^T f^2(t)dt} \qquad \textbf{(10)}$$

and the experimental quantizing SNR was obtained by:

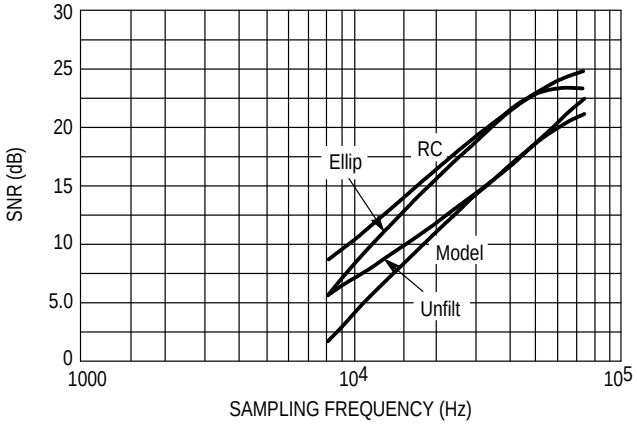
$$SNR_{exp} = 20 \times \log\left(\frac{S}{N}\right) \qquad \textbf{(11)}$$

were S is the effective signal voltage and N is the effective noise voltage.

Experimental and Model Results Compared

The following compares the unfiltered SNR produced by the model to filtered SNR obtained from Figure 12.

Figure 23. Comparison of SNRs for a Simple RC Filter, an Elliptical Filter, an Unfiltered Output and the Output Predicted by the Model for an Analog Input of 1000 Hz and 1.0 V Amplitude while Varying the Clock Frequency for the MC34115



Relationship Between Noise, Analog Input Frequency and Clock Frequency

The relationship between quantizing noise (Figure 24) and SNR (Figure 25) versus sampling frequency is illustrated. It is demonstrated that SNR improves with decreasing analog input frequency.

Figure 24. Noise (V) versus Sampling Frequency (Hz) for the MC34115

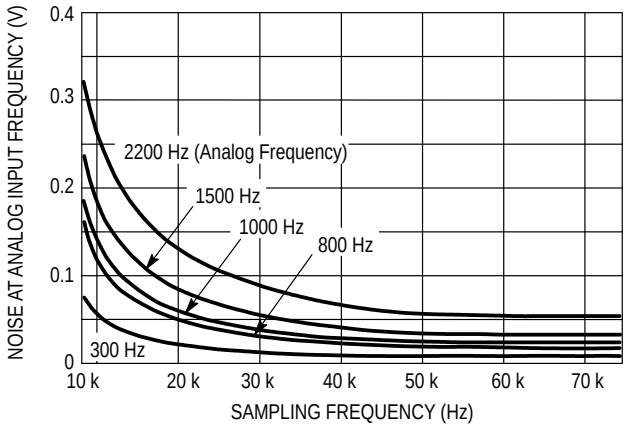


Figure 25. Signal to Noise Ratio (V) versus Sampling Frequency (Hz) for the MC34115

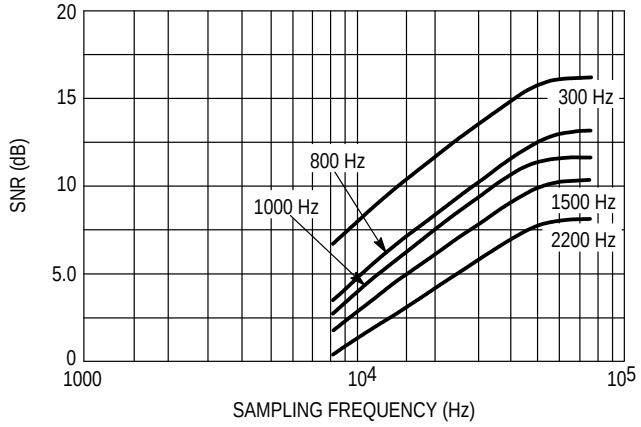


Figure 26. RMS Noise (V) versus Input Frequency (Hz) for the MC34115

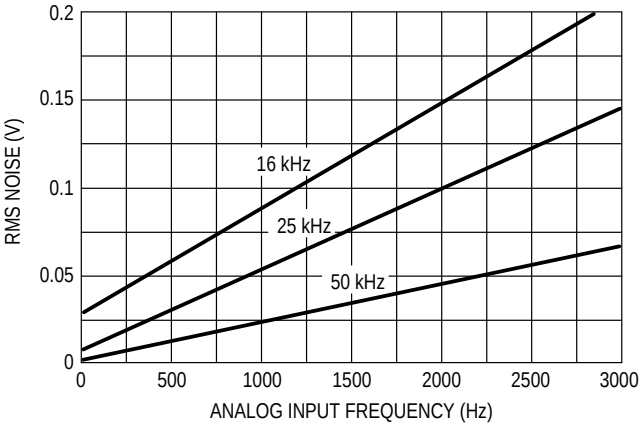
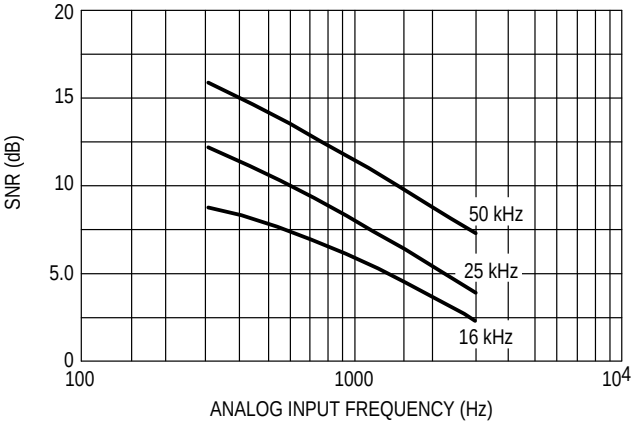


Figure 27. SNR (dB) versus Input Frequency (Hz) for the MC34115



Comparison of MC34115 and MC3418

The SNR performances of the MC34115 and MC3418 CVSD's are compared with a clock frequency of 50 kHz.

Figure 28. Comparison of RMS Noise for MC34115 and MC3418 at Clock Frequency of 50 kHz

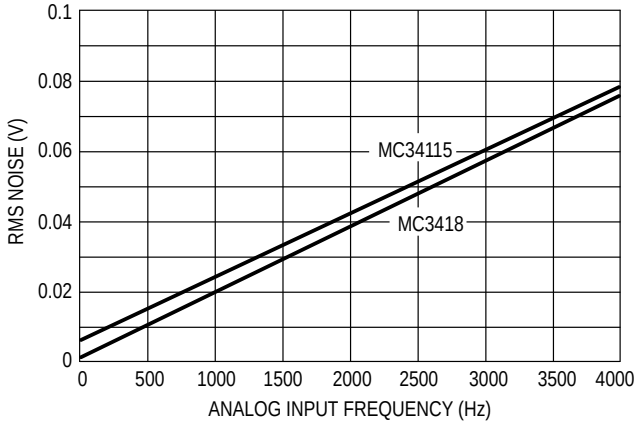
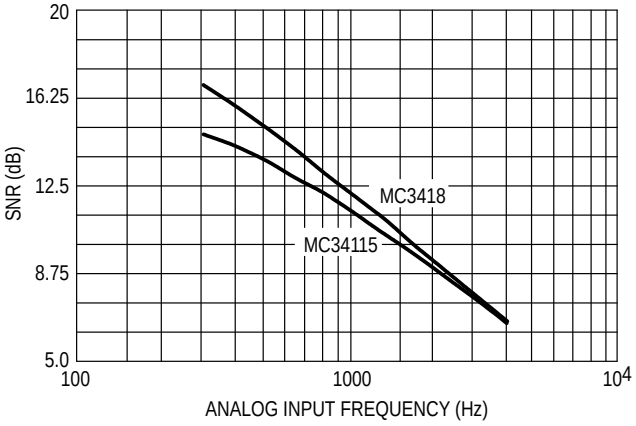


Figure 29. Comparison of SNR for MC34115 and MC3418 at Clock Frequency of 50 kHz for an Analog Input of 1.0 V Amplitude



CONCLUSIONS

The design of a simple single–pole CVSD communication system using the MC34115 and MC3418 is modeled and demonstrated with reasonable results. The model results are compared with actual data to verify the validity of the model. Adjust the gain resistor, R_X, to vary the slope of the output to optimize the sound quality. Typically, results are best when the slope of the output matches the slope of the analog input at the zero crossing. The MC3418 sounds better and performs better than the MC34115 with regards to quantizing noise.

REFERENCES

[1] *Modern Digital and Analog Communication Systems,* B. P. Lathi, Holt, Rinehart and Winston, Inc. (1989).

[2] *The Electronic Communications Problem Solver,* Research and Education Association (Piscataway, NJ, 1984).

[3] *Continuously Variable Slope Delta Modulator/ Demodulator,* MC34115, MC3418, Motorola Semiconductors Specifications and Applications, Motorola, Inc., 1988.

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APPENDIX A

Delta Modulation Design Program

This MathCAD program was developed to provide guidance to the user in designing applications for the Motorola Continuously Variable Slope Delta Modulator/ Demodulator (CVSD) MC34115 and MC3418. This MathCAD program calculates the delta modulation function, given the input amplitude and frequency and sampling frequency. The seven design considerations involved in the configuration of the CVSD into a specific codec application are as follows:

1. Selection of clock rate
2. Required number of shift register bits
3. Design of syllabic filter transfer function
4. Design of integration filter transfer function
5. Selection of minimum step size
6. Design of low pass filter at the receiver

Global Definitions

$$\text{deg} \equiv \frac{\pi}{180} \quad \Psi(\theta) \equiv \text{angle}(\text{Re}(\theta), \text{Im}(\theta)) - 360 \text{ deg}$$

Pin Definitions

Pin 1 – Analog Input

This is the analog comparator inverting input where the voice signal is applied. A bias resistor between Pins 1 and 10 is required to level shift the voice signal to the internal reference voltage.

Pin 2 – Analog Feedback

This is the noninverting input to the analog signal comparator within the IC. This pin is connected to Pin 7, the analog output of the encoder circuit.

Pin 3 – Syllabic Filter

The syllabic filter voltage is returned to the IC to control the integrator step size. Time constant values typically range between 3.0 and 50 ms in voice codecs (recommend between 4.0 and 10 ms).

Pin 4 – Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The R_X resistor is varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 – Reference Input

This is the noninverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and be tied to Pin 10.

Pin 6 – Filter Input

This inverting operational amplifier input is used to connect the integrator external components.

Pin 7 – Analog Output

This is the integrator operational amplifier output. It is capable of driving a 600 Ω load referenced to $V_{CC}/2$ to 6.0 dB.

Pin 8 – V_{EE}

The most negative voltage supply.

Pin 9 – Digital Output

The digital output provides the results of the delta modulator's conversion.

Pin 10 – $V_{CC}/2$ Output

An internal low impedance mid–supply reference is provided for use in single supply applications. This pin must have the 1.0 kΩ resistor and 0.1 μF capacitor shown in Figure 9 to maintain stability.

Pin 11 – Coincidence Output

The duty cycle of this pin is proportional to the voltage across C_S.

Pin 12 – Digital Threshold

This input sets the switching threshold for Pins 13, 14 and 15.

Pin 13 – Digital Data Input

The digital data stream is applied to Pin 13 in a decode application.

Pin 14 – Clock Input

The clock input determines the data rate of the codec circuit.

Pin 15 – Encode/Decode

This input controls the connection of the analog input comparator to the internal shift register.

Pin 16 – V_{CC}

The power supply range is from 4.75 to 16.5 V between Pins V_{CC} and V_{EE}.

Selection of Clock Rate and Analog Input Function

Designer's Input

supply voltage:	$V_{CC} := 5.0$ V	
sampling frequency:	$f_S := 32 \times 10^3$ Hz	(vary between 9600 Hz to 64 kHz)
input amplitude:	$V_o := 1.0$ V	(a 0 dBmo sine wave has a peak value of 1.095 V)
analog input frequency:	f := 1000 Hz	
input damping factor:	$\zeta := \ln(3)$	(set to zero for no damping)
input waveform:	$m(t) := V_o \times \sin(2 \times \pi \times f \times t) \times e^{-(t \times \zeta \times f)}$ V	

input period: $T := \frac{1}{f}$ $T = 1 \times 10^{-3}$ sec

sampling interval: $\Delta T_S := \frac{1}{f_S}$ $\Delta T_S = 3.125 \times 10^{-5}$ sec

length of sample: $L := 2 \times T$ sec

number of samples: $\alpha := \text{ceil}\left(\frac{\log(f_S \times L)}{\log(2)}\right)$ $\alpha = 6$ $2^\alpha = 64$ $k := 0 .. 2^\alpha - 1$

Required Number of Shift Register Bits

The MC34115 is designed for low bit rate systems and the MC3418 is designed for high performance, high bit rate systems. The MC34115 has a 3–bit algorithm and the MC3418 has a 4–bit algorithm. For clock rates of 16 kHz and below, the 3–bit algorithm is well suited. For clock rates of 32 kHz and above, the 4–bit algorithm is preferred.

Design of Integration Filter Transfer Function

The gain of the circuit is set by the resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle on Pin 11 of the codec circuit. The system gain is dependent on:

1. The maximum level and frequency of the input signal
2. The transfer function of the integration filter

For voice codecs the typical input signal is taken to be a sine wave at 1.0 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6.0 dB above the design level. The companding ratio should not exceed 30% in any system.

Single–Pole

To calculate the required step size current, the transfer function of the integration filter must be described.

Choose the pole frequency in Hz (recommend under 300 Hz to provide 1/s voice content curve).

$f_p := 160$ Hz

Design of Syllabic Filter Transfer Function

Choose a syllabic filter time constant much larger than the maximum input signal period. Choose a value with 3.0 ms being the minimum in voice band communications. The time constant for the averaging of the coincidence output signal is given by:

$\tau_S := \frac{1}{160}$

$\tau_S = 6.25 \times 10^{-3}$ sec syllabic filter time constant (recommended somewhere between 5.0 and 10 ms)

To achieve this time constant, choose a capacitor with a reasonable value:

$C_S := .33 \times 10^{-6}$ F syllabic filter capacitance

The syllabic filter resistance is then: $R_S := \frac{\tau_S}{C_S}$ $R_S = 1.894 \times 10^4\ \Omega$

Using a standard resistor value: $R_S := 18 \times 10^3\ \Omega$

The single–pole break frequency in radians is given by: $\omega p := 2 \times \pi \times f_p$ $\omega p = 1.005 \times 10^3/\text{sec}$

Design of Integration Filter Transfer Function

Choose a reasonable capacitance value: $C1 := 0.1 \times 10^{-6}\ F$

The resistance value, R1, is given by: $R1 := \frac{1}{\omega p \times C1}$ $R1 = 9.947 \times 10^3\ \Omega$

Using a standard resistor value for R1: $R1 := 10 \times 10^3\ \Omega$

The CVSD step should trace the change of a sine wave centered around the zero crossing at 1/8 of a cycle, where the wave changes by approximately its peak value. Thus:

$dV_0 := V_0$ $dt := \frac{1}{8} \times T$ $dt = 1.25 \times 10^{-4}$ sec

The integrator filter input current is given by: $I_i := \frac{V_0}{2 \times R1} + \left(C1 \times \frac{dV_0}{dt}\right)$ $I_i = 8.5 \times 10^{-4}$ A

Note: The maximum voltage across R1 when maximum slew is required is V_0/2.0 V.

The voltage range of the syllabic filter is the power supply voltage, thus:

$R_X := .25 \times V_{CC} \times \frac{1}{I_i}$ $R_X = 1.471 \times 10^3\ \Omega$

Using a standard resistor value for R_X (<5.0 kΩ): $R_X := 1.3 \times 10^3\ \Omega$

Minimum Step Size

The final design parameter to be selected is the idle channel step size. With no input signal, the digital output becomes a one–zero alternating pattern and the analog output becomes a small triangle wave. The idle channel step size, ΔV_0, must be twice the specified total loop offset if a one–zero idle pattern is desired.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones and zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} sets the minimum allowed voltage across the syllabic filter capacitor. As the input amplitude increases from zero, the step size of the output, ΔV, will in turn increase and its slope will continuously vary to match the slope of the input at the zero crossing. The designer should ensure these parameters are within minimum allowed tolerances to ensure proper circuit configurations are achieved.

It can be derived that the minimum step size, ΔV, required to avoid slope overload for the full amplitude of the input is:

$\Delta V := V_0 \times 2 \times \pi \times \left(\frac{f}{f_S}\right)$ $\Delta V = 0.196$ Minimum step size required

Define the minimum idle channel step size: $\Delta V_0 := 20 \times 10^{-3}\ V$

Set ΔV_0 = 0.02 V to match design parameters of Figure 14 of the MC34115 data sheet.

For values of V_0 near ΔV_0/2: $I_{i1} := C1 \times \frac{\Delta V_0}{\Delta T_S}$ $I_{i1} = 6.4 \times 10^{-5}$ A

The voltage on C_S which produces current I_{i1} is determined by R_X:

$V_{s(min)} := I_{i1} \times R_X$ $V_{s(min)} = 8.32 \times 10^{-2}$ V

The value suggested for R_{min} is: $R_{min} := R_S \times \left(\frac{V_{CC}}{V_{s(min)}} - 1\right)$ $R_{min} = 1.064 \times 10^6\ \Omega$

Define the transfer function: $G1(s) := \frac{R_X}{C1 \times \left(S + \frac{1}{R1 \times C1}\right)}$

Range of calculations (rad/sec): $Min := 10^0$ $Max := 10^5$ $n := 50$ $i := 0 .. n$

Log ratio of maximum and minimum frequencies: $r := \ln\left(\frac{Max}{Min}\right)$ $s_i := Min \times e^{\left(i \times \frac{r}{n}\right)} \times 2 \times \pi$

$\theta_i := \Psi(G1(s_i \times j))$ $Mag_i := |G1(s_i \times j)|$

Figure 30. Simulated Single–Pole Bode Plot of System

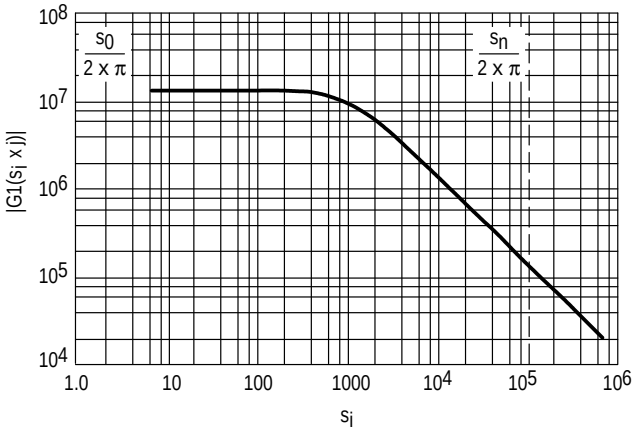
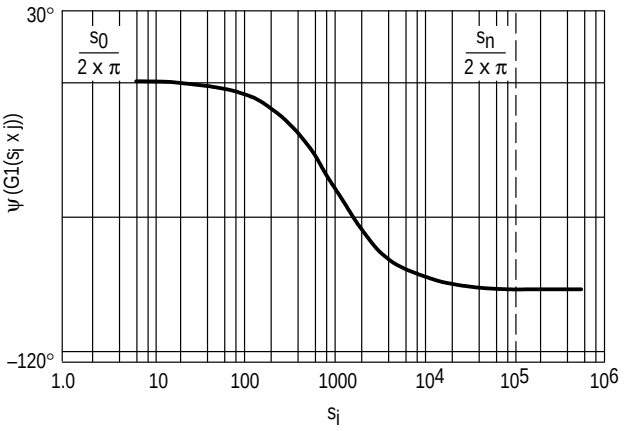


Figure 31. Simulated Phase Angle of Single–Pole System



Two–Pole

Choose the first pole frequency in Hz (recommend under 300 Hz to provide 1/s voice content curve).

$f_{p1} := 120$ Hz

Choose the second pole frequency in Hz (recommend above 1.0 kHz, or greater than 1.8 kHz for 1633 touchtone frequency).

$f_{p2} := 1800$ Hz

Choose the zero frequency (recommend slightly above the second pole frequency, such that the phase shift is kept less than 180 degrees).

$f_z := 2600$ Hz

Integrator Parameters

The loop gain resistor is: $R_X = 1.3 \times 10^3\ \Omega$

$C1 := 0.1 \times 10^{-6}$ F $C2 := 0.15 \times 10^{-6}$ F Choose reasonable values for C1 and C2

Using the values chosen for C1 and f_z: $R1 := \frac{1}{C1 \times f_z \times 2 \times \pi}$ $R1 = 612.134\ \Omega$

Adjust R1 to a standard resistor value: $R1 := 600\ \Omega$

Using the values chosen for C2 and f_{p2}: $R2 := \frac{1}{C2 \times f_{p2} \times 2 \times \pi}$ $R2 = 589.463\ \Omega$

Adjust R2 to a standard resistor value: $R2 := 600\ \Omega$

Using the values chosen for C1 and f_{p1}: $R0 := \frac{1}{C1 \times f_{p1} \times 2 \times \pi} - R1$ $R0 = 1.266 \times 10^4\ \Omega$

Adjust R0 to a standard resistor value: $R0 := 13 \times 10^3\ \Omega$

The adjusted frequency values are now:

$$f_{p1} := \frac{1}{(R0 + R1) \times C1 \times 2 \times \pi} \qquad f_{p1} = 117.026 \text{ Hz}$$

$$f_{p2} := \frac{1}{R2 \times C2 \times 2 \times \pi} \qquad f_{p2} = 1.768 \times 10^{3} \text{ Hz}$$

$$f_{z} := \frac{1}{R1 \times C1 \times 2 \times \pi} \qquad f_{z} = 2.653 \times 10^{3} \text{ Hz}$$

$$I_i := \frac{V_o}{R0} + \left(\frac{R2 \times C2}{R0} + \frac{R1 \times C1}{R0} + C1\right) \times \frac{\Delta V_o}{\Delta T_S} + \left(R2 \times C2 \times C1 + \frac{R1 \times C1 \times R2 \times C2}{R0}\right) \times \frac{\Delta V_o{}^2}{\Delta T_S{}^2}$$

$$I_i = 1.522 \times 10^{-4} \text{ A}$$

$$V_{s(min)} := I_i \times R_X \qquad V_{s(min)} = 0.198 \text{ V}$$

$$R_{min} := R_S \times \left(\frac{V_{CC}}{V_{s(min)}} - 1\right) \qquad R_{min} = 4.37 \times 10^{5} \ \Omega$$

Define the transfer function:

$$G2(s) := \frac{R_X \times \left[R0 \times R1 \times \left(S + \frac{1}{R1 \times C1}\right)\right]}{R2 \times C2 \times (R0 + R1) \times \left[S + \frac{1}{(R0 + R1) \times C1}\right] \times S + \left(\frac{1}{R2 \times C2}\right)}$$

Range of calculations (rad/sec): $Min := 10^{-2}$ $Max := 10^{5}$

Log ratio of maximum and minimum frequencies: $r := \ln\left(\frac{Max}{Min}\right)$ $s_i := Min \times e^{\left(i \times \frac{r}{n}\right)} \times 2 \times \pi$

Figure 32. Simulated Double–Pole Bode Plot of System

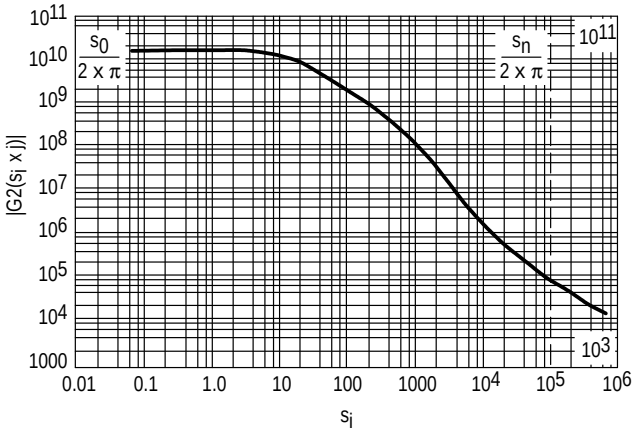
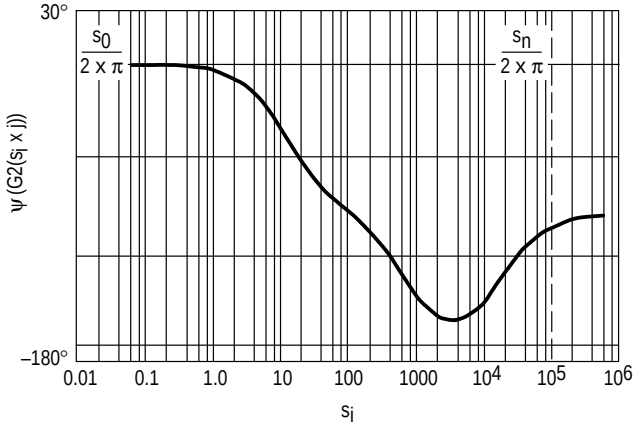


Figure 33. Simulated Phase Angle of Double–Pole System



Design of Low Pass Filter at the Receiver

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. Generally, the lower the bit rate, the better the filter must be. Low pass filtering at the receiver output can eliminate most of the quantizing noise if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal.

Modeling Delta Modulation

This section numerically models delta modulation given the variable provided for the design configuration.

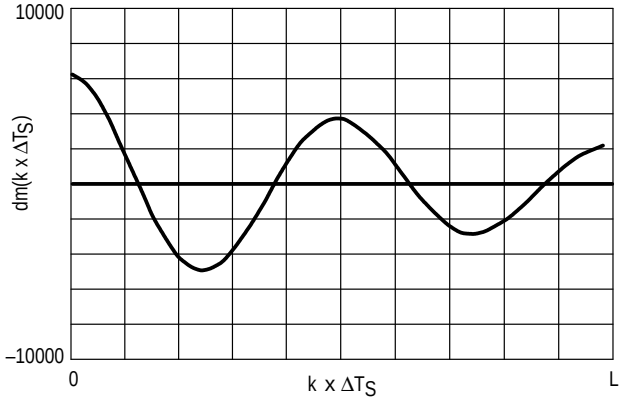
Sampling interval: $\Delta T_S = 3.125 \times 10^{-5}$ sec

Determines direction of integration: $sign(a) := (a > 0) - (a < 0)$

Starting matrix values: $\begin{pmatrix} S_0 \\ M_0 \end{pmatrix} := \begin{pmatrix} \Delta V \\ -\Delta V \end{pmatrix}$ $n := 0 .. 2^{\alpha} + 2$

dV/dt (slope of curve at t): $dm(t) := 2 \times \pi \times f \times \cos(2 \times \pi \times f \times t) \times e^{-\left(\frac{k \times \Delta T_S \times \zeta}{L}\right)}$

Figure 34. Simulated Continuously Variable Slope of Input Signal (dV/dt)



Point in phase where slope of modulated signal matches the input function. $\theta = 2\pi$ yields slope that matches the zero crossing.

$\theta := 2 \times \pi$

$slope(\theta) := 2 \times \pi \times f \times \cos(\theta \times f \times \Delta T_S)$ V/s

$slope(\theta) = 6.162 \times 10^3$ V/s dV/dt (slope of curve at V = 0)

Gives slope at each point: $\Delta m_k := dm(0) \times e^{-\left(\frac{k \times \Delta T_S \times \zeta}{L}\right)}$

$signal_n := m(n \times \Delta T_S)$ A := max (signal) B := min (signal)

Calculate the value of the modulated output signal:

$$\begin{pmatrix} S_{k+1} \\ M_{k+1} \end{pmatrix} := \begin{bmatrix} S0 \times \frac{\Delta m_k}{dm(0)} \times sign(signal_{k+2} - (M_k + S_k)) \times e^{-\left(\frac{k \times \Delta T_S \times \zeta}{L}\right)} \\ M_k + S_k \end{bmatrix}$$

Define the transmitted signal:

$fx_{k+1} := \frac{V_{CC}}{2} \times (sign(signal_{k+2} - (M_k + S_k)) + 1)$ $fx_0 := V_{CC}$ $fx_1 := fx_0$

Figure 35. Simulated Input and Modulated Output (Volts versus Time)

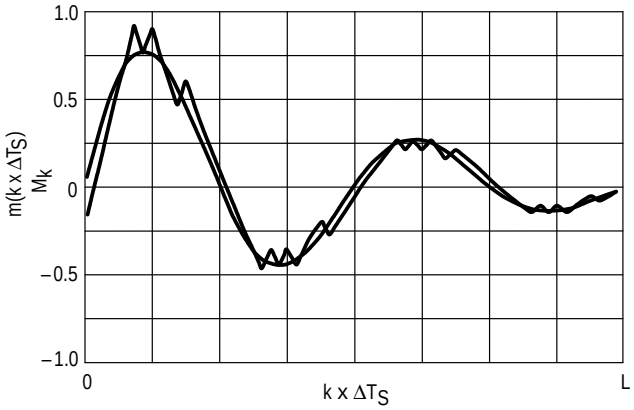
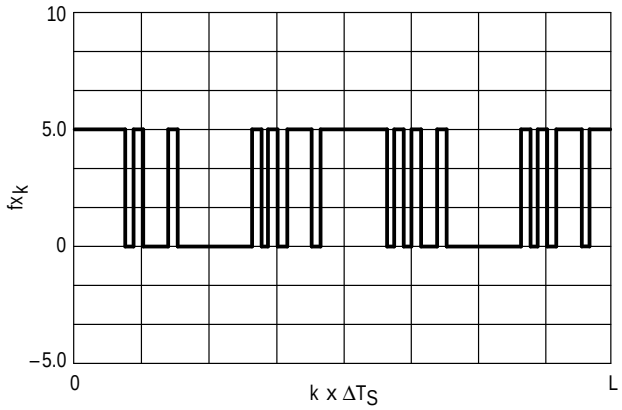


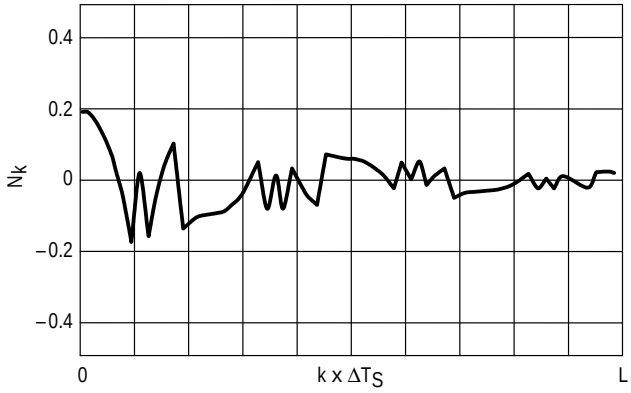
Figure 36. Simulated Transmitted Signal (Volts versus Time)



Noise Analysis

The quantizing noise is given by the voltage of the output referenced to the input: $N_k := m\ (k \times \Delta T_S) - M_k$

Figure 37. Simulated Quantizing Noise (Volts versus Time)



Find the effective (root mean square values of the input, output and noise voltages).

Input: $m\_rms := \sqrt{\frac{1}{T} \times \int_0^T m(t)^2\ dt}$ $m\_rms = 0.443$

Output: $M\_rms := \sqrt{\frac{1}{L} \times \sum_k (M_k)^2 \times \Delta T_S}$ $M\_rms = 0.34$

Noise: $N\_rms := \sqrt{\frac{1}{L} \times \sum_k (N_k)^2 \times \Delta T_S}$ $N\_rms = 0.071$

Single to Noise Ratio: $SNR := \frac{m\_rms}{N\_rms}$ $SNR = 6.24$

Frequency Analysis of Output Signal

Fourier analysis of output: $Y_k := M_k \quad c := fft\ (Y) \quad N := last\ (c) \quad j := 0\ ..\ N$

Figure 38. Simulated Modulated Output (Volts versus Time)

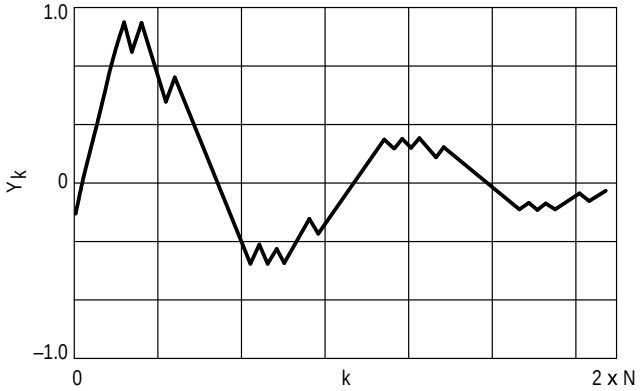
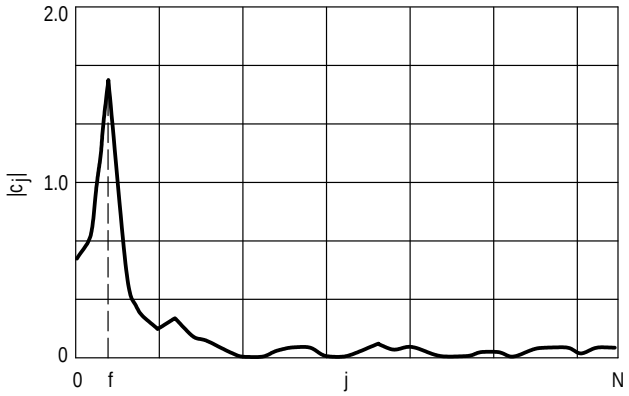


Figure 39. Simulated Spectral Analysis of Modulated Output



f = 1000 Hz THE FUNDAMENTAL FREQUENCY

NOTES

NOTES

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