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Applications of the MOC2A40 and MOC2A60 Series POWER OPTO™ ISOLATORS

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INTRODUCTION

Electronic controls of AC power loads based on microprocessor controllers, digital or linear sensor circuits are increasing in popularity. Consequently, there is an increasing need for a simple and robust interface between the low voltage control circuitry and the AC line and loads. This interface must galvanically isolate the AC power line and its superimposed transients from the noise sensitive, low-voltage dc control circuits. It also must be simple to use, regulatory approved, consume little PC board space and be able to switch the most common loads such as small motors, power relays, incandescent lights and resistive loads without generating excessive heat.

The MOC2A40 and MOC2A60 POWER OPTO Isolator families meet all the above requirements and offer an ideal system solution.

Figure 1. Internal Construction of the POWER OPTO Isolator

POWER OPTO is a trademark of Motorola, Inc.

PRODUCT DESCRIPTION

The Motorola AC POWER OPTO Isolator is a hybrid device containing three individual active semiconductor chips. Figure 1 shows the internal structure of this device. An infrared light emitting diode on the input side converts the input current signal of several milliamps into an infrared radiation of 940 nm. This is transferred through a transparent isolation barrier onto the photo sensitive area of an AC compatible detector which controls the gate of a power triac. This creates galvanic isolation between the dc input control circuit and the output AC line voltage potential. The light sensitive detector contains a AC zero voltage detector which allows turn on of the detector chip by the LED only when the AC line voltage is below the specified inhibit voltage of ±10 V. This feature guarantees turn on of the load close to the AC line zero cross point and prevents excessive inrush surge currents for most loads. High inrush currents are still experienced for loads such as motor startup and inductors which saturate at turn-on. For this reason, a guaranteed inrush surge current capability of 60 A is provided. This extremely high surge capability can be attributed to the rugged 120 x 120 mil power triac chip which is mounted on a large internal copper heat spreader. A patented interdigitated interface between the internal heat spreader and the devices integral heat tab provides optimized heat transfer and meets the regulatory requirements for safe (reinforced) isolation. This regulatory requirement mandates an external 8.0 mm creepage and clearance between the input and output leads and the isolated heat tab of the device. A 0.4 mm thick isolation barrier which must be able to withstand a surge voltage of 3750 V_{rms} is also mandated. The isolation barrier between dc input and the AC output leads is formed by the silicone optical dome. The isolation barrier for the integral heat sink is formed by the package epoxy which isolates the interlaced internal heat spreader from the external heat tab. A heavy duty 15 mil aluminum wire bond on the output side of the power triac ensures high surge capability.

Equivalent Electrical Circuit Diagram

Figure 2 shows in detail the internal circuitry of the MOC2A40 and MOC2A60 POWER OPTO Isolator families. Details of the of the triac driver ICs internal circuitry is shown and discussed to explain the theory of operation for these devices.

LED D1 emits light which is received by the detector light sensitive integrated circuit which is commonly named triac driver. PNP transistor, Q1, and light sensitive NPN transistor, Q2, form a light sensitive SCR with a gate resistor R1. Diode, D2, and FET, Q3, form the inhibiting network. The leakage current of D2 transfers the main terminal voltage to the FET gate and Zener diode, D3, clamps this voltage to about 15 V to prevent gate oxide breakdown when the main terminal voltage rises with the line voltage. A voltage on the main terminals above the gate threshold voltage of Q3 switches FET Q3 on, which shorts the photo sensitive gate and inhibits it to latch on. Q1', Q2′, Q3′, R1′, D2′, D3′ form the same circuit as described above.

The two circuits are connected inverse parallel and may be described as two inverse parallel light sensitive photo SCRs with zero cross voltage detectors. This circuit can be further simplified and described as an optically controlled small signal triac with an AC zero cross detection circuit. The triac driver controls the gate of the main triac. Resistor R2 limits the current through the triac driver.

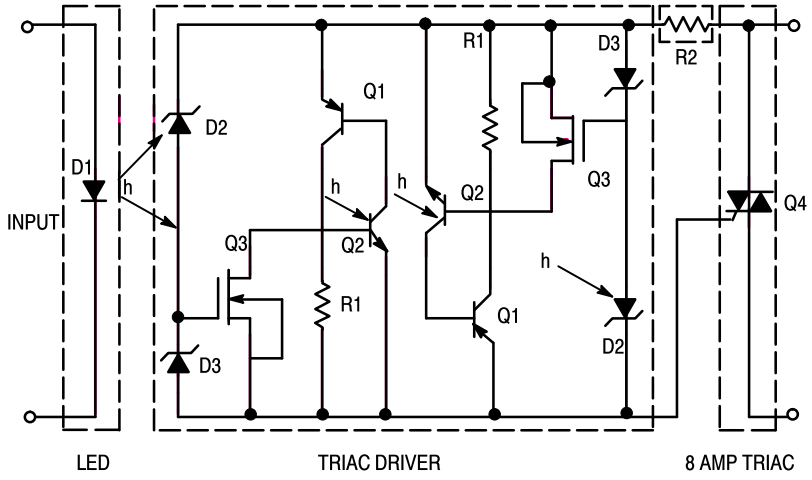

Figure 2. 2 Amp Optocoupler Circuit

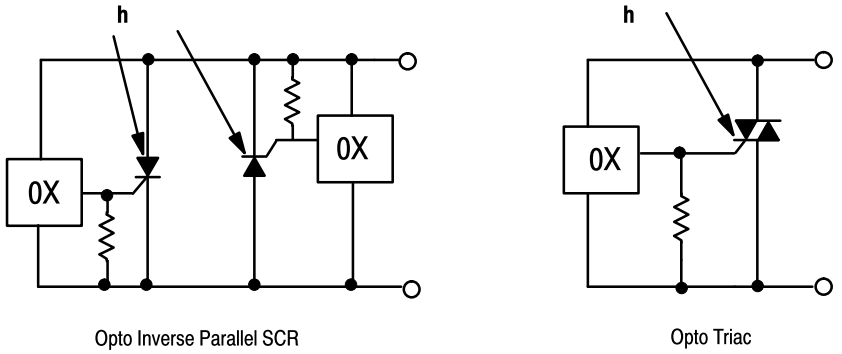

Figure 3. Triac Driver Simplified Circuits

OPERATION

An LED current of several mA will generate a photo current of several tens of micro amps in the collector base junctions of the NPN transistors of the triac driver chip. The SCR formed by the NPN-PNP transistor combination latches on when the photo generated current is present and the line voltage is below the inhibit voltage window, or in other words, within the zero cross window. Once the triac driver is latched on it allows sufficient current flow to the gate of the main triac which in turn latches on and carries the load current.

If the LED is turned on at a time when the line voltage exceeds the inhibit voltage, the driver is effectively disabled and will wait to latch on until the line voltage falls below the inhibit voltage. The driver and triac, however, are not able to switch on at absolute zero line voltage because they need a minimum voltage and current to be able to latch on. For example, if the LED is switched on when the line voltage is zero, the LED flux generates a photo current in the detector of several tens of micro amps, but the triac driver is not able to latch on until the line voltage rises to the driver's minimum main terminal voltage of about 1.0 V and a latching current of several 100 μA is present. A further increase in line voltage is necessary to trigger the main triac because its minimum gate voltage requirement in respect to MT1 voltage is also about 1.0 V and has to be added to the voltage drop across the triac driver. The main triac is able to turn on when at least 2.0 V are across its main terminals and enough gate current is generated to meet the triacs gate trigger current requirement. This is the earliest possible turn-on point within the zero-cross window. Conversely, the maximum inhibit voltage represents the last possible opportunity to turn on within the zero-cross window.

When the main triac is triggered, the voltage across its main terminals collapses to about 1.0 V. Figure 4 shows the zero voltage turn-on characteristic of a POWER OPTO Isolator as observed with an oscilloscope by monitoring the voltage across the main terminals of the device. Figure 5 shows a curve tracer plot which gives information about the voltage and current characteristic.

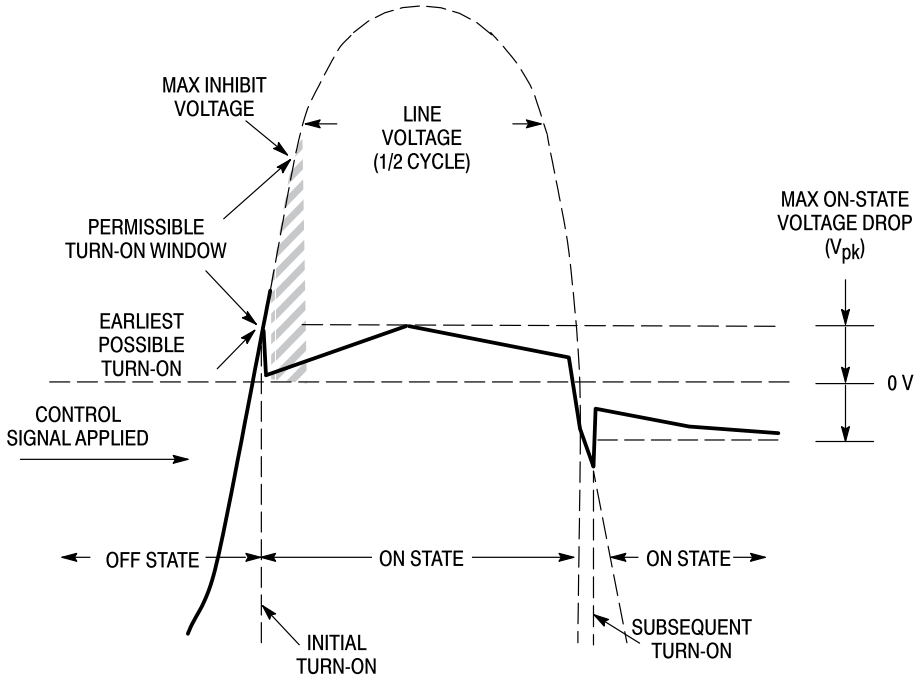

Figure 4. Zero-Voltage Turn-On Voltage Characteristics

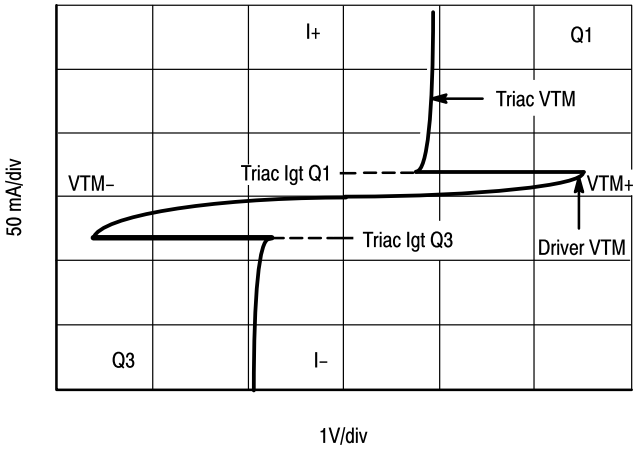

Figure 5. Curve Tracer Voltage versus Current Plot

After the power triac is turned on, the triac driver conducts only several hundred micro amps when the LED is still on but switches off and stays off when the LED current is removed. The main triac remains latched on until the load current falls below the triacs holding current. After this transition point, the driver will exclusively conduct the load current until the current falls below several 100 micro amps. At this point only the photo generated current of several tens of micro amps remains. Triac driver and main triac are switched off and are retriggered every half cycle until the LED is turned off. As the LED is switched off the triac driver is switched off, and the main triac falls out of conduction when the load current falls below the main triac's holding current (typically 20 mA).

The fact that the triac driver has an extremely low holding current allows the minimum load currents to be below the main triac trigger and holding current. In this triac driver only mode, the main triac never conducts and the load is only carried by the triac driver. In this low current triac driver only mode, commutating dv/dt is no longer a function of the main triac commutating capability, but is dependent on the triac drivers commutating dv/dt capability. This is only about 0.5 V/μs and should be considered marginal. Therefore, the use of a snubber is absolutely mandatory when switching loads in triac driver only mode is anticipated.

APPLICATIONS

Snubber Requirements

The application of the 2 amp POWER OPTO Isolators is very simple. Most loads ranging from 30 mA up to 2 A rms, including complex loads as discussed below, may be controlled without the use of a snubber network. Snubbers are required when the static and commutating dv/dt either generated by the load switched by the POWER OPTO Isolators or generated elsewhere on the AC line exceed the device's dv/dt ratings. In industrial environments where large inductive loads are switched on and off by contactors, transients may be generated which surpass the devices static dv/dt rating or the maximum V_{DRM} rating. For these cases a snubber consisting of a resistor and a capacitor will attenuate the rate of rise of the transient. A voltage clipping device (Metal Oxide Varistor MOV) which limits the amplitude of the transients should be used when the amplitude of the transients exceed the devices V_{DRM} ratings. Snubber and transient suppressors are connected across the main terminals of the POWER OPTO Isolator as shown in Figure 6.

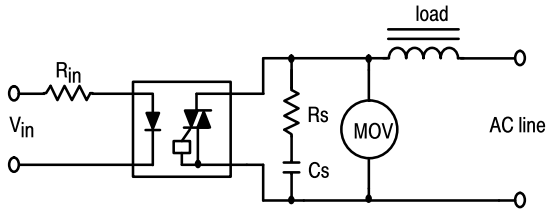

Figure 6. Application with Snubber and MOV

Typical values for the snubber capacitor C's and snubber resistor R's are 0.01 μF and 39 Ω respectively. These values may be adjusted for specific applications. See Application Note AN1048 for detailed information about snubber design considerations.

The placement of the load has no influence on the optocoupler's performance. It may be switched from the line neutral to the phase (hot) side or from the phase to neutral.

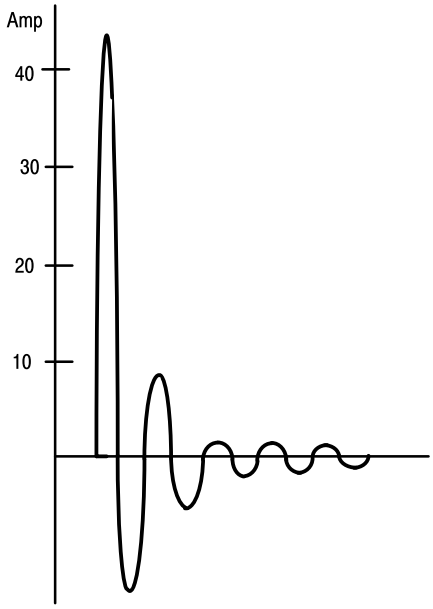

Figure 7. Size No. 4 Contactor Inrush Current

Input Current Requirement

It is very important to supply the data sheet specified input current to the device. Less input current may prevent turn-on of either both light sensitive SCRs or worse, be able to turn on only one SCR due to slight differences in I_{FT} for the positive and negative AC half wave. This situation causes half-waving of the load. Most inductive loads draw excessive current under this condition which may destroy either the load or the optocoupler. Low temperature operation requires increased input LED current as shown on the data sheet's I_{FT} vs. Temperature graph .

For example:

The I_{FT} for a MOC2A40-10 at 25°C is 10 mA, but is at –40°C 15,5 mA (I_{FT} @ 25°C*factor 1.55 as shown on the graph).

This minimum control current requirement dictates the value of the input current limiting resistor R_{in} for a given input voltage.

$$R_{in(max)} = \frac{V_{in} - V_{F(LED)}}{I_{FT(on)}}$$

$$R_{in(min)} = \frac{V_{in} - V_{FL(LED)}}{I_{Fmax}}$$

V_{in} = Input Voltage

$V_{F(LED)}$ = voltage drop across LED = 1.3 V

$I_{FT(on)}$ = specified LED trigger current*factor for low temperature operation

$I_{F(max)}$ = maximum continues LED forward current (50mA)

Complex Loads

Surge Currents in Inductive Loads

Inductive loads may cause very high inrush surge currents because their magnetic core is forced into saturation as observed with transformers or the inductance is low at the initial startup which is typical for relays, solenoids and motors.

Example 1: Size No. 4 Contactor Control

The MOC2A40 has demonstrated its ability to handle large inrush currents by driving a size No. 4 contactor out to 2 million cycles without failure. The device is cycled one second on and one second off. The 115 V_{rms} input coil generates a 50 A peak in the first half cycle, and 20 A peak in the second half cycle as shown in Figure 7. The RMS steady state current is below 1 A. A MOC2A40 in free air is able to control this load without additional heat sinking and without the use of a snubber.

Two million device cycles without failure represent a reliability of M.T.B.F of >19.8 million device cycles.

Example 2: Transformer Inrush Current

It is mandatory in this application to make certain that the inrush current does not exceed the maximum 60 A specified surge current of the device. Residual core magnetization combined with zero cross turn-on may force the transformer into saturation with only the winding resistance left as effective load current limitation. For example, a 150 VA transformer with a 1.5 Ω winding resistance may draw in the first half-cycle up to 80 A of surge current. This excessive surge current can be avoided by using a NTC thermistor in series with the load as shown in Figure 8. A negative temperature coefficient thermistor has a relative high initial resistance when cold, which fast becomes lower due to self-heating in the steady-state operation.

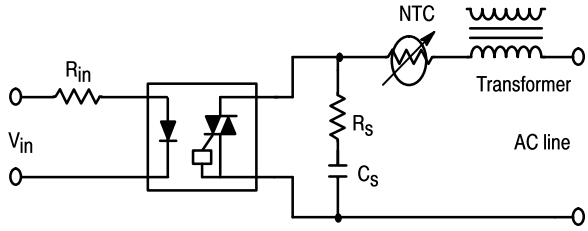

Figure 8. Thermistor Limits Excessive Inrush Current

Example 3: Surge Currents in Capacitive Loads

A rectifier bridge or a single diode in combination with a large capacitor in the micro Farad range represent a very low impedance at startup when the capacitor is being charged. When this type of load is switched on at the peak of the line voltage, the inrush peak current is only limited by the wiring resistance and the ESR of the capacitor. However, the maximum inrush current Ip at zero voltage turn-on is limited by the AC line frequency and the peak line voltage and can be calculated as Ip= C 2π f Vp, where C is the capacitance in Farad, f the line frequency in Herz and Vp the peak line voltage. For an AC line voltage of 120 V_{rms} 60 Hz and a capacitor of 100 μF, the surge current Ip is 6.4 A.

The above calculation for Ip applies to absolute zero voltage turn-on. Turn-on within the zero cross window voltage range of the POWER OPTO Isolators generates considerable higher inrush currents. A 100 μF capacitor switched on at 5.0 V already produced an inrush current of 25 A. Accidental turn-on of the device at the peak of the line voltage charging a 100 μF capacitor without current limitation leads to certain destruction of the power triac. Turn on outside the zero-cross window may be caused by line transients exceeding the devices VTM or dv/dt ratings. A inrush current limiting resistor or NTC Thermistor connected in series to the AC side of the rectifier and the POWER OPTO Isolators output can prevent this potential problem.

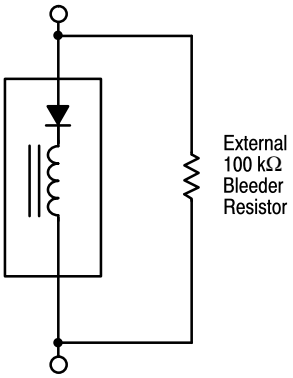

Figure 9. AC-DC Solenoid with Integral Diode

Example 4: AC-DC Solenoid with Internal Rectifier Diode

Some AC-DC relays and solenoids are made ac–dc compatible by using an internal rectifier diode in series with the coil. This poses a problem to a zero-crossing switch because the rectifier diode allows a dc build up across the input terminals. This DC forces the zero-cross switch into the inhibit mode which prevents the load from being switched on. A 100 K bleeder resistor across the input terminals of this type of load prevents dc build up thus allowing proper control. The wattage rating of this resistor is

$$P = \frac{Vrms^2}{R}$$ where P = 1/2 W for 220 V_{rms} and 1/4 W for 115 V_{rms}

Example 5: Controlling an Inductive Load in a Rectifier Bridge

This configuration may cause triac switch off difficulties when the L/R time constant of the inductor to be switched is longer than 1/2 cycle of the line AC. In this case, the load current is not sinusoidal but constant, which causes the current to be switched off rapidly as the line voltage changes polarity. The resulting high commutating di/dt may prevent the triac from turning off. The effect of this commutating dv/dt can be minimized by using a snubber across the device in combination with a commutating softening inductor Ls as shown in Figure 10. Ls is a small high permeability “square loop” inductor which can be constructed by using a ferrite torroid of 3/4″ outside diameter with 33 turns of a number 18 gauge wire. Its core saturates when the load current is high but adds a high inductance when the load current falls below the holding current of the triac. This arrangement slows the rapid di/dt and delays the reapplication of the line voltage which improves the dv/dt capability of the triac.

Thermal Management

To insure proper and reliable operation of the isolated 2 A power switch, it is mandatory to operate the junction of the power triac within or below the maximum specified junction temperature. Temperatures above 125°C may lead to a possible loss of control (permanent latch on) and shortened life of the semiconductors. Junction over temperature problems can be avoided in the application when the devices thermal ratings are properly observed.

Free Standing Power Rating

The 2 Amp POWER OPTO Isolator device families are designed to be able to switch 2 A of AC rms and dissipate 2 W at an ambient free air temperature of up to 40°C without any additional heat sink. The single device rating only applies when free air circulation around the device – i.e. – natural air convection is allowed. There are major differences in effective air convection and the resulting temperature drop between the junction-to-air, depending on the amount and position of the devices on the PC board, and the PC board itself in respect to the natural air flow. Other power dissipating devices in close vicinity of the power switch will raise the ambient temperature which means less power can be dissipated by the switch. This also holds true for enclosures which inhibit or restrict the free air flow around the power switch and result in an increased ambient temperature. The maximum allowed power dissipation versus the increase of ambient temperature is shown in Figure 11. A horizontally positioned PC board with the device in its center will restrict natural air convection, while a vertical positioned PC board with the device positioned along the vertical axis will result in an optimized air convection. Free air flow around the epoxy body of the device and its heat sink creates a thermal air convection that cools the power semiconductor junction. Pin 7 conducts some of the generated heat to the PC board because it is part of the internal power semiconductor heat spreader. This heat transfer can be enhanced when one allows a large metalized area on the PC board at the vicinity of this pin for increased heat spreading.

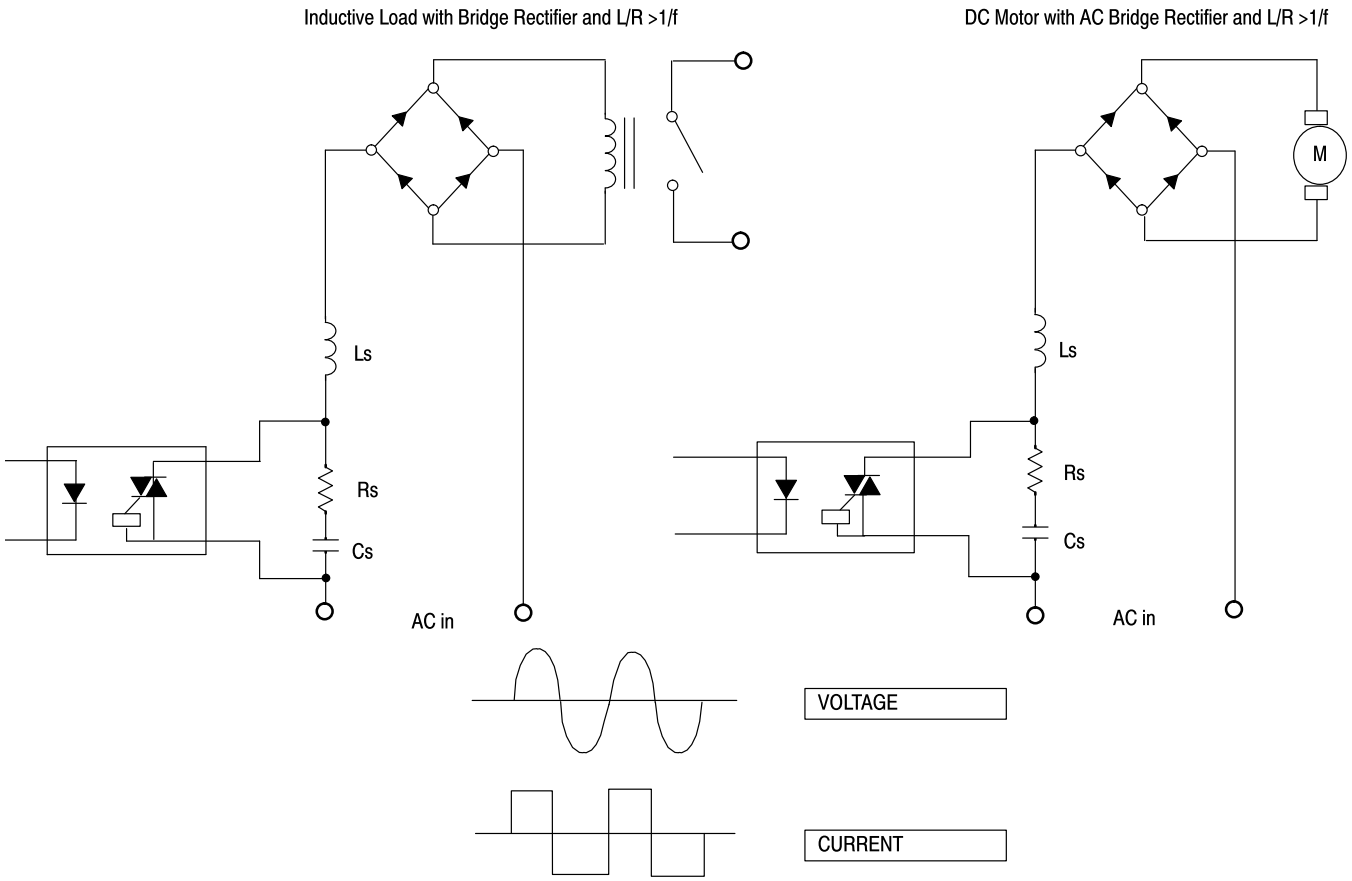

Figure 10. Inductive Loads with Bridge Rectifier

Thermal Resistances of the Device

The heat of the power semiconductor junction is conducted to the internal heat spreader where it is then distributed to the epoxy body and the integral and electrically isolated heat tab of the device. Some of the heat in the heat spreader is transferred to the printed circuit board through main terminal pin 7. The epoxy body, integral heat sink and the PC board transfer this heat to the ambient air. Each heat path has its own thermal resistance. All these thermal resistances are in parallel and grouped together in the device's thermal rating of $R_{\theta JA}$ which is 40°C/W for a free-standing, single device mounted on a PC board.

Thermal resistances are as follows:

$R_{\theta JA}$ Thermal resistance from junction to ambient air = 40°C/W

$R_{\theta JC}$ Thermal resistance junction to case (epoxy body back side and heat tab) = 8°C/W

$R_{\theta JT}$ Thermal resistance junction to heat tab only ~14°C/W. (This is not specified in the data sheet)

$R_{\theta J\ p7}$ Junction to pin 7 (thermocouple on pin 7) ~10°C/W (This is not specified in the data sheet).

$R_{\theta SA}$ Thermal resistance of additional heat sink to ambient.

The junction temperature for a free standing single device is calculated as follows:

$$T_J = (VTM*Irms*R_{\theta JA}) + T_A.$$

Power dissipation equals P = VTM*Irms which is approximately 1 W per Ampere RMS flowing through the main terminals of the device. For exact calculation use the data sheet VTM value for a given current.

The maximum power dissipation for a free standing device is

$$P_{(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

For example, the maximum power dissipation for a free standing MOC2A40 at an ambient temperature of 70°C is

$$P_{(max)} = \frac{125°C - 70°C}{40°C/W} = 1.375\ W \text{ or } I_{(max)} \text{ is } 1.37\ A.$$

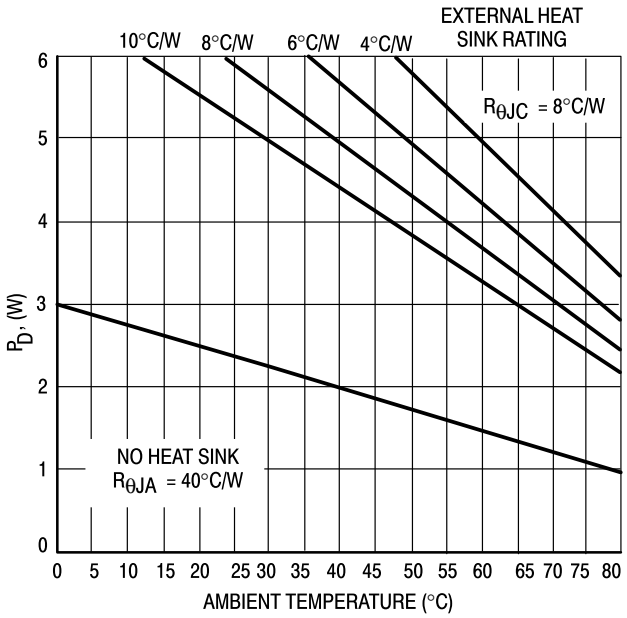

Figure 11. Power Derating versus Ambient Temperature

Material	Conductivity W/Inch °C	Resistivity °C Inch/Watt
Air (100°C)	0.001	1,000
Aluminum	5.63	0.178
Alumina (Al Oxide)	0.55	1.82
Brass	2.97	0.337
Copper	9.93	0.101
Epoxy (Conductive)	0.02	50.0
Iron (Pure)	1.90	0.526
Nickel	1.52	0.658
Nickel Silver	0.84	1.19
Phosphor Bronze	1.80	0.555
Steel (1045)	1.27	0.787
Steel, Stainless (347)	0.41	2.44
Tin	1.60	0.625
Zinc	2.87	0.348

Figure 12. Thermal Resistance of Common Materials Used for Heat Sinking

Devices with Additional Heat Sink

All AC POWER OPTO Isolators contain an 8 A triac chip, but the maximum allowable switching current is limited by the heat dissipation of the package. Significant increase in switching current and the consequent power dissipation is possible by the use of an additional heat sink.

Since the integral sink and the epoxy body of these devices transfer heat, the best results are seen when the devices' entire back side is held in contact with the external heat sink, and thermal grease is used. This mounting method results in optimized heat conduction with the lowest practical possible thermal resistance of 8°C/W which is specified as $R_{\theta JC}$. This includes the thermal resistance of the interface between the device and the heat sink.

Connecting the heat tab only to the external heat sink results in an thermal resistance $R_{\theta JT}$ of 14°C/W which includes the thermal interface resistance between the integral heat sink to the external heat sink .

The external heat sink can be of an extruded type which is commercially available, a flat aluminum plate or simply a part of a sheet metal frame or housing to which the device is held by a steel spring clip. External heat sinks are characterized by $R_{\theta SA}$ which is the thermal resistance from the heat sink to the ambient air. The lower the rating of the heat sink in terms of °C/W the better its thermal efficiency is. Figure 12 shows the thermal resistance of common heat sink materials. This thermal resistance must be added to the optocouplers thermal resistance $R_{\theta JC}$ or $R_{\theta JT}$ where applicable.

There are no electrical safety considerations because the device's heat sink is electrically isolated and regulatory approved.

It is possible to calculate the devices junction temperature T_J as follows, $T_J = ((VTM*Irms*(R_{\theta JC} + R_{\theta CA})) + T_A$.

We are also able to calculate the maximum current and power dissipation allowed as follows,

$$P_{(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JC} + R_{\theta CA}}$$

For example, a MOC2A40 device is mounted with its entire back side to a flat aluminum heat sink with a thermal rating $R_{\theta SA}$ of 5°C/W. Thermal grease is used on the interface and the ambient temperature is maximum 70°C.

$$P_{(max)} = \frac{125°C - 70°C}{8°C/W + 5°C/W} = 4.23\ W$$

The same external heat sink is used but only the device's heat tab is connected to aluminum heat sink which increases the thermal resistance from the semiconductor junction to the external heat sink. Note the considerable loss of power handling capability.

$$P_{(max)} = \frac{125°C - 70°C}{14°C/W + 5°C/W} = 2.89\ W$$

Figure 11 shows the maximum allowed power dissipation for a single free standing device without heat sink and for devices with various external heat sinks versus the ambient temperature.

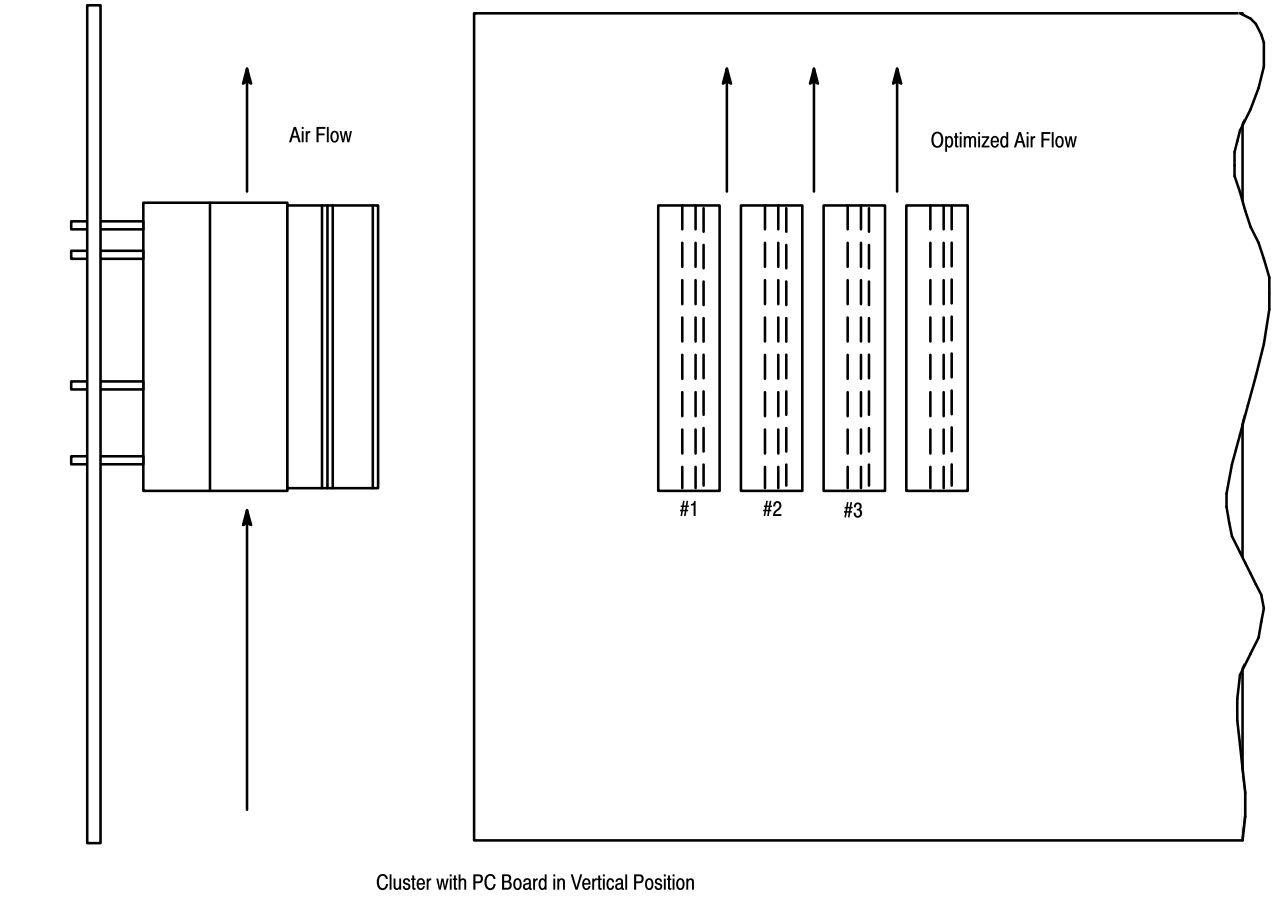

Figure 13. Clusters of Devices on a PC Board

Devices Stacked in Clusters with Minimal Spacing of 200 Mils

One of the great advantages of the 2 A optocoupler family is its small footprint on a PC board. This enables the user to cluster many devices in one row with only 200 mil spacing from lead to lead as shown in Figure 13. Devices in this close approximation influence each other thermally by heat transfer through the epoxy bodies, the integral heat sinks and by heat conduction through pin 7 to the PC board. Prudence would suggests that clustered devices are running much hotter than a single free standing device and the maximum power handling must be derated when all devices within this cluster are switched on. It can be also predicted that devices in the center of the cluster run much hotter than the devices at each end. This also means the individual devices within the cluster are not able to dissipate the full rated power but must be thermally derated. The following study with clusters show the impact of this derating. Of course, the position of this cluster in respect to the natural air convection is also very important. Clusters on a horizontal positioned circuit board run much hotter than devices on a vertical oriented circuit board. Vertical orientation of the devices and the circuit board allow optimized heat flow due to the "chimney" effect. Figure 14 shows the heat distribution for each individual device in a cluster of 10 devices for vertical and horizontal circuit board positions. All devices are conducting 1 A of current which is about 1 W of power dissipation. As predicted, the devices in the center of the cluster show the highest temperature, while the devices at the end run cooler but are still much hotter than the stand alone rating would predict. The graph also demonstrates the importance of free air flow versus restricted air flow caused by a horizontal positioned PC board. It is important to note that the junction temperature of the center devices on the vertical positioned board exceeds the maximum rating of 125°C with a input power of only 1 watt! The dissipated power for these devices has to be lowered in order to stay within their maximum junction temperature rating.

It is now of interest to know the maximum power dissipation allowed for devices in various sized clusters or the maximum power allowed for devices within a large cluster versus the amount of devices switched on at the same time. The graph in Figure 15 is taken from a cluster of 25 devices where the X axis shows the number of units which are turned on with the same power dissipation and the Y axis shows the resulting maximum allowed power dissipation for each unit. The power is first applied to device #1 then to device #1 and device #2 then to device #1 and 2 and 3, and so on. The junction temperature of the hottest unit in the cluster (which is always in the center of the units turned on within the cluster) is the limiting factor. It is also interesting to note that the power derating is not a linear function of the cluster size but asymptotically levels out to a steady value for cluster sizes exceeding 20 devices.

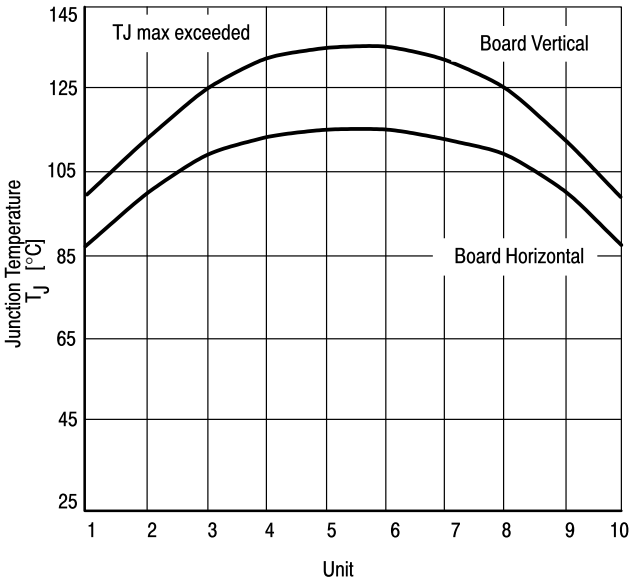

Figure 14. Cluster T_J Junction Temperature Distribution in a Cluster of 10 T_A = 25°C, All Devices on with I = 1 Arms

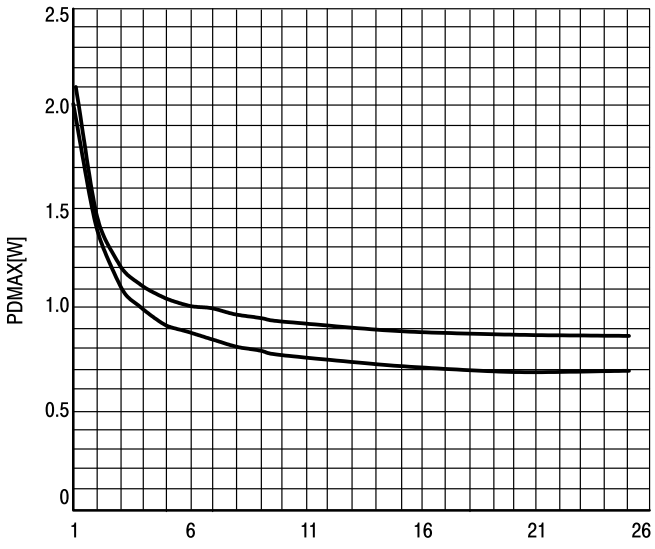

Figure 15. Maximum Allowed Power Dissipation per Device Versus Cluster Size

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