APPLICATION NOTE

AN1431
SA5223 — SONET applications note

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ABSTRACT

The SA5223 is a wideband variable gain transimpedance amplifier fabricated in Philips 1μm "QUBiC" BiCMOS technology. The device is primarily intended for Synchronous Optical Network (SONET) / (OC3) or the International Telecommunications Union, (ITU) Synchronous Transmission Module (STM) applications using NRZ or RZ data format at 155MB/s. The SA5223 has a spectral noise current density of 1.2pA/√Hz with an electrical dynamic range of 105dB. A Bit Error Rate (BER) of 10^{-10} is obtainable for an optical input level of -36dBmW$_{AVG}$.

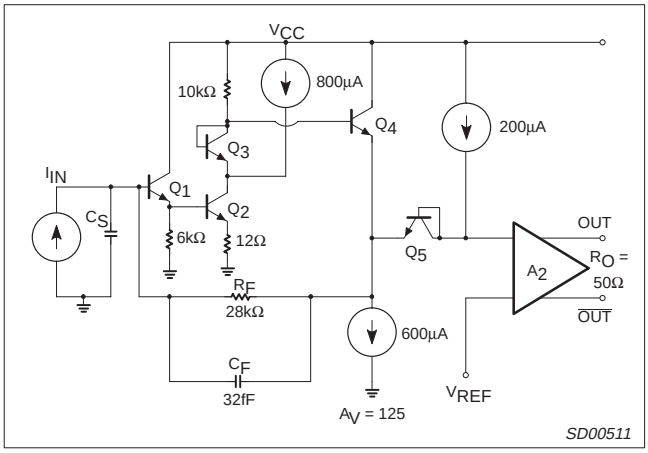

Figure 1. SA5223 Simplified Diagram

THEORY OF OPERATION

Figure 1 shows a simplified diagram of the input stage of the SA5223 without the internal gain control circuitry. The input stage (Q_1-Q_2) is a Darlington bipolar transistor configuration with level translation through series diode, Q_3, to the emitter follower, Q_4. The closed loop transimpedance is set by transistors Q_1 to Q_4 using shunt feedback resistance R_f. Note that the first stage transimpedance is set to 28kΩ at maximum gain. The second stage, A_2, consists of a differential pair having a gain of four, increasing the total transimpedance to about 100kΩ and provides a low impedance output source to drive the postamplifier. The transimpedance varies from 98kΩ with a 1μA input signal to a minimum of 50Ω for an input current of 4mA.

The first stage is designed to provide low noise and a relative insensitivity to input capacitance by use of shunt feedback resistor, R_f. Assigning a first stage voltage gain, A_V, of 125 allows the determination of the input resistance as

$$R_{IN} = \frac{R_F}{1 + A_V} \qquad \text{(EQ. 1.)}$$

where R_{IN} is the Miller resistance as seen by the signal source (Photodiode.) For R_F equal to 28kΩ and for the maximum gain setting:

$$R_{IN} = \frac{28k\Omega}{1 + 125} \approx 220\Omega$$

In a similar manner the equivalent input capacitance is calculated as

$$C_{IN} = (1 + A_V) \cdot C_f \approx 4pF \qquad \text{(EQ. 2.)}$$

These two input parameters set the dominant frequency determining pole of the first transimpedance stage, thus the 3dB bandwidth is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}} \qquad \text{(EQ. 3.)}$$

$$= \frac{1}{2\pi(220\Omega \cdot 4pF)}$$

$$= 180MHz\ (BW_n)$$

By inserting the PIN diode capacitance in EQ 3, the new bandwidth of the first stage can be determined. For instance, if a pin diode with 1pF shunt capacitance is connected to the input of the SA5223, the bandwidth will be lowered as shown below,

$$f_{C-new} = \frac{1}{2\pi(220\Omega \cdot 5pF)} = 145MHz$$

while a PIN diode with 3pF shunt capacitance will lower the bandwidth to 103 MHz. This allows the user to quickly determine if the fiber optic receiver will provide sufficient signal bandwidth for the particular data rate selected. Note that external shunt capacitance also increases the noise gain of the device with increasing frequency. This will be discussed in more detail in the section dealing with receiver noise and the effect of amplifier bandwidth on Bit-Error-Rate (BER).

First Stage Noise Current

Noise current is generated in the first stage due to first stage (Q_1) base current, (shot noise) and resistor noise (thermal noise) generated in the feedback resistor Rf. Both noise sources are random in nature and are limited by the bandwidth of the individual stage as described above. The calculation of the mean squared noise from both sources is shown in equation EQ-4 and is in Amps. The spectral noise density in A/Hz is determined by dividing the mean squared noise by the square-root of the stage bandwidth. Note that the first stage spectral noise density is a constant independent of bandwidth.

$$i_{1n}^2 = [2qI_{B1}BW_n] + \left[\frac{(4kT\ BW_n)}{R_f}\right] \qquad \text{(EQ. 4.)}$$

where I_{B1} is the base current of Q_1 taken as 1μA, q is electron charge, R_f is 28kΩ and BW_n is the noise bandwidth. Thus, the input spectral noise current at room temperature is:

$$I_{1n} = \left[2\ (1.6\ 10^{-19}coul)\ (1\mu A) + 4\ (1.38 \cdot 10^{-23}\frac{J}{K})\ (\ 300K\ )\ \frac{1}{28k\Omega}\right]^{\frac{1}{2}}$$

$$i_{1n} = 9.55 \cdot 10^{-13}\ A/\sqrt{Hz}$$

$$\approx 1pA/\sqrt{Hz}$$

Differential Output Improves Common Mode Noise Rejection

The differential output section of the SA5223 as shown in Figure 2, provides significant improvement in the Bit-Error-Rate over that obtainable with single ended signal detection schemes. After conversion from a single-ended optical to electrical signal, only the differential mode signal is used for threshold detection at the post amplifier. This results in the cancellation of any induced common mode noise before threshold detection takes place. By providing a noise resistant PC board layout around the PIN diode section, where single mode signal levels must be relied upon, the overall preamplifier noise is further reduced.

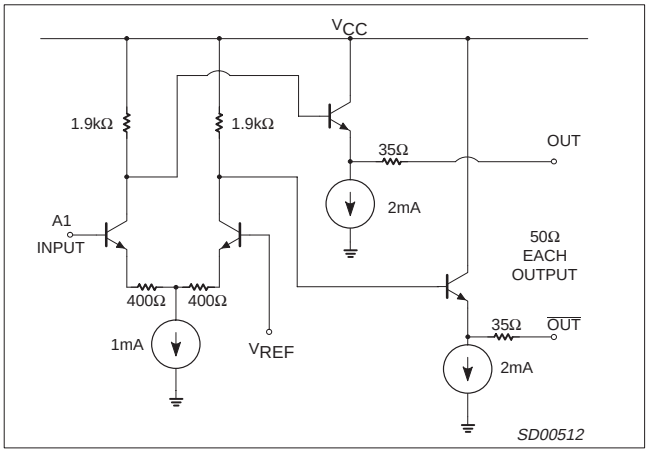

Figure 2. Differential Output Stage A2

The differential gain of A is fixed at approximately 4 by the relatively high emitter to collector feedback ratio and does not vary with AGC. The output common mode voltage of the emitter followers is nominally 3.2V above ground for plus 5V operation. The full peak-to-peak signal levels have a range of ±200 mV around this common mode DC value. Note that the emitter follower output stages are limited to approximately 2mA DC load current for symmetrical signal operation. This corresponds to a minimum ground referenced resistive load at each output of 1.6kΩ. However the differential mode signal is capable of symmetrically driving a 100 Ω load since each output has a typical output impedance of 50 Ω. This allows the use of low impedance RC lowpass filter configurations to improve BER through noise bandwidth limiting.

The AGC Control Section and Its Operation

The AGC control circuit consists of a peak detector which consists of an internal 30pF storage capacitor, signal buffer, and threshold comparator. This circuit provides the gate control bias to the gain control MOSFETs' (Figure 3) The input to the peak detector is taken from the single-ended output of the main differential gain stage, A_2.

AGC Operation

The automatic gain control operates over a range of voltage levels derived from the output of the SA5223. AGC action takes place when the peak output voltage from the second stage buffer amplifier reaches the threshold level of 187mV. This level corresponds to an input current which is calculated using the maximum single ended transimpedance of 50kΩ. The equivalent peak input current to the SA5223 is then derived as

$$I_{in} = \frac{187mV}{50\Omega} = 3.7\mu A \text{ (0 – peak)}$$

The required optical input power is then calculated from the PIN diode responsivity. Choosing the typical PIN responsivity of 0.8 A/ W results in a minimum optical power for which the AGC becomes active as calculated below.

$$P_{in\,min} = \frac{(0.707)\ (3.7\mu A)}{0.8A/W} = 3.3\mu W \text{ optical}$$

This results in a relative power level of

$$P_{dBmW} = 10 \log \left|\frac{3.3\mu W}{1mW}\right| = -25dBmW \text{ optical}$$

With increasing input current, the transimpedance gain (R_T) decreases and IGC (internal loop control current) increases (as shown in Figure 4 where IGC varies from 0μA at maximum gain to 16μA for minimum gain).

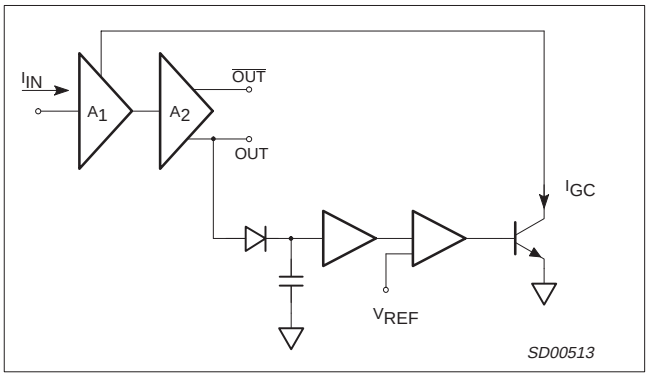

Figure 3. Peak Detector / AGC Generator

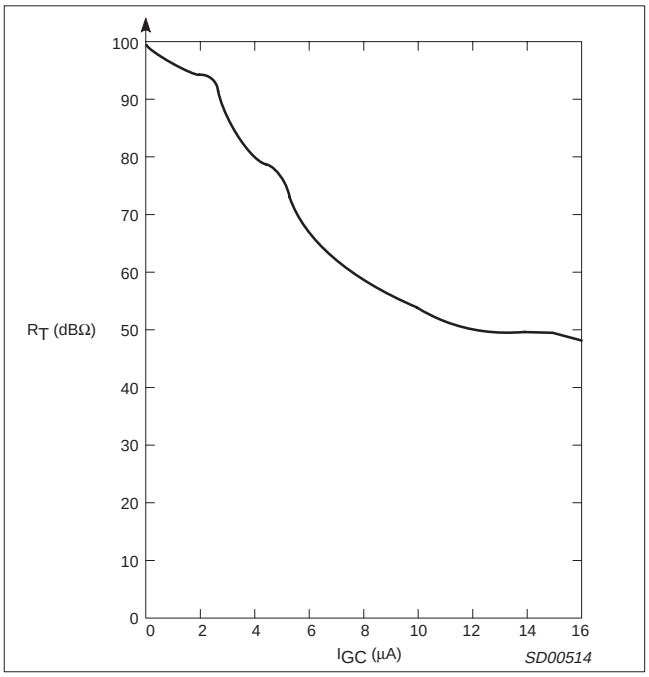

Figure 4. Transimpedance Gain vs IGC

Loop Time Constant

The response time of the AGC loop is determined by a MOSFET peak detector voltage which increases in proportion to the output levels above 187mV thereby charging the 30pF hold capacitor. The hold capacitor voltage is buffered by the MOSFET gain stage and in turn drives the differential transconductance stage. (See Figure 5)

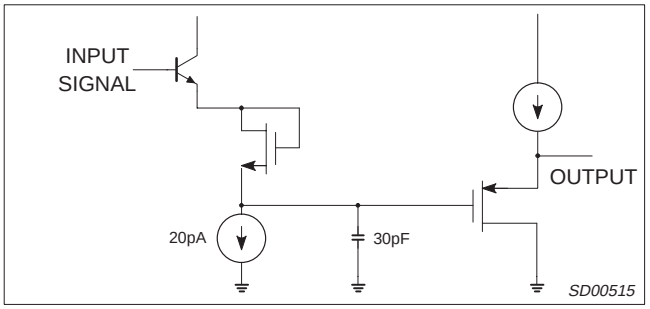

Figure 5. AGC Peak Detector

Amplifier Gain Change with Extended Same Polarity Data

The equation below shows the AGC loop time response for constant amplitude input current or continuous binary 1s or 0s input data patterns.

$$\text{AGC Gain Droop} \approx \pm\ 1\text{dB} \ /\ \text{millisecond}$$
(depends on optical polarity)

Noting that the charge current into the peak detector capacitor is directly proportional to the AC optical signal level at the input, the above equation allows one to calculate how much droop will occur for a given pseudo-random-bit sequence. An absence of optical signal will cause the AGC circuit to respond with a gain increase. Therefore, when the data signal consists of a series of continuous 1s or 0s which last over a long duration, that binary state which removes optical signal will result in a gain increase in the SA5223. To determine the number of same polarity binary bits per dB of gain increase/decrease, the following relationship may be used:

$$\text{Gain Change (dB)} = \frac{1 \cdot 10^{-3}\ \text{seconds}}{\text{Bit Rate (bits/sec)}}$$

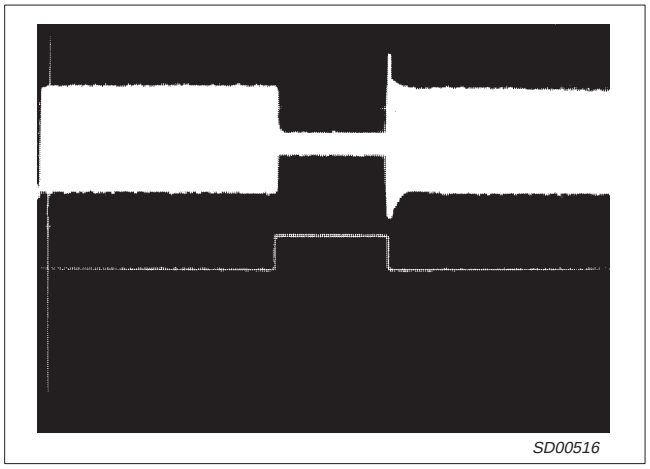

Figure 6. AGC Recovery Transient for 1ms Signal Gap

At 155MB/s it is possible to calculate the gain control function as follows:

For a +1 dB gain change –

$$\text{number of bits per dB} = \frac{1 \cdot 10^{-3}\ \text{seconds}}{1/155 \cdot 10^{6}\text{sec/bit}}$$

$$= \frac{1 \cdot 10^{-3}\ \text{seconds}}{6.45 \cdot 10^{-9}\text{sec/bit}}$$

$$= 155\text{kbits}$$

This corresponds to a PRBS pattern of about (2^{17} - 1). Therefore, a 1dB change in gain will occur for a string of 1s or 0s of greater than 2^{17} bits. Now what is the effect on the system BER due to a data anomaly of this magnitude? First, the noise gain will increase 1dB for each 2^{17} bit pattern group as noted above. Second, the transient recovery response of any time delay system will suffer overshoot and limiting will eventually occur when the alternating data pattern re-appears. However, the amplifier is capable of recovering data without errors due to overshoot distortion up to about 10dB of gain change. Beyond this level some bits would be lost at the restart of data. That is, for continuous same bit patterns above about 2^{18} bits, the system would begin to produce recovery errors. Figure 6 shows an example of this sort of gain and overshoot recovery phenomenon. This ability of the SA5223 to maintain a correct output in the presence of non 50% duty cycle data is unique for integrated transimpedance amplifiers.

Dynamic Gain Range of the SA5223

The overall dynamic range of the SA5223 is approximately (using differential gain).

$$\text{Dynamic Range } (\Omega)\ \frac{100\text{k}\Omega}{50\Omega} = 2000$$

$$= 66\text{dB}\Omega$$

These are hypothetical conditions and are only given to show by what order of magnitude the system function will change if worst case bit patterns exist. In actual SONET applications, the bit stuffing and data preamble will not allow such huge orders of bit pattern variation and there is little concern given to the BER change due AGC time constant.

Optical Signal Dynamic Range of the System

Using a signal-to-noise ratio based on optical power to the receiver, it is possible to obtain a figure of merit for the SA5223 given the PIN diode parameters and the system bandwidth. If it is accepted that the minimum signal power to noise power ratio at the input to the transimpedance amplifier must be at least 12 to 1 for a BER of 10^{-10}, then given the PIN diode dark current, combined geometrically with the equivalent input noise of the SA5223, we may calculate the worst case minimum input power. Using the input spectral noise current of the SA5223 as 1.2pA / Hz, and a dark current for the PIN diode of 5nA_{RMS}, leads to the following result:

$$\text{PIN diode responsivity} = 0.8\text{A/W}$$

$$\text{Bandwidth of the first stage} = 165\text{MHz}$$

$$i_{n5223} = \sqrt{\left[(1.2 \cdot 10^{-12)^2} \cdot 165 \cdot 10^{6}\right]}$$

$$= 15\text{nA}_{\text{RMS}}$$

Therefore the combined current is

$$i_n = \sqrt{(15 \cdot 10^{-9})^2 + (5 \cdot 10^{-9})^2}$$

$$= 16\text{nA}_{\text{RMS}}$$

Using the 12-to-1 signal to noise factor given above for a BER criteria of 10, the minimum input current signal is

$$I_{in\,min} = 12 \cdot 16nA = 190nA_{RMS}$$
$$= 190nA \cdot 1/0.8A/W$$
$$= 238nW \text{ optical}$$
$$= 10 \log (238nW/1mW)$$
$$= -36dBmW \text{ optical}$$

And for an upper input signal current of 3 mA:

$$P_{in} = 3 \cdot 10^{-3}A \;/\; 0.8A/W$$
$$= 3.75mW \text{ optical}$$
$$= 10 \log 3.75mW$$
$$= +5.7dBmW \text{ optical}$$

This gives a total input refered optical dynamic range of 42dB.

NOISE BANDWIDTH

Modifying the Noise Bandwidth of the Output Signal

For many applications it is desired to limit the noise bandwidth of the SA5223. The most obvious method might be to add shunt capacitance to ground at the input creating a shunt filter which limits the signal bandwidth before it is amplified. There is a serious drawback to this method with any shunt feedback transimpedance amplifier. Increasing the shunt capacitance creates a zero in the noise gain transfer function of the stage and degrades the signal-to-noise ratio with increasing frequency.

The recommended method for limiting noise bandwidth is to insert a balanced differential RC filter between the SA5223 output pins which feed the post amplifier. The major requirement is that the filter must pass the most significant spectral frequency components of the data while attenuating the excess noise bandwidth prior to threshold detection.

The particular detection method described in this applications note uses the Philips SA5224 postamplifier. This particular device contains a high gain amplifier coupled with a peak detection circuit, level comparator and differential ECL output drivers. The level detector provides a Jam function which enables the outputs for signals which exceed the user defined threshold. In addition, the postamplifier contains an auto-zero loop which nulls out low frequency DC wander due to changes in the data pattern and SA5223 DC offset. The data format considered is NRZ.

Figure 7 shows the SA5223 with a typical balanced differential RC lowpass filter. Keeping the total differential source resistance low prevents thermal noise voltage generation and allows the use of reasonable values of shunt capacitance for the lowpass filter.

The low level signals encountered when working with long distance fiber are in the range of $25mV_{RMS}$ differential at the output of the preamplifier. This translates to peak-to-peak signals of about 60mV. To illustrate, consider only the typical SA5223 input stage with a spectral noise current of $1.2pA/\sqrt{Hz}$ over a 145MHz bandwidth. The RMS input referred noise current equals about 15nA. This produces about 1.5mV of RMS differential noise at the output of the preamp which is summed with the data signal. The equivalent signal-to-noise ratio is then 20log(25mV/1.5) or 24dBV, or 12dB optical. This is a theoretical maximum for this receiver and easily exceeds the 10.5dB necessary for a BER of 10^{-9}. However, when all other external noise is added from both electrical and optical sources, the limit is not so easily met and bandwidth limiting must be added.

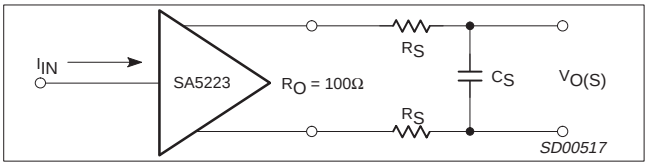

Figure 7. Differential Interstage Noise Filter with Bandwidth B_n

The circuit in Figure 7 shows a single section first-order filter which is tailored to modify the noise bandwidth with a minimum of parts. The design engineer must determine what minimum -3dB frequency to use to optimize the receiver Bit-Error-Rate. Using the Nyquist sampling rule, the NRZ binary signal channel requires a -3dB bandwidth equal to the highest data frequency to be processed by the receiver to insure accurate digital signal detection. The best BER would occur for a square response filter of constant phase with upper bandlimit equal to a bit frequency of continuously alternate 1s and zeros. Such ideal square response filters are not only difficult to design but require additional PC board space. Therefore, a simpler RC-filter is used. This type filter is considered adequate for SONET applications if sufficient bandwidth is allowed to pass the required data signal rise and fall times. The true criteria is that the eye pattern of the data signal must meet the SONET specification for these rise times while improving the signal-to-noise-ratio. The justification for adding the filter is that the SA5223 has excessive bandwidth (145MHz) for the particular OC3 application. In order to define the required noise bandwidth we begin by finding the minimum bandwidth required to pass a sinewave of 155MB/s as shown below.

$$f_{NYQUIST} = \frac{1}{(2bit\ time)}$$

However, setting the first order filter for this -3dB frequency will cause attenuation of the higher order components necessary to define a square wave data signal. The -6 dB-per-octave response region of such a filter degrades the time base accuracy of the bit symbol (creates differential phase error) at the post amplifier. These higher order Fourier components preserve the duty cycle integrity of the data and provide for maximum eye pattern opening. The Nyquist rule must be modified as follows

$$f_{-3dB} > \frac{1}{(2bit\ time)}$$

For a bit rate of 155 MB/s, the bit time is 6.45ns, therefore:

$$f_{-3dB} > \frac{1}{(2 \cdot 6.45 \cdot 10^{-9}sec)} = 77.5MHz$$

How much excess filter bandwidth is necessary to prevent signal risetime degradation while attenuating the noise and thus improving the BER? To find out, we must look at the SONET specification and test the receiver response. One method is to measure the quality of the eye pattern using the standard OC3 test signal rate. In the case shown, a 155MB/s NRZ data stream is used. The eye pattern response is shown in Figure 8. A pseudo random bit sequence of 2^7-1 is used with the filter bandwidth as described. The degree of openness of the eye pattern is a standard method of measureing digitally what is considered S/N for analog signals. In any case, the single pole filter will suffice to both reduce the noise bandwidth while allowing sufficient signal bandwidth to avoid intersymbol interference. This points to the first order RC-lowpass filter as the

most economical solution. It is only necessary to determine the proper -3dB frequency to avoid intersymbol interference while improving BER. The following graph shows the amplitude response of a first order RC filter using the SA5223 internal differential source resistance of 100Ω combined with balanced series resistors of 240Ω and a shunt capacitance.

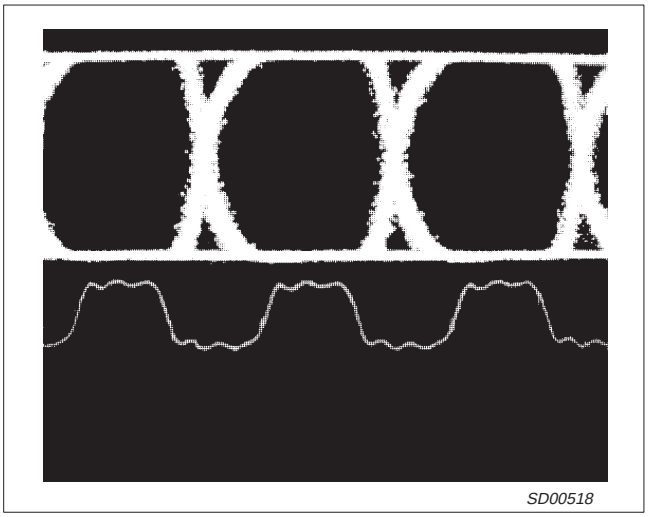

Figure 8. Typical SONET Eye Pattern with -30dBmW Optical Input at 155MB/s

The transfer function for a 99.6MHz RC filter is shown in the graph in Figure 9.

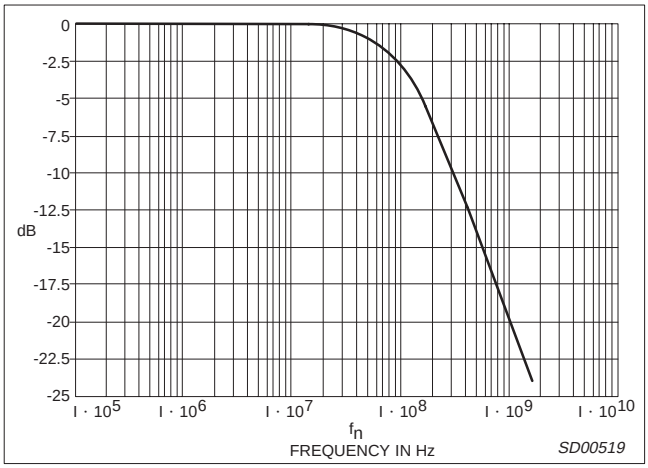

Figure 9. RC Low-pass Noise Filter with R=340Ω and C=4.7pF

(f_c = 99.6MHz)

The noise bandwidth of such a filter differs from the -3dB frequency by the factor

$$\frac{\pi}{2}\ (BW_{-3dB}) = B_n$$

Figure 10 shows the calculated rise and fall time of a filter with this particular set of R_C constants.

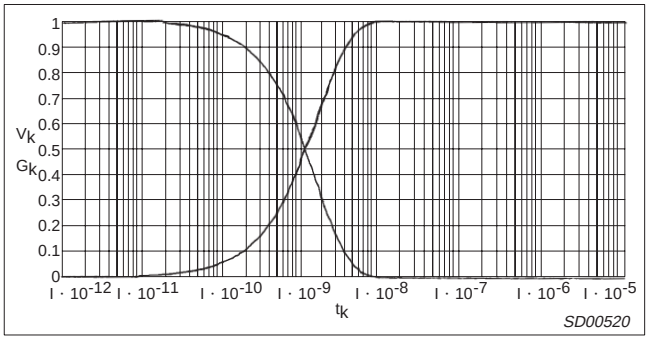

Figure 10. Exponential Rise and Fall Time of the Low-pass Filter

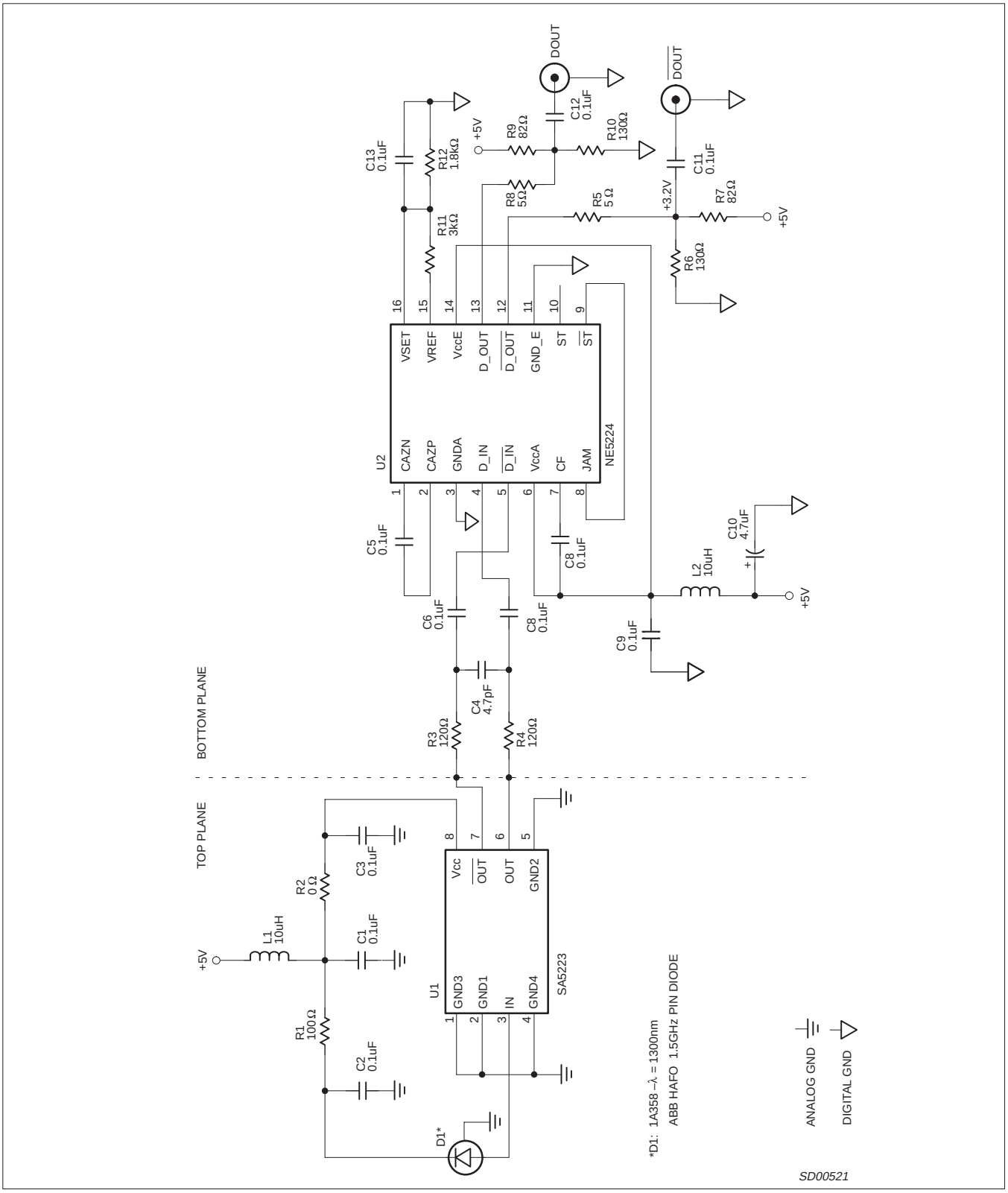

Figure 11. SONET Test Board — 155MB/s (1300nm)

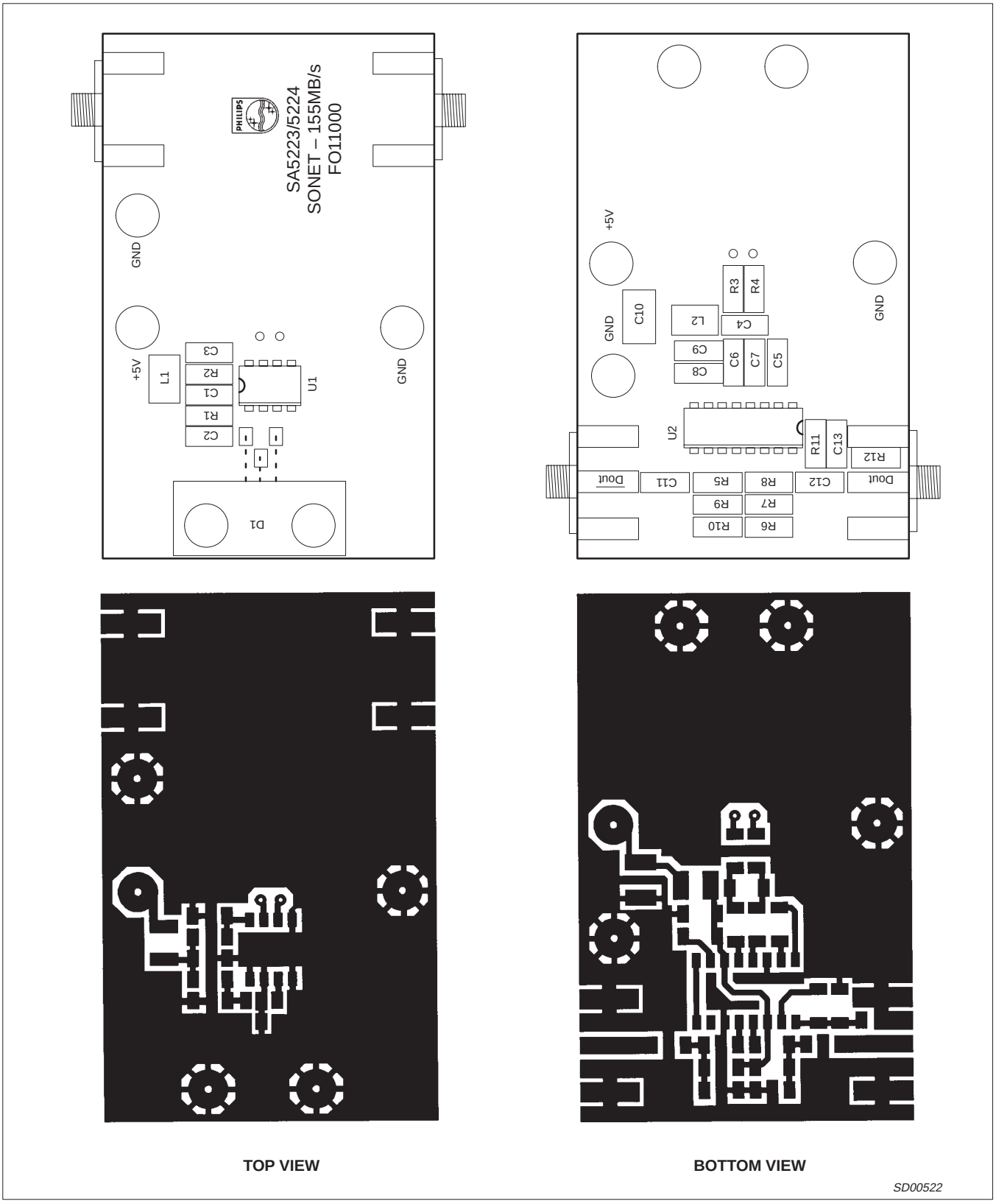

Figure 12. SA5223 Board Layout (NOT ACTUAL SIZE)

Test Results with a Typical SONET Receiver

The circuit in Figure 11 was used to test the Bit-Error-Rate at 155 MB/s using the particular interstage filter bandwidth discussed above. The BER attained at -36 dBmW optical input was 10^{-10}. The printed circuit board layout is critical to meeting the long distance sensitivity specification. Particular care must be used in lead placement for the SA5223. Input ground signals from the PIN diode should be returned to the Pin 2 (GND) node for best noise reduction. V_{CC} on Pin 8 carries the ECL output return currents from the differential outputs and should be kept away from the input circuit ground return currents to avoid oscillation. This is very critical in regards to any high level V_{CC} currents from the post amplifier. These circuits must be well isolated both physically and electrically. A major factor to consider in the combining of pre- and postamps on one board is the very large gain that is present. Because of this, planer coupling capacitance becomes critical. It can be shown that electrostatic coupling from the high level ECL outputs of the post amplifier back to the PIN diode traces entering Pin 3 of the SA5223 only require a few fempto-Farads of input-to-output coupling to cause instability. It was for this reason that the layout of the test and demo board was done as shown with the PIN diode and SA5223 on the top plane and the SA5224 postamplifier on the bottom plane of the PC board. This has resulted in a very stable circuit without any oscillation tendency. However to obtain the best signal to noise the PIN diode leads had to be shielded from outside RF signal emissions. The small electrostatic shield was designed to cover the PIN diode leads and the input side of the SA5223. In the case of a hybrid layout for the SA5223 where the PIN diode is brought into close proximity, V_{CC} decoupling is still a major concern and good bypassing between the supply leads to the PIN and the transimpedance amplifier must be preserved to avoid instability. (Shield shown below, Figure 13.) The bandwidth limiting –3dB frequency to set at 99.7 MHz

The SONET Signal Specification.

The optical signal levels encountered with OC3/SONET are shown below. These levels are tabulated with reference to fiber transmission distances in kilometers.

Levels are in dBmW optical.

Table 1. SONET Signal Specification

Short Range	Medium Range	Long Range
<2km	**<15km**	**<40km**
–8 (maximum)	–8	–10
–15 (minimum)	–28	–34

Under each signal condition, a BER of at least –10 is considered optimum for good communications. The test circuit shown in this applications note will meet this specification using the filter bandwidth shown. In addition, the ABB Hafo 1A358 GaInAs PIN diode or an equivalent device, must be used. All tests are at a 1300nm wavelength. This device has a typical bandwidth of 1.5GHz, a maximum shunt capacitance of 1.2pF with a minimum responsivity of 0.6A/W and a maximum dark current of 3nA.

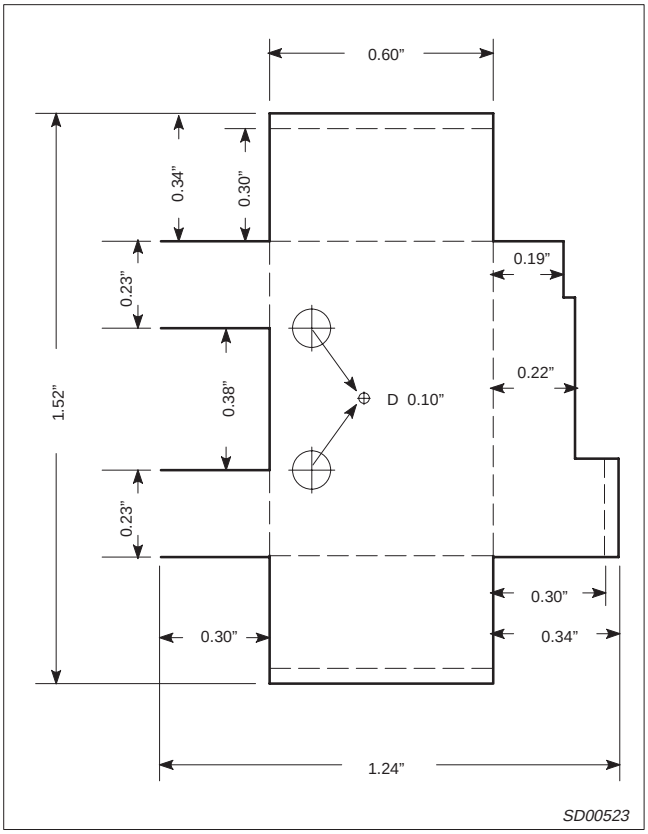

Figure 13. RF Shield Materials: Brass and Tin Plating

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2. John Bellamy, Digital Telephony, 2nd ed., John Wiley & Sons, Inc., 1991
3. Philips Applications Note AN4003, “ A New Fiber Optic Receiver Chip Set for 100MB/s FDDI Data Links. (Applications information on the SA5224 ECL output postamplifier.)
4. Phillips Applications Note AN1443, “Low Cost Fiber Optic Receivers for up to 100 MB/s NRZ.”

SA5223—SONET applications note AN1431

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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