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Application Note

Power Dissipation for Active SCSI Terminators

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This revised application note provides information on the power dissipation and resultant chip junction temperatures when designing with SCSI active terminators. Information on the MCCS142236, MCCS142237 and "active negation" are new in this revision.

10/95

REV 1

MOTOROLA

Power Dissipation for Active SCSI Termination

Much concern has been raised about the ability of silicon based SCSI terminators to reliably dissipate power. The basis of this concern is that all 18-bits of the SCSI bus may remain Low during normal operation. This argument is simply not true. All lines Low represent a hard bus short to ground; a non-functional condition for SCSI. Under normal operation no more than 14 lines can be Low at one time, and the duty cycle of the control bits (other than BSY) is much less than 10%. The following table shows the possible simultaneous assertions on the bus.

Table 1. SCSI Bus Phases (Source: SCSI Bench Reference - ENDL Publications)

BSY	SEL	MSG	C/D	I/O	REQ	ACK	ATN	RST	Data (0-8)	Bus Phase or Condition	
1	0	X	X	X	0	0	X	0	X's	between Information Transfer Phases	
1	0	0	0	0	1	0	X	0	X's	beginning of DATA OUT Phase	
1	0	0	0	0	1	1	X	0	X's	state during DATA OUT Phase	
1	0	0	0	0	0	1	X	0	X's	state during DATA OUT Phase	
1	0	0	0	0	0	0	X	0	X's	state during DATA OUT Phase	
1	**0**	**0**	**0**	**1**	**1**	**0**	**X**	**0**	**X's**	**beginning of DATA IN Phase}**	
1	**0**	**0**	**0**	**1**	**1**	**1**	**X**	**0**	**X's**	**state during DATA IN Phase }**	**worst case: # lines asserted**
1	**0**	**0**	**0**	**1**	**0**	**1**	**X**	**0**	**X's**	**state during DATA IN Phase }**	
1	**0**	**0**	**0**	**1**	**0**	**0**	**X**	**0**	**X's**	**state during DATA IN Phase }**	
1	0	0	1	0	1	0	X	0	X's	beginning of COMMAND Phase	
1	0	0	1	0	1	1	X	0	X's	state during COMMAND Phase	
1	0	0	1	0	0	1	X	0	X's	state during COMMAND Phase	
1	0	0	1	1	1	0	X	0	X's	beginning of STATUS Phase	
1	0	0	1	1	1	1	X	0	X's	state during STATUS Phase	
1	0	0	1	1	0	1	X	0	X's	state during STATUS Phase	
1	0	1	1	0	1	0	X	0	X's	beginning of MESSAGE OUT Phase	
1	0	1	1	0	1	1	X	0	X's	state during MESSAGE OUT Phase	
1	0	1	1	0	0	1	X	0	X's	state during MESSAGE OUT Phase	
1	0	1	1	1	1	0	X	0	X's	beginning of MESSAGE IN Phase	
1	0	1	1	1	1	1	X	0	X's	state during MESSAGE IN Phase	
1	0	1	1	1	0	1	X	0	X's	state during MESSAGE IN Phase	
1	0	1	0	0	1	0	X	0	X's	reserved phase	
1	0	1	0	1	1	0	X	0	X's	reserved phase	
1	0	X	X	X	X	X	1	0	X's	ATTENTION CONDITION	
0	0	X	X	X	X	X	X	0	0's	BUS FREE	
0	0	X	X	X	X	X	X	1	0's	RESET CONDITION	
1	0	0	0	0	0	0	0	0	X's	ARBITRATION	
1	1	0	0	X	0	0	X	0	X's	bus winner takes bus	
0	1	0	0	0	0	0	1	0	X's	SELECTION	
1	1	0	0	0	0	0	1	0	Xs	Target responds to Selection	
1	0	0	0	0	0	0	1	0	X's	Initiator responds to Target	
0	1	0	0	1	0	0	0	0	X's	RESELECTION	
1	1	0	0	1	0	0	0	0	X's	Target responds to Reselection	
1	0	0	0	1	0	0	0	0	X's	Initiator responds to Initiator	
1	0	X	X	X	0	0	X	0	X's	between Information Transfers Phases	
1	0	X	X	X	X	X	1	0	X's	ATTENTION CONDITION	
BSY	**SEL**	**MSG**	**C/D**	**I/O**	**REQ**	**ACK**	**ATN**	**RST**	**Data (0-8)**	**Bus Phase or Condition**	

0 = Negated Release; 1 = Asserted; X = Can be Either State

Duty cycle of each of the 18 SCSI bits was measured while a disk drive emulator was writing (or reading) continuous Lows to the bus. The setup closely simulates the worst case operation. Any other situation will likely lower the power dissipation over what has been measured and shown here. Furthermore, to eliminate the host access time variable, the host access time of the cycle has been disregarded in the power calculations. So, even with the fastest host/controller, power dissipation will only be improved in the user's favor over the data presented below (even the fastest computers have access time). Although it is true that the slower the initiator the longer the data can remain Low, with the trend toward ever increasing speeds, slower initiators are of little concern. Host access time is being ignored in these calculations, anyway.

Reliability data (see Figure 9 and Table 2) assumes that the peripherals are being accessed 24 hours a day, everyday (studies show disk drives are used only an average of 2.4 hours a day). So, on the average, reliability improves about 10 times over the listed values. It may seem that faster data rates have higher power dissipation. However, for SCSI, the opposite is true. Increasing the number of accesses decreases the amount of time that the bus is asserted (Low). Every time that there is an access then the target/initiator must answer. The corresponding response has High or de-asserted signals. When the bus is unused or de-asserted it is High, and no power is consumed by the terminators.

Following are the waveforms (Figure 1 through Figure 6) that occur during a continuous repetitive write (or read) of 512 bytes (a block) of Lows. The driver used in this experiment is a software driven hard disk drive emulator. The waveforms below represent a repetitive cycle of about 340mS duration. 340mS/512bytes equates to 664μS/byte or a 1.51Kbyte/S sustained data rate. This transfer speed is extremely slow and unacceptable by today's standards, making the calculations presented in this note even more conservative. A more reasonable data rate is 1Mbyte/S or 664 times as fast as the experimental data rate. If a system were running at 1Mbyte/S, the repetitive cycle would be repeated 664 times in 340mS. The percentage of time the bus is Low in 340mS would remain basically the same, regardless of the data rate. However, the faster the transfer speed, the less time the chip has to heat up during a cycle, so junction temperatures are further reduced. Also the "Bus Free (Host Access Time)" becomes a possible variable. The access time depends on the speed of the host platform. If the decrease in the access time is not proportional to the increase in the sustained data rate then the SCSI bus lines are High longer and consume less power. Data transfers measured here were performed in the "asynchronous mode," so there is an ACK for each REQ. The ACK signal does not remain Low for long and contributes no appreciable power. RMS voltages are used in the calculations which take into account V_{OH} and V_{OL} levels of the bus signals. The scale used is 1 volt per division vertical and 50mS per division on the horizontal axis.

The "bus free" time between data accesses is ignored to keep the calculations as simple and as general as possible. Referring to Figure 1, the longest period of time that the data lines are High is the time being ignored in the power calculations. So, any access time extends the time that the bus is "free" and improves the power calculations.

Again referring to Figure 1: the first High-to-Low transition begins the data transfer phase; the next transition (Low-to-High) signifies the end of the transfer; the 2nd High-to-Low transition occurs when status is being sent; then the bus goes into the bus free condition (2nd Low-to-High). The pattern is then repeated.

The data from these measurements allows worst case power dissipation to be calculated. Worst case resistance (104.5Ω) and worst case regulator voltage (2.93V) are both used in these calculations. (Please note that worst case resistance and worst case regulator voltage will not normally occur in real systems. The highest voltage and the lowest resistance occur at opposite ends of the temperature range.) Power dissipation estimates can be made for all types of terminators using the data shown in Figure 1 to Figure 6.

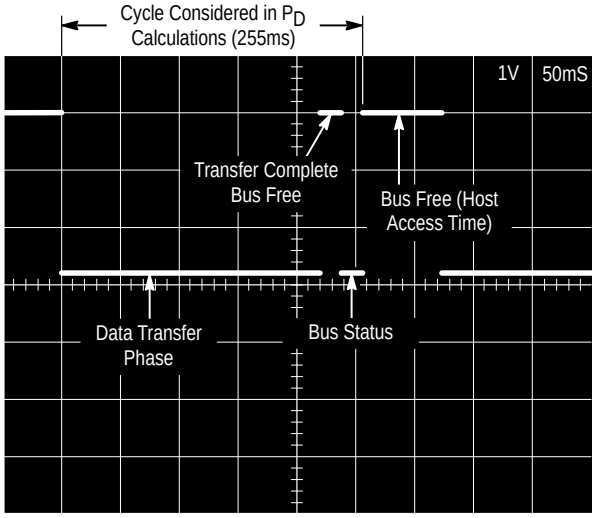

Figure 1. Volts versus Time for DB(0) to DB(7), DB(P); V_{RMS} = 0.814V

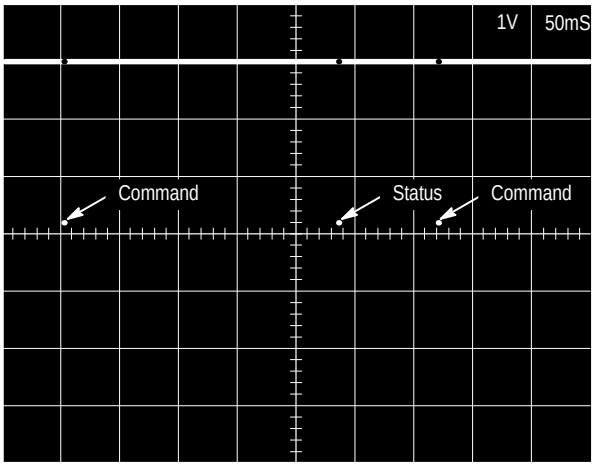

Figure 2. Volts versus Time for SEL, C/D; V_{RMS} = 2.912V

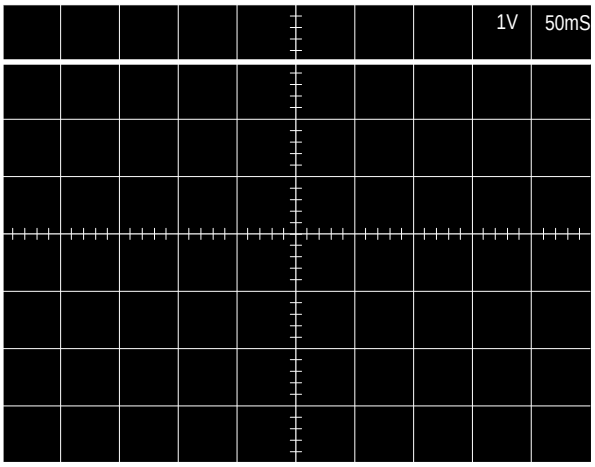

Figure 3. Volts versus Time for ATN, ACK, RST, MSG; V_{RMS} = 2.911V

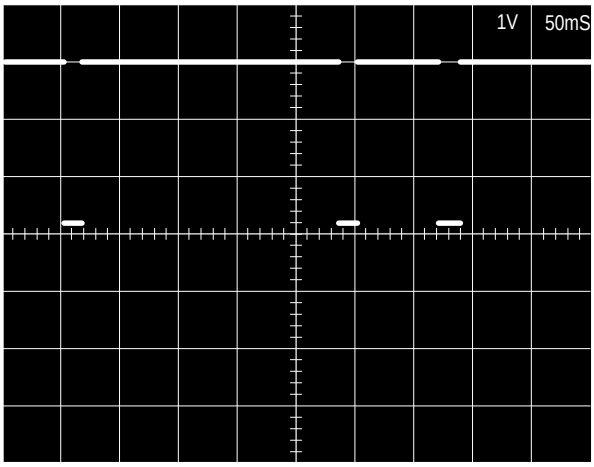

Figure 4. Volts versus Time for REQ; V_{RMS} = 2.737V

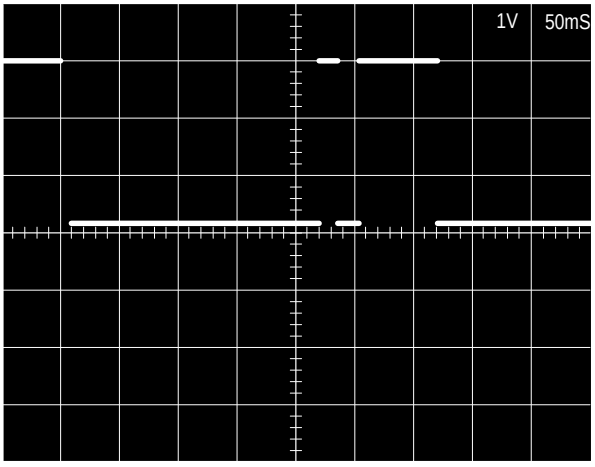

Figure 5. Volts versus Time for BSY; V_{RMS} = 0.730V

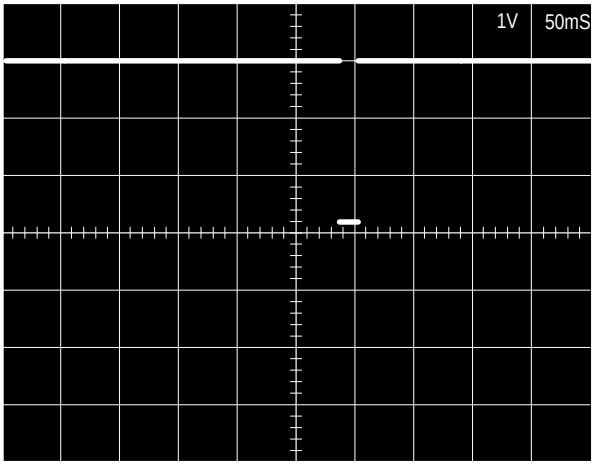

Figure 6. Volts versus Time for I/O; V_{RMS} = 2.823V

Power Dissipation and Junction Temperature Calculations

$P_D = V_{diss} \times I_{diss} = (V_{REG}-V_{RMS}) \times [(V_{REG}-V_{RMS})/R_T]$

V_{REG} = 2.93V, for these measurements
R_T = 104.5Ω
V_{RMS} = RMS voltage each line contributes

For the data/parity pins V_{RMS} = 0.814V

For the SEL and C/D pins V_{RMS} = 2.912V

ATN, ACK, RST and MSG pins have V_{RMS} = 2.911V

REQ has V_{RMS} = 2.737V

BSY looks much like the data and has V_{RMS} = 0.730V

and I/O has V_{RMS} = 2.823V

Using the data shown in the figures, worst case power dissipation can be estimated for each line termination.

P_D = [(2.93-0.814) X (2.93-0.814)/104.5] X 9 = 385.5mW

\+ [(2.93-2.912) X (2.93-2.912)/104.5] X 2 = 0.0062mW

\+ [(2.93-2.911) X (2.93-2.911)/104.5] X 4 = 0.014mW

\+ [(2.93-2.737) X (2.93-2.737)/104.5] X 1 = 0.356mW

\+ [(2.93-0.730) X (2.93-0.730)/104.5] X 1 = 46.3mW

\+ [(2.93-2.823) X (2.93-2.823)/104.5] X 1 = 0.11mW

= 432.3mW.

The calculations show that the Data, Parity and BSY pins contribute the most significant amounts of power dissipation.

Calculating Junction Temperature

$T_J = (P_D) (\varnothing_{JA}) + T_A$

where

T_J = junction temperature (°C)

T_A = ambient temperature (worst case is 70°C)

P_D = Power dissipation

$\varnothing_{JA}$ = thermal resistance of package from junction to ambient with **no forced air flow**

MCCS142235™

Power dissipation for the MCCS142235, Motorola's 18-bit active terminator without an internal voltage regulator, is calculated below. Using the assumptions made before (104.5Ω resistors and 2.93V from the regulator) the worst case power dissipation can be accurately estimated.

The MCCS142235 junction temperature would be:

T_J = 0.4323W X 75°C/W + 70°C = 102.4°C

($\varnothing_{JA}$ for 24-pin SOIC pkg = 75°C/W)

If the '2235 was placed in the TQFP package then the junction temperature would become:

T_J = 0.4323W X 92°C/W + 70°C = 109.8°C

($\varnothing_{JA}$ for 32-pin TQFP pkg = 92°C/W)

Reduction in package size impairs the ability to dissipate power effectively and is represented by an increase in thermal resistance, $\varnothing_{JA}$. Reduction of package size is becoming a necessity in system designs. One method of countering the increased $\varnothing_{JA}$ is to employ special package and heat sinking techniques. The 32-pin FQFP has heat sinking pins placed in each corner of the package. The heat sink pins are electrically isolated from the device. This allows the user to tie these pins to the largest heat sinking medium available without affecting the function of the terminator.

The T_J numbers calculated above cause no long term reliability worries for those using the '2235, either with or without heat sinking.

MC34268

Since the MCCS142235 does not have an onboard voltage regulator, the power dissipation of the MC34268 must also be considered. Using the same measurements and assumptions made previously, the worst case power dissipation can be estimated for the regulator. In this calculation an additional assumption is that a diode (V_D = 0.4V) is placed between TERMPWR and V_{in} of the regulator. Standby power must also be included.

$P_D = I_{CC\_max}$ X (TERMPWR – V_D) + [(V_{REG} – V_{RMS})/R_T] X [(TERMPWR – V_D) – V_{REG}]

Where:

V_D = diode drop voltage (assume 0.4V)
I_{CC_max} = maximum specified I_{CC}
V_{REG} = 2.93V
R_T = 104.5Ω
V_{RMS} = RMS voltage each line contributes

For the data and parity pins V_{RMS} = 0.814V

For the SEL and C/D pins V_{RMS} = 2.912V.

ATN, ACK, RST and MSG pins have V_{RMS} = 2.911V

REQ has V_{RMS} = 2.737V

BSY looks much like the data and has V_{RMS} = 0.730V

and I/O has V_{RMS} = 2.823V

P_D = 15mA X 4.85V
+ [(2.93-0.814)/104.5 X 9
+ (2.93-2.912)/104.5 X 2
+ (2.93-2.911)/104.5 X 4
+ (2.93-2.737)/104.5 X 1
+ (2.93-0.730)/104.5 X 1
+ (2.93-2.823)/104.5 X 1] X 1.92V
= 72.75mW + 398mW = 470.6mW

The MC34268 junction temperature would be:

T_J = 0.4706W X 87°C/W + 70°C = 110.9°C

($\varnothing_{JA}$ for 4-pin DPAK pkg = 87°C/W)

The junction temperature calculation assumes no special heat sinking at all! No additional board space must be used for heat sinking. If the 8-pin SOIC is the package of choice ($\varnothing_{JA}$ = 138°C/W) T_J would be about 135°C without $\varnothing_{JA}$ reduction techniques. The value is a little high, but the assumptions made above are for absolute worst case operating conditions. With a minimum amount of copper flagging (4mm^2) the $\varnothing_{JA}$ is reduced enough to decrease T_J to 106.7°C for worst case 18-bit operation. (refer to the MC34268 data sheet for details of copper flagging). Assuming a 50% duty cycle for data transfer, T_J is reduced to 123.1°C (in 8-pin SOIC) without any $\varnothing_{JA}$ reduction techniques.

MCCS142236

Motorola's 18–bit *integrated* terminator puts eighteen 110Ω pull–up resistors and a 2.85V regulator into one package. The RMS voltages and currents measured and calculated for the 18–bit terminator (MCCS142235) and external regulator (MC34268) can also be applied to the MCCS142236. The power dissipation for this device can be estimated by using the 18–bit terminator without internal regulator power estimation and adding the voltage regulator power. The standby I_{CC} current for the MCCS142236 internal voltage regulator is typically 15mA; the following calculation takes that into account.

T_J = (0.4323W +0.4706W) X 70°C/W + 70°C
= 133.2°C (Worst Case)

($\varnothing_{JA}$ for 28–pin SOIC = 70°C/W)

If this worst case scenario was possible, the time to 0.1% bond failures is about 2 years, if the SCSI drive (or other SCSI peripheral) is used 24 hours a day. If the SCSI drive is used an average amount of time per day (2.4hrs), then it would be nearly 20 years to the time to 0.1% bond failures!

If a "typical" case is assumed, (continue to ignore host access time-hedging toward worst case), then a more realistic power dissipation results. Let the resistor and regulator be typical values (110Ω and 2.85V), and rather than using the multiple of "9" on the data lines, use "4.5" (50% duty cycle).

Calculating the typical integrated terminator power dissipation results in 210.4mW for the resistors and 290.3mW for the regulator portion.

T_J = (0.2104W +0.2903W) X 70°C/W + 70°C
= 105.0°C (“typical”)

This calculation shows that under typical conditions that there are no thermal reliability concerns.

MCCS142237

Motorola’s 9–bit *integrated* terminator (MCCS142237) solution simply stated is one half of the 18–bit solution. The worst case power dissipation for this device is estimated by dividing the 18–bit *integrated* terminator power dissipation by two.

T_J = (0.4323W +0.4706W)**/2** X 99°C/W + 70°C
= 114.7°C

($\varnothing_{JA}$ for 300mil wide 16–pin SOIC = 99°C/W)

T_J = (0.4323W +0.4706W)**/2** X 110°C/W + 70°C
= 119.7°C

(estimated $\varnothing_{JA}$ for thermally enhanced 20–pin TSSOP ≤ 110°C/W)

Using the same assumptions as were used for the “typical” MCCS142236 calculation, the MCCS142237 power dissipation also greatly decreases.

T_J = (0.2104W +0.2903W)**/2** X 99°C/W + 70°C
= 94.8°C (16–pin 300mil wide SOIC)

T_J = (0.2104W +0.2903W)**/2** X 110°C/W + 70°C
= 97.5°C (20–pin TSSOP)

Even the results from the worst case show that there are no thermal related reliability concerns. All equations in this section are based on the assumption that the probable high–current Data, Parity and BSY pins are split evenly between two MCCS142237 devices. Terminating 9 high–current pins in one device would cause the T_J to be much higher than necessary. It is strongly recommended that the user terminate the Data, Parity and BSY pins by dividing them between the 9–bit terminators. (See Figure 7).

Active Negation

What about added power consumption resulting from active negation overshoot? On the surface, it may appear that current caused by an active negation event may add credence to further power concerns. However, after close scrutiny, active negation (fully supported by the MCCS142236 and the MCCS142237) actually provides source current to any active (Low) outputs. Because of this, the regulator does not need to supply all of the source current. Figure 8 illustrates how an active negation incident assists the regulator in providing needed source current to the active (Low) lines.

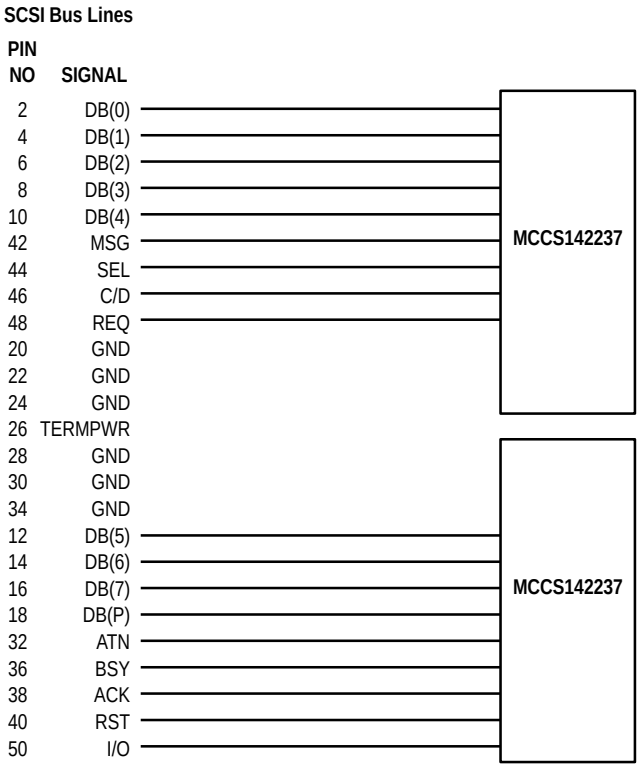

Figure 7. Example of Distributing Most Frequently Asserted Signal Lines

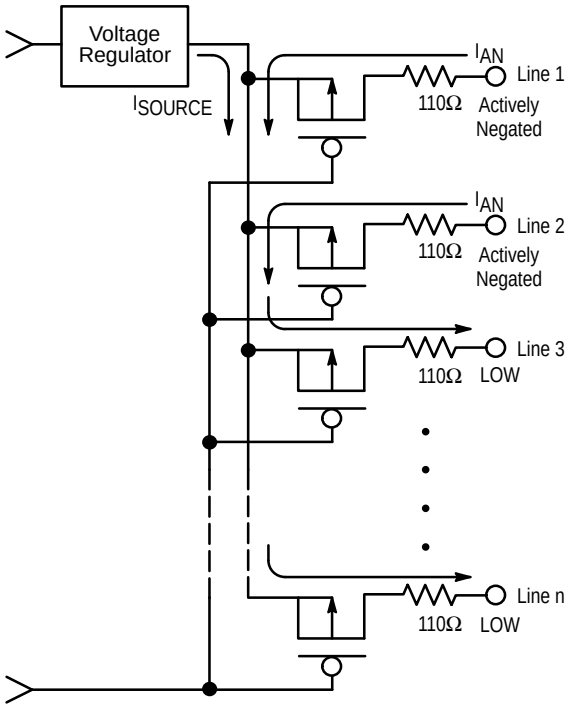

Figure 8. Active Negation Currents

Given that a Low output consumes more power than does an actively negated output (High), the calculations are altered so that the Data, Parity and BSY lines are all Low (still) and the rest of the SCSI control lines are actively negated (Low–to–High). This condition is the newly assumed worst case condition. Using the same equation, found on page 4, the numbers are altered for the new worst case termination scenario. For the purposes of these calculations 3.24V is used as the highest overshoot voltage of an active negation occurrence (3.24V is the worst case overshoot noted in the SCSI–II standard). The following equation applies only to the resistor portion of the integrated terminator.

P_D = [(2.93-0.814) X (2.93-0.814)/104.5] X 9 lines
= 385.5mW(Data(8) + Parity)

+[(3.24-2.93) X (3.24-2.93)/104.5] X 2 lines
= **1.84mW**(SEL + C/D)

+[(3.24-2.93) X (3.24-2.93)/104.5] X 4 lines
= **3.68mW**(ATN, ACK, RST, MSG)

+[(3.24-2.93) X (3.24-2.93)/104.5] X 1 line
= **0.92mW**(REQ)

+[(2.93-0.73) X (2.93-0.73)/104.5] X 1 line
= 46.3mW(BSY)

+[(3.24-2.93) X (3.24-2.93)/104.5] X 1 line
= **0.92mW**(I/O)

= **439.2mW**.

These calculations still show that the Data, Parity and BSY pins by far contribute the most significant amounts of power dissipation.

The power dissipation of the voltage regulator portion will decrease in the event of active negation overshoot.

$P_D = I_{CC}max$ X (TERMPWR – V_D)
+ [(V_{REG} – V_{RMS})/R_T – (V_{AN} – V_{REG})/R_T]
X [(TERMPWR – V_D) – V_{REG}]

(V_{AN}= Maximum active negation voltage noted in the SCSI–II specification)

Notice that the active negation current (sink) is subtracted from the source current. The active negation drivers actually help the regulator source current to the resistors that are pulled Low!

P_D = 15mA X 4.85V

+ [(2.93-0.814)/104.5 X 9

– (3.24-2.93)/104.5 X 2 active negation

– (3.24-2.93)/104.5 X 4 active negation

– (3.24-2.93)/104.5 X 1 active negation

+ (2.93-0.730)/104.5 X 1

– (3.24-2.93)/104.5 X 1] active negation

X 1.92V

= 72.75mW + 344.8mW = **417.5mW**

Using the worst case MCCS142236 equation for comparison, the final junction temperature calculation is T_J=(0.4392W+0.4175W) x 70°C/W + 70°C =130°C for the active negation case.

For the case with no active negation, T_J=(0.4323W+ 0.4706W) x 70°C/W + 70°C =133.2°C. This shows that active negation incidents can reasonably be ignored when calculating power dissipation of an integrated terminator with active negation.

Optimizing the Long Term Reliability of Plastic Package

Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However, when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold (Au) wire bonded to aluminum (Al) bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time, an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time

Based on the results of almost ten (10) years of +125°C operating life testing, a special Arrhenius equation for Au to Al integrity has been developed to show the relationship between junction temperature and reliability. Table 2 shows the relationship between junction temperature and continuous operating time to 0.1% bond failure, (1 failure per 1000 bonds).

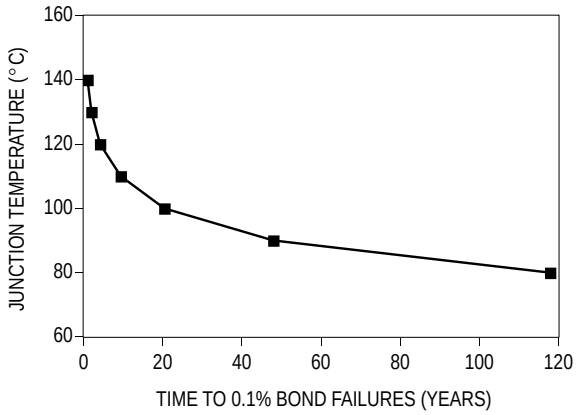

Figure 9. Junction Temperature versus Time to 0.1% Bond Failures (Years)

Table 2. Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature (°C)	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

System Considerations

The junction temperature versus time to bond failures calculations are estimates of device capabilities based upon specific test conditions. The test conditions used were the same as those used industry wide. The manner in which an IC is mounted and positioned in its surrounding system environment will have a significant effect on the IC junction temperature. The conditions are wholly under the control of the system designer and should be seriously considered in board layout, system ventilation and airflow features.

Forced-air cooling will significantly reduce $\varnothing_{JA}$. Air flow parallel to the long dimension of the package is generally a few percent more effective than air flow perpendicular to the long dimension of the package. In actual board layouts, other components can provide air flow blocking and flow turbulence, which may affect the net reduction of $\varnothing_{JA}$.

External heat sinks applied to an IC can improve thermal resistance by increasing heat flow to the ambient environment. Heat sink performance will vary by size, material, design, and system air flow. Heat sinks can provide a substantial improvement.

Package mounting can affect thermal resistance. Surface mount packages dissipate significant amounts of heat through the leads. Improving heat flow from package leads to ambient will decrease thermal resistance.

The metal (copper) traces on PC boards conduct heat away from the package and dissipate it to the ambient; thus the larger the trace area the lower the thermal resistance.

The use of *thermally conductive adhesive* under SOICs can lower thermal resistance by providing a direct heat flow path from the package to the board. High thermal conductivity board material and cool board temperatures amplify this effect.

High thermal conductive board material will decrease thermal resistance. Data indicates that a change in board material from epoxy laminate to ceramic reduces thermal resistance.

Conclusions

Thermal management remains a major concern of producers and users of ICs. As IC manufacturing continues pushing the limits of surface mount technology, a thorough understanding of both device and system thermal characteristics becomes increasingly important.

As SMD packages are reduced in size, the resulting $\varnothing_{JA}$ increases. The increased $\varnothing_{JA}$ is the major trade-off that must be accepted for package miniaturization. The end user must consider the variables that affect the IC junction temperature and take advantage of the material, tools, and data that are available.

SCSI terminators are required to sink up to 24mA per pin. Proper board layout and judicious use of heat sinks, the problems associated with high junction temperatures can be avoided. If the peripherals are not constantly accessed and/or the data on the bus is an even mix of Highs and Lows, the worst case calculations made in this note become extremely conservative. Remember, the worst case power dissipation assumptions are made in this paper. Power dissipation and junction temperature will only improve from the numbers presented.

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