AN1406
Application Note

Designing With PECL (ECL at +5.0V)

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This application note provides detailed information on designing with Positive Emitter Coupled Logic (PECL) devices.

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Designing With PECL (ECL at +5.0V)

The High Speed Solution for the CMOS/TTL Designer

Introduction

PECL, or Positive Emitter Coupled Logic, is nothing more than standard ECL devices run off of a positive power supply. Because ECL, and therefore PECL, has long been the "black magic" of the logic world many misconceptions and falsehoods have arisen concerning its use. However, many system problems which are difficult to address with TTL or CMOS technologies are ideally suited to the strengths of ECL. By breaking through the wall of misinformation concerning the use of ECL, the TTL and CMOS designers can arm themselves with a powerful weapon to attack the most difficult of high speed problems.

It has long been accepted that ECL devices provide the ultimate in logic speed; it is equally well known that the price for this speed is a greater need for attention to detail in the design and layout of the system PC boards. Because this requirement stems only from the speed performance aspect of ECL devices, as the speed performance of any logic technology increases these same requirements will hold. As can be seen in Table 1 the current state-of-the-art TTL and CMOS logic families have attained performance levels which require controlled impedance interconnect for even relatively short distances between source and load. As a result system designers who are using state-of-the-art TTL or CMOS logic are already forced to deal with the special requirements of high speed logic; thus it is a relatively small step to extend their thinking from a TTL and CMOS bias to include ECL devices where their special characteristics will simplify the design task.

Table 1. Relative Logic Speeds

Logic Family	Typical Output Rise/Fall	Maximum Open Line Length (L_{max})*
10KH	1.0ns	3"
ECLinPS	400ps	1"
FAST	2.0ns	6"
FACT	1.5ns	4"

* Approximate for stripline interconnect ($L_{max} = T_r/2T_{pd}$)

System Advantages of ECL

The most obvious area to incorporate ECL into an otherwise CMOS/TTL design would be for a subsystem which requires very fast data or signal processing. Although this is the most obvious it may also be the least common. Because of the need for translation between ECL and CMOS/TTL technologies the performance gain must be greater than the overhead required to translate back and forth between technologies. With typical delays of six to seven nanoseconds for translating between technologies, a significant portion of the logic would need to be realized using ECL for the overall system performance to improve. However, for very high speed subsystem requirements ECL may very well provide the best system solution.

Transmission Line Driving

Many of the inherent features of an ECL device make it ideal for driving long, controlled impedance lines. The low impedance of the open emitter outputs and high input impedance of any standard ECL device make it ideally suited for driving controlled impedance lines. Although designed to drive 50Ω lines an ECL device is equally adept at driving lines of impedances of up to 130Ω without significant changes in the AC characteristics of the device. Although some of the newer CMOS/TTL families have the ability to drive 50Ω lines many require special driver circuits to supply the necessary currents to drive low impedance transmission interconnect. In addition the large output swings and relatively fast output slew rates of today's high performance CMOS/TTL devices exacerbate the problems of crosstalk and EMI radiation. The problems of crosstalk and EMI radiation, along with common mode noise and signal amplitude losses, can be alleviated to a great degree with the use of differential interconnect. Because of their architectures, neither CMOS nor TTL devices are capable of differential communication. The differential amplifier input structure and complimentary outputs of ECL devices make them perfectly suited for differential applications. As a result, for systems requiring signal transmission between several boards, across relatively large distances, ECL devices provide the CMOS/TTL designer a means of ensuring reliable transmission while minimizing EMI radiation and crosstalk.

Figure 1 shows a typical application in which the long line driving, high bandwidth capabilities of ECL can be utilized. The majority of the data processing is done on wide bit width words with a clock cycle commensurate with the bandwidth capabilities of CMOS and TTL logic. The parallel data is then serialized into a high bandwidth data stream, a bandwidth which requires ECL technologies, for transmission across a long line to another box or machine. The signal is received differentially and converted back to relatively low speed parallel data where it can be processed further in CMOS/TTL logic. By taking advantage of the bandwidth and line driving capabilities of ECL the system minimizes the number of lines required for interconnecting the subsystems without sacrificing the overall performance. Furthermore by taking advantage of PECL this application can be realized with a single five volt power supply. The configuration of Figure 1 illustrates a situation where the mixing of logic technologies can produce a design which maximizes the overall performance while managing power dissipation and minimizing cost.

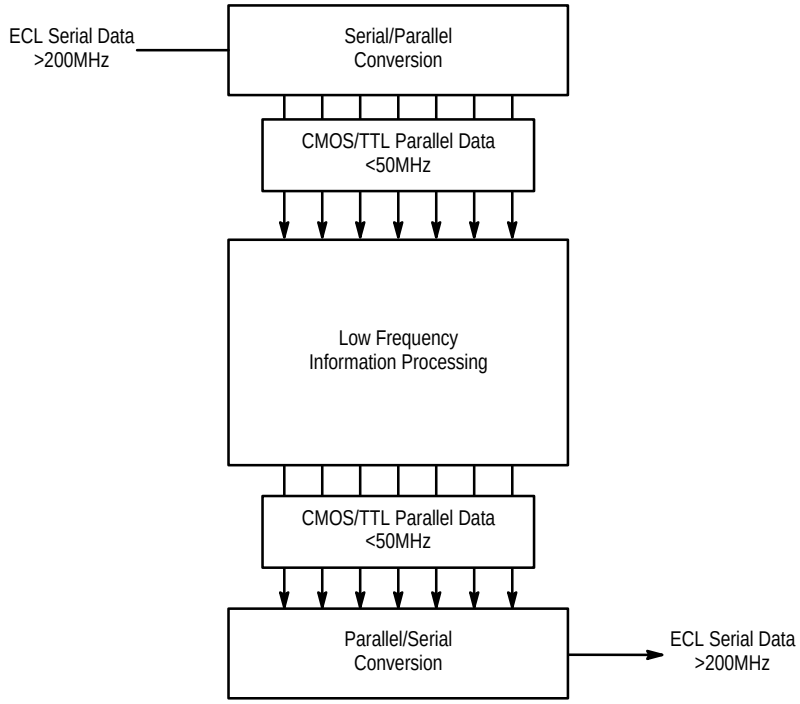


Figure 1. Typical Use of ECL's High Bandwidth, Line Driving Capabilities

Clock Distribution

Perhaps the most attractive area for ECL in CMOS/ TTL designs is in clock distribution. The ever increasing performance capabilities of today's designs has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions throughout an entire system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or costly, faster logic. ECL logic has the capability of significantly reducing the clock skew of a system over an equivalent design utilizing CMOS or TTL technologies.

The skew introduced by a logic device can be broken up into three areas; the part-to-part skew, the within-part skew and the rise-to-fall skew. The part-to-part skew is defined as the differences in propagation delays between any two devices while the within-device skew is the difference between the propagation delays of similar paths for a single device. The final portion of the device skew is the rise-to-fall skew or simply the differences in propagation delay between a rising input and a failing input on the same gate. The within-device skew and the rise-to-fall skew combine with delay variations due to environmental conditions and processing to comprise the part-to-part skew. The part-to-part skew is defined by the propagation delay window described in the device data sheets.

Careful attention to die layout and package choice will minimize within-device skew. Although this minimization is independent of technology, there are other characteristics of ECL which will further reduce the skew of a device. Unlike their CMOS/TTL counterparts, ECL devices are relatively insensitive to variations in supply voltage and temperature. Propagation delay variations with environmental conditions must be accounted for in the specification windows of a device. As a result because of ECLs AC stability the delay windows for a device will inherently be smaller than similar CMOS or TTL functions.

The virtues of differential interconnect in line driving have already been addressed, however the benefits of differential interconnect are even more pronounced in clock distribution. The propagation delay of a signal through a device is intimately tied to the switching threshold of that device. Any deviations of the threshold from the center of the input voltage swing will increase or decrease the delay of the signal through the device. This difference will manifest itself as rise-to-fall skew in the device. The threshold levels for both CMOS and TTL devices are a function of processing, layout, temperature and other factors which are beyond the control of the system level designer. Because of the variability of these switching references, specification limits must be relaxed to guarantee acceptable manufacturing yields. The level of relaxation of these specifications increases with increasing logic depth. As the depth of the logic within a device increases the input signal will switch against an increasing number of reference levels; each encounter will add skew when the reference level is not perfectly centered. These relaxed timing windows add directly to the overall system skew. Differential ECL, both internal and external to the die, alleviates this threshold sensitivity as a DC switching reference is no longer required. Without the need for a switching reference the delay windows, and thus system skew, can be significantly reduced while maintaining acceptable manufacturing yields.

What does this mean to the CMOS/TTL designer? It means that CMOS/TTL designers can build their clock generation card and backplane clock distribution using ECL. Designers will not only realize the benefits of driving long lines with ECL but will also be able to realize clock distribution networks with skew specs unheard of in the CMOS/TTL world. Many

specialized functions for clock distribution are available from Motorola (MC10/100E111, MC10/100E211, MC10/100EL11). Care must be taken that all of the skew gained using ECL for clock distribution is not lost in the process of translating into CMOS/TTL levels. To alleviate this problem the MC10/100H646 can be used to translate and fanout a differential ECL input signal into TTL levels. In this way all of the fanout on the backplane can be done in ECL while the fanout on each card can be done in the CMOS/TTL levels necessary to drive the logic.

Figure 2 illustrates the use of specialized fanout buffers to design a CMOS/TTL clock distribution network with minimal skew. With 50ps output-to-output skew of the MC10/100E111 and 1ns part-to-part skew available on the MC10/100H646 or MC10/100H641, a total of 72 or 81 TTL clocks, respectively, can be generated with a worst case skew between all outputs of only 1.05ns. A similar distribution tree using octal CMOS or TTL buffers would result in worst case skews of more than 6ns. This 5ns improvement in skew equates to about 50% of the up/down time of a 50MHz clock cycle. It is not difficult to imagine situations where an extra 50% of time to perform necessary operations would be either beneficial or even a life saver. For more information about using ECL for clock distribution, refer to application note AN1405/D – ECL Clock Distribution Techniques.

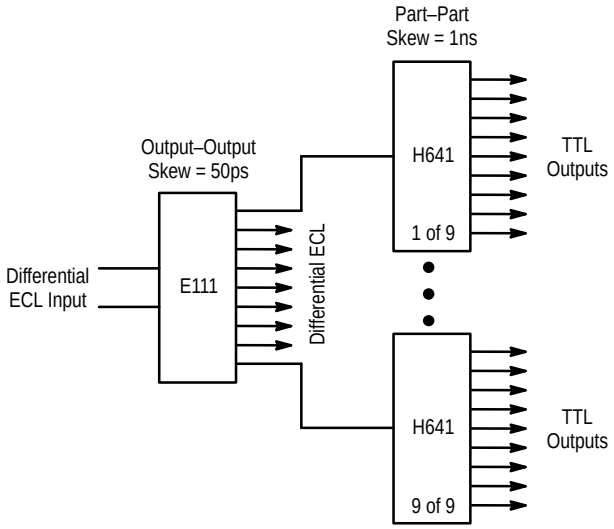


Figure 2. Low Skew Clock Fanout Tree

PECL versus ECL

Nobody will argue that the benefits presented thus far are not attractive, however the argument will be made that the benefits are not enough to justify the requirements of including ECL devices in a predominantly CMOS/TTL design. After all the inclusion of ECL requires two additional negative voltage supplies; V_{EE} and the terminating voltage V_{TT}. Fortunately this is where the advantages of PECL come into play. By using ECL devices on a positive five volt CMOS/TTL power supply and using specialized termination techniques ECL logic can be incorporated into CMOS/TTL designs without the need for additional power supplies. What about power dissipation you ask, although it is true that in a DC state ECL will typically dissipate more power than a CMOS/TTL counterpart, in applications which operate continually at frequency, i.e.. clock distribution, the disparity between ECL and CMOS/TTL power dissipation is reduced. The power dissipation of an ECL device remains constant with frequency while the power of a CMOS/TTL device will increase with frequency. As frequencies approach 50MHz the difference between the power dissipation of a CMOS or TTL gate and an ECL gate will be minimal. 50MHz clock speeds are becoming fairly common in CMOS/TTL based designs as today's high performance MPUs are fast approaching these speeds. In addition, because ECL output swings are significantly less than those of CMOS and TTL the power dissipated in the load will be significantly less under continuous AC conditions.

It is clear that PECL can be a powerful design tool for CMOS/TTL designers, but where can one get these PECL devices. Perhaps the most confusing aspect of PECL is the misconception that a PECL device is a special adaptation of an ECL device. In reality *every* ECL device is also a PECL device; there is nothing magical about the negative voltage supply used for ECL devices. The only real requirement of the power supplies is that the potential difference described in the device data sheets appears across the upper and lower power supply rails (V_{CC} and V_{EE} respectively). A potential stumbling block arises in the specified V_{EE} levels for the various ECL families. The 10H and 100K families specify parametric values for potential differences between V_{CC} and V_{EE} of 4.94V to 5.46V and 4.2V to 4.8V respectively; this poses a problem for the CMOS/TTL designer who works with a typical V_{CC} of 5.0V ±5%. However, because both of these ECL standards are voltage compensated both families will operate perfectly fine and meet all of the performance specifications when operated on standard CMOS/TTL power supplies. In fact, Motorola is extending the V_{EE} specification ranges of many of their ECL families to be compatible with standard CMOS/TTL power supplies. Unfortunately earlier ECL families such as MECL 10K™ are not voltage compensated and therefore any reduction in the potential difference between the two supplies will result in an increase in the V_{OL} level, and thus a decreased noise margin. For the typical CMOS/TTL power supplies a 10K device will experience an ≈50mV increase in the V_{OL} level. Designers should analyze whether this loss of noise margin could jeopardize their designs before implementing PECL formatted 10K using 5.0V ± 5% power supplies.

The traditional choice of a negative power supply for ECL is the result of the upper supply rail being used as the reference for the I/0 and internal switching bias levels of the technology. Since these critical parameters are referenced to the upper rail any noise on this rail will couple 1:1 onto them; the result will be reduced noise margins in the design. Because, in general, it is a simpler task to keep a ground rail relatively noise free, it is beneficial to use the ground rail as this reference. However when careful attention is paid to the power supply design, PECL can be used to optimize system performance. Once again the use of differential PECL will simplify the designer's task as the noise margins of the system will be doubled and any noise riding on the upper V_{CC} rail will appear as common mode noise; common mode noise will be rejected by the differential receiver.

MECL to PECL DC Level Conversion

Although using ECL on positive power supplies is feasible, as with any high speed design there are areas in which special attention should be placed. When using ECL devices with positive supplies the input output voltage levels need to be translated. This translation is a relatively simple task. Since these levels are referenced off of the most positive rail, V_{CC}, the following equation can be used to calculate the various specified DC levels for a PECL device:

PECL Level = V_{CCNEW} – |Specification Level|

As an example, the V_{OHMAX} level for a 10H device operating with a V_{CC} of 5.0V at 25°C would be as follows:

PECL Level = 5.0V – |–0.81V|
PECL Level = (5.0 – 0.81)V = 4.19V

The same procedure can be followed to calculate all of the DC levels, including V_{BB} for any ECL device. Table 2 at the bottom of the page outlines the various PECL levels for a V_{CC} of 5.0V for both the 10H and 100K ECL standards. As mentioned earlier any changes in V_{CC} will show up 1:1 on the output DC levels. Therefore any tolerance values for V_{CC} can be transferred to the device I/0 levels by simply adding or subtracting the V_{CC} tolerance values from those values provided in Table 2.

PECL Termination Schemes

PECL outputs can be terminated in all of the same ways standard ECL, this would be expected since an ECL and a PECL device are one in the same. Figure 3 illustrates the various output termination schemes utilized in typical ECL systems. For best performance the open line technique in Figure 3 would not be used except for very short interconnect between devices; the definition of short can be found in the various design guides for the different ECL families. In general for the fastest performance and the ability to drive distributive loads the parallel termination techniques are the best choice. However occasions may arise where a long uncontrolled or variable impedance line may need to be driven; in this case the series termination technique would be appropriate. For a more thorough discourse on when and where to use the various termination techniques the reader is referred to the MECL System Design Handbook (HB205/D) and the design guide in the ECLinPS Databook (DL140/D). The parallel termination scheme of Figure 3 requires an extra V_{TT} power supply for the impedance matching load resistor. In a system which is built mainly in CMOS/TTL this extra power supply requirement may prohibit the use of this technique. The other schemes of Figure 3 use only the existing positive supply and ground and thus may be more attractive for the CMOS/ TTL based machine.

Parallel Termination Schemes

Because the techniques using an extra V_{TT} power supply consume significantly less power, as the number of PECL devices incorporated in the design increases the more attractive the V_{TT} supply termination scheme becomes. Typically ECL is specified driving 50Ω into a –2.0V, therefore for PECL with a V_{CC} supply different than ground the V_{TT} terminating voltage will be V_{CC} – 2.0V. Ideally the V_{TT} supply would track 1:1 with V_{CC}, however in theory this scenario is highly unlikely. To ensure proper operation of a PECL device within the system the tolerances of the V_{TT} and the V_{CC} supplies should be considered. Assume for instance that the nominal case is for a 50Ω load (R_t) into a +3.0V supply; for a 10H compatible device with a V_{OHmax} of –0.81V and a realistic V_{OLmin} of –1 .85V the following can be derived:

$I_{OHmax} = (V_{OHmax} - V_{TT})/R_t$
$I_{OHmax} = (\{5.0 - 0.81\} - 3.0)/50 = 23.8mA$
$I_{OLmin} = (V_{OLmin} - V_{TT})/R_t$
$I_{OLmin} = (\{5.0 - 0.81\} - 3.0)/50 = 3.0mA$

If +5% supplies are assumed a V_{CC} of V_{CCnom} –5% and a V_{TT} of V_{TTnom} +5% will represent the worst case. Under these conditions, the following output currents will result:

$I_{OHmax} = (\{4.75 - 0.81\} - 3.15)/50 = 15.8mA$
$I_{OLmin} = (\{4.75 - 1.85\} - 3.15)/50 = 0mA$

Using the other extremes for the supply voltages yields:

$I_{OHmax} = 31.8mA$
$I_{OLmin} = 11mA$

Table 2. ECL/PECL DC Level Conversion for V_{CC} = 5.0V

	10E Characteristics						100E Characteristics		
	0°C		25°C		85°C		0 to 85°C		
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
V_{OH}	–1.02/3.98	–0.84/4.16	–0.98/4.02	–0.81/4.19	–0.92/4.08	–0.735/4.265	–1.025/3.975	–0.880/4.120	V
V_{OL}	–1.95/3.05	–1.63/3.37	–1.95/3.05	–1.63/3.37	–1.95/3.05	–1.600/3.400	–1.810/3.190	–1.620/3.380	V
V_{OHA}	—	—	—	—	—	—	—	–1.610/3.390	V
V_{OLA}	—	—	—	—	—	—	–1.035/3.965	—	V
V_{IH}	–1.17/3.83	–0.84/4.16	–1.13/3.87	–0.81/4.19	–1.07/3.93	–0.735/4.265	–1.165/3.835	–0.880/4.120	V
V_{IL}	–1.95/3.05	–1.48/3.52	–1.95/3.05	–1.48/3.52	–1.95/3.05	–1.450/3.550	–1.810/3.190	–1.475/3.525	V
V_{BB}	–1.38/3.62	–1.27/3.73	–1.35/3.65	–1.25/3.75	–1.31/3.69	–1.190/3.810	–1.380/3.620	–1.260/3.740	V

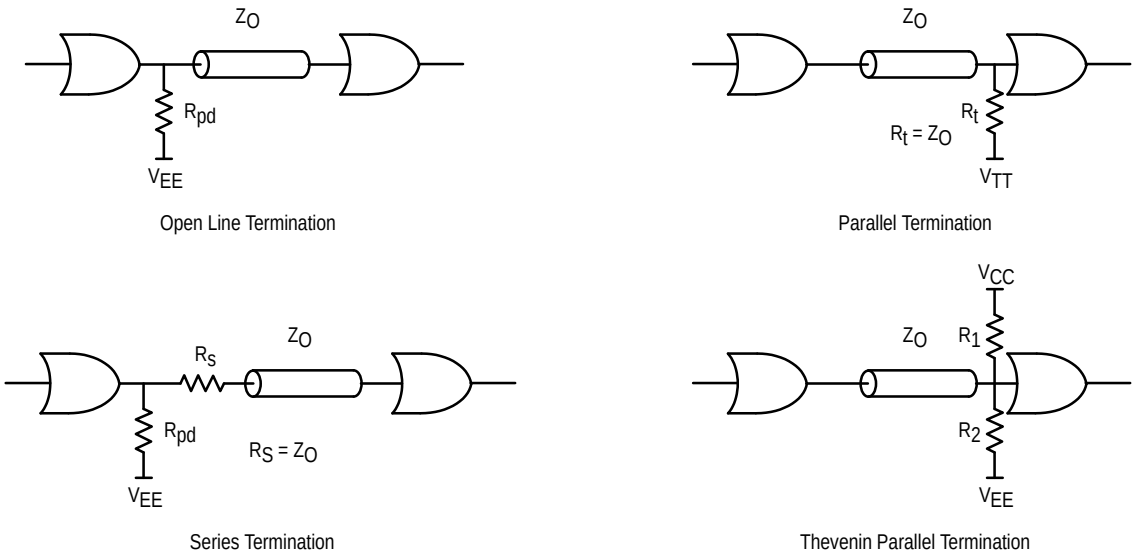


Figure 3. Termination Techniques for ECL/PECL Devices

The changes in the I_{OH} currents will affect the DC V_{OH} levels by ≈±40mV at the two extremes. However in the vast majority of cases the DC levels for ECL devices are well centered in their specification windows, thus this variation will simply move the level within the valid specification window and no loss of worst case noise margin will be seen. The I_{OL} situation on the other hand does pose a potential AC problem. In the worst case situation the output emitter follower could move into the cutoff state. The output emitter followers of ECL devices are designed to be in the conducting "on" state at all times. If cutoff, the delay of the device will be increased due to the extra time required to pull the output emitter follower out of the cutoff state. Again this situation will arise only under a number of simultaneous worst case situations and therefore is highly unlikely to occur, but because of the potential it should not be overlooked.

Thevenin Equivalent Termination Schemes

The Thevenin equivalent parallel termination technique of Figure 3 is likely the most attractive scheme for the CMOS/TTL designer who is using a small amount of ECL. As mentioned earlier this technique will consume more power, however the absence of an additional power supply will more than compensate for the extra power consumption. In addition, this extra power is consumed entirely in the external resistors and thus will not affect the reliability of the IC. As is the case with standard parallel termination, the tolerances of the V_{TT} and V_{CC} supplies should be addressed in the design phase. The following equations provide a means of determining the two resistor values and the resulting equivalent V_{TT} terminating voltage.

$$R1 = R2\ (\{V_{CC} - V_{TT}\}/\{V_{TT} - V_{EE}\})$$
$$R2 = Z_O\ (\{V_{CC} - V_{EE}\}/\{V_{CC} - V_{TT}\})$$
$$V_{TT} = V_{CC}\ (R2/\{R1 + R2\})$$

For the typical setup:

V_{CC} = 5.0V; V_{EE} = GND; V_{TT} = 3.0V; and Z_O = 50Ω

R2 = 50 ({5 – 0}/{5–3}) = 125Ω
R1 = 125 ({5–3}/{3–0}) = 83.3Ω

checking for V_{TT}

V_{TT} = 5 (125/{125 – 83.3}) = 3.0V

Because of the resistor divider network used to generate V_{TT} the variation in V will be intimately tied to the variation in V_{CC}. Differentiating the equation for V_{TT} with respect to V_{CC} yields:

$$dV_{TT}/dV_{CC} = R2/(R1 + R2)\ dV_{CC}$$

Again for the nominal case this equation reduces to:

$$\Delta V_{TT} = 0.6\ \Delta V_{CC}$$

So that for ΔV_{CC} = ±5% = ±0.25V, ΔV_{TT} = ±0.15V.

As mentioned previously the real potential for problems will be if the V_{OL} level can potentially put the output emitter follower into cutoff. Because of the relationship between the V_{CC} and V_{TT} levels the only situation which could present a problem will be for the lowest value of V_{CC}. Applying the equation for I_{OLmin} under this condition yields:

$$I_{OLmin} = (\{V_{OLmin} - V_{TT}\}/R_t$$
$$I_{OLmin} = (\{4.75 - 1.85\} - 2.85)/50 = 1.0mA$$

From this analysis it appears that there is no potential for the output emitter follower to be cutoff. This would suggest that the Thevenin equivalent termination scheme is actually a better design to compensate for changes in V_{CC} due to the fact that these changes will affect V_{TT}, although not 1:1 as would be ideal, in the same way. To make the design even more immune to potential output emitter follower cutoff the designer can design for nominal operation for the worst case situation. Since the designer has the flexibility of choosing the V_{TT} level via the selection of the R1 and R2 resistors the following procedure can be followed.

Let V_{CC} = 4.75V and $V_{TT} = V_{CC} – 2.0V = 2.75V$
Therefore:

R2 = 119Ω and R1 = 86Ω thus:
I_{OHmax} = 23mA and I_{OLmin} = 3.0mA

Plugging in these values for the equations at the other extreme for V_{CC} = 5.25V yields:

V_{TT} = 3.05V, I_{OHmax} = 28mA and I_{OLmin} = 5.2mA

Although the output currents are slightly higher than nominal, the potential for performance degradation is much less and the results of any degradation present will be significantly less dramatic than would be the case when the output emitter follower is cutoff. Again in most cases the component manufactures will provide devices with typical output levels; typical levels significantly reduces any chance of problems. However it is important that the system designer is aware of where any potential problems may come from so they can be dealt with during the initial design.

Differential ECL Termination

Differential ECL outputs can be terminated using two different strategies. The first strategy is to simply treat the complimentary outputs as independent lines and terminate them as previously discussed. For simple interconnect between devices on a single board or short distances across the backplane this is the most common method used. For interconnect across larger distances or where a controlled impedance backplane is not available the differential outputs can be distributed via twisted pair of ribbon cable (use of ribbon cable assumes every other wire is a ground so that a characteristics impedance will arise). Figure 4 illustrates common termination techniques for twisted pair/ribbon cable applications. Notice that Thevenin equivalent termination techniques can be extended to twisted pair and ribbon cable applications as pictured in Figure 4. However for twisted pair/ribbon cable applications the standard termination technique picture in Figure 4 is somewhat simpler and also does not require a separate termination voltage supply. If however the Thevenin techniques are necessary for a particular application the following equations can be used:

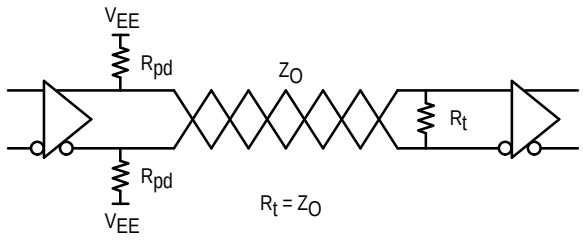
$R1 + R2 = Z_O/2$
$R3 = R1\ (V_{TT} – V_{EE})/(V_{OH} + V_{OL} – 2V_{TT})$
$V_{TT} = (R3\{V_{OH} + V_{OL}\} + R1\{V_{EE}\})/(R1 + 2R3)$

where V_{OH}, V_{OL}, V_{EE} and V_{TT} are PECL voltage levels.

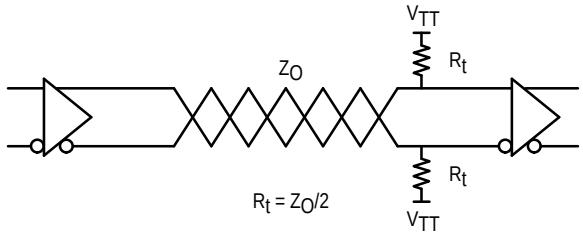
Plugging in the various values for V_{CC} will show that the V_{TT} tracks with V_{CC} at a rate of approximately 0.7:1. Although this rate is approaching ideal it would still behoove the system designer to ensure there are no potential situations where the output emitter follower could become cutoff. The calculations are similar to those performed previously and will not be repeated.

Noise and Power Supply Distribution

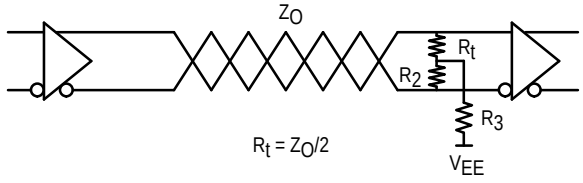
Since ECL devices are top rail referenced it is imperative that the V_{CC} rail be kept as noise free and variation free as possible. To minimize the V_{CC} noise of a system liberal bypassing techniques should be employed. Placing a bypass capacitor of 0.01μF to 0.1μF on the V_{CC} pin of every device will help to ensure a noise free V_{CC} supply. In addition when using PECL in a system populated heavily with CMOS and TTL logic the two power supply planes should be isolated as much as possible. This technique will help to keep the large current spike noise typically seen in CMOS and TTL drivers from coupling into the ECL devices. The ideal situation would be multiple power planes; two dedicated to the PECL V_{CC} and ground and the other two to the CMOS/TTL V_{CC} and ground. However if these extra planes are not feasible due to board cost or board thickness constraints common planes with divided subplanes can be used (Figure 5). In either case the planes or sub planes should be connected to the system power via separate paths. Use of separate pins of the board connectors is one example of connecting to the system supplies.



Standard Twisted Pair Termination



Parallel Twisted Pair Termination



Thevenin Twisted Pair Termination

Figure 4. Twisted Pair Termination Techniques

For single supply translators or dual supply translators which share common power pins the package pins should be connected to the ECL V_{CC} and ground planes to ensure the noise introduced to the part through the power plane is minimal. For translating devices with separate TTL and ECL

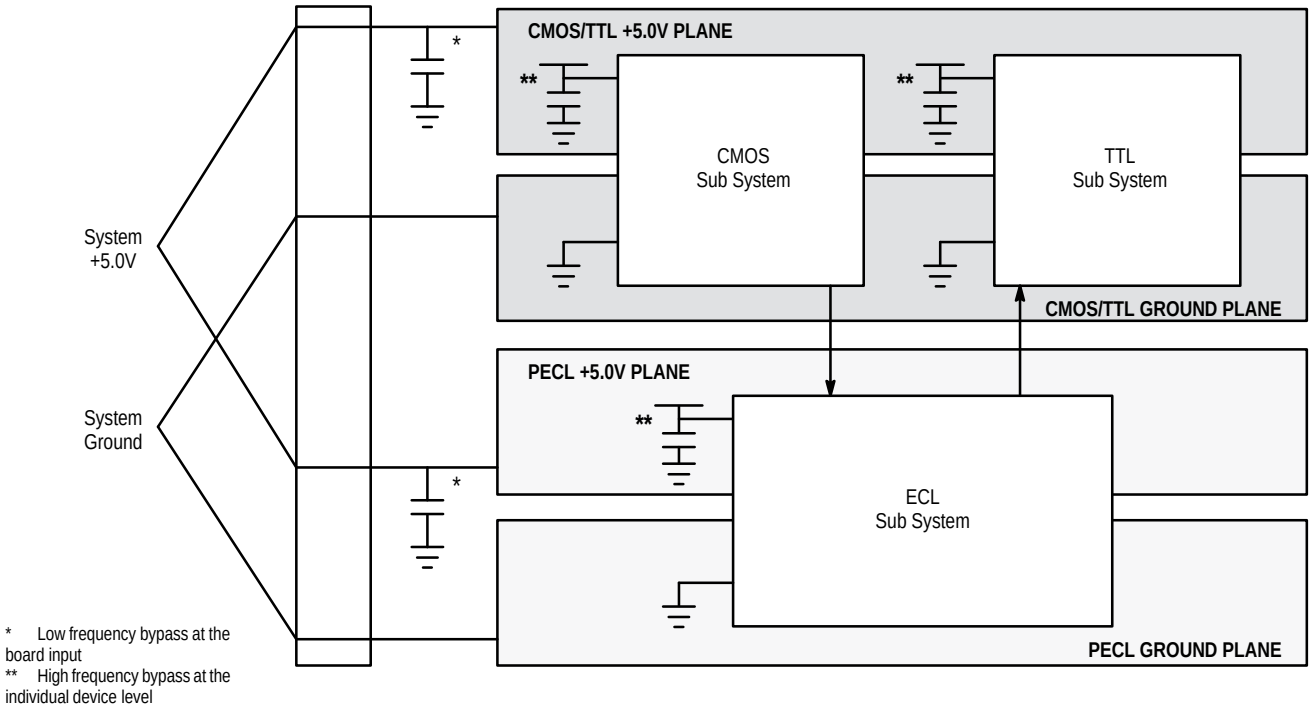


Figure 5. Power Plane Isolation in Mixed Logic Systems

power supply pins, the pins should be tied to the appropriate power planes.

Another concern is the interconnect between two cards with separate connections to the V_{CC} supply. If the two boards are at the opposite extremes of the V_{CC} tolerance, with the driver being at the higher limit and the receiver at the lower limit, there is potential for soft saturation of the receiver input. Soft saturation will manifest itself as degradation in AC performance. Although this scenario is unlikely, again the potential should be examined. For situations where this potential exists there are devices available which are less susceptible to the saturation problem. This variation in V_{CC} between boards will also lead to variations in the input switching references. This variation will lead to switching references which are not ideally centered in the input swing and cause rise/fall skew within the receiving device. Obviously the later skew problem can be eliminated by employing differential interconnect between boards.

When using PECL to drive signals across a backplane, situations may arise where the driver and the receiver are on different power supplies. A potential problem exists if the receiver is powered down independent of the driver. Figure 6 (on the following page) represents a generic driver/receiver pair. From Figure 6, one can see if the receiver is powered down and presents a path to ground through its V_{CC} pin while the driver is still powered at +5.0V the base/collector junction of the input transistor of the receiver will be forward biased and conduct current. Although the collector load resistor will limit the current in the situation of Figure 6, the current may still be enough to damage the junction or exceed the current handling capability of the base electrode metal stripe. Either of these situations could lead to degradation of the reliability of the devices. Because different devices have different ESD protection schemes, and input architectures, the extent of the potential problem will vary from device to device.

Another issue that arises in driving backplanes is situations where the input signals to the receiver are lost and present an open input condition. Many differential input devices will become unstable in this situation, however, most of the newer designs, and some of the older designs, incorporate internal clamp circuitry to guarantee stable outputs under open input conditions. All of the ECLinPS (except for the E111), ECLinPS Lite, and H600 devices, along with the MC10125, 10H125 and 10114 will maintain stable outputs under open input conditions.

Conclusion

The use of ECL logic has always been surrounded by clouds of misinformation; none of those clouds have been thicker than the one concerning PECL. By breaking through this cloud of misinformation the traditional CMOS/TTL designers can approach system problems armed with a complete set of tools. For areas within their designs which require very high speed, the driving of long, low impedance lines or the distribution of very low skew clocks, designers can take advantage of the built in features of ECL. By incorporating this ECL logic using PECL methodologies this inclusion need not require the addition of more power supplies to unnecessarily drive up the cost of their systems. By following the simple guidelines presented here CMOS/TTL designers can truly optimize their designs by utilizing ECL logic in areas in which they are ideally suited. Thus bringing to market products which offer the ultimate in performance at the lowest possible cost.

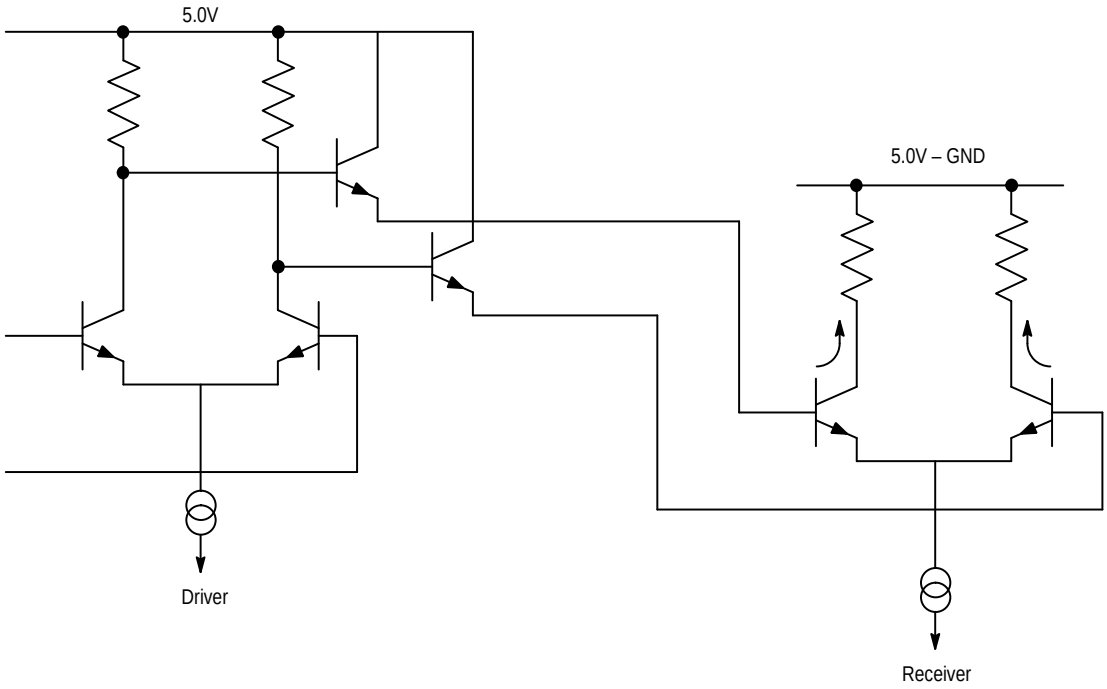


Figure 6. Generic Driver/Receiver Pair

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