APPLICATION NOTE

AN140

Compensation techniques for use with the NE/SE5539

Author: Tom DeLurio

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NE5539 DESCRIPTION

The Philips Semiconductors NE/SE5539 ultra-high frequency operational amplifier is one of the fastest monolithic amplifiers made today. With a unity gain bandwidth of 350MHz and a slew rate of 600V/µs, it is second to none. Therefore, it is understandable that to attain this speed, standard internal compensation would have to be left out of its design. As a consequence, the op amp is not unconditionally stable for all closed-loop gains and must be externally compensated for gains below 17dB. Properly done, compensation need not limit slew rate. The following will explain how to use the methods available with the NE/SE5539.

LEAD AND LAG-LEAD COMPENSATION

A useful method for compensating the device for closed-loop gains below seven is to use lag-lead and lead networks as shown in Figure 1. The lead network is primarily concerned with compensating for loss of phase margin caused by distributed board capacitance and input capacitance, while lag-lead is mainly for optimizing transient response. Lead compensation modifies the feedback network and adds a zero to the overall transfer function. This increases the phase, but does not greatly change the gain magnitude. This zero improves the phase margin.

To determine components, it can be shown that the optimal conditions for amplifier stability occur when:

$$(R1)\ (C_{DIST}) = (R_F)\ (C_{LEAD}) \quad (1)$$

However, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed-loop amplifier will be reduced. Based on using a double-sided copper-clad printed circuit board with a distributed capacitance of 3.5pF and a unity gain configuration, C_{LEAD} would be 3.5pF. Another way of stating the relationship between the distributed capacitance closed-loop gain and the lead compensation capacitor is:

$$C_{LEAD} = C_{DIST}\ \frac{R1}{R_F} \quad (2)$$

When bandwidth is of primary concern, the lead compensation will usually be adequate. For closed-loop gains less than seven, lag-lead compensation is necessary for stability.

If transient response is also a factor in design, a lag-lead compensation network may be necessary (Reference Figure 1). For practical applications, the following equations can be used to determine proper lag-lead components:

$$\frac{R_F}{R1/R_{LAG}} \geq 7 \quad (3)$$

Therefore,

$$R_{LAG} \leq \frac{R_F}{7 - R_F/R1} \quad (4)$$

Using the above equation will insure a closed-loop gain of seven above the network break frequency. C_{LAG} may now be approximated using:

$$W_{LAG} \simeq \frac{2\pi\ (GBW)}{10}\ Rad/Sec \quad (5)$$

$$W_{LAG} = \frac{\pi\ (GBW)}{5}\ Rad/Sec \quad (6)$$

where

$$W_{LAG} = \frac{1}{(R_{LAG})\ (C_{LAG})} \quad (7)$$

therefore,

$$\frac{\pi\ (GBW)}{5} = \frac{1}{(R_{LAG})\ (C_{LAG)}} \quad (8)$$

and

$$C_{LAG} = \frac{5}{\pi\ R_{LAG}\ (GBW)} \quad (9)$$

This method adds a pole and zero to the transfer function of the device, causing the actual open-loop gain and phase curve to be reshaped, thus creating a progressive improvement above the critical frequency where phase changes rapidly. (Near 70MHz, see Figures 2a and 2b.) But also, the lag-lead network can be adjusted to optimize gain peaking for transient responses. Therefore, rise time, overshoot, and settling time can be changed for various closed-loop gains. The result of using this technique is shown for a pulse amplifier in Figure 3.

USING PIN 12 COMPENSATION

An alternate method of external compensation is obtained by use of the NE/SE5539 frequency compensation pin. The circuits in Figure 4 show the correct way to use this pin. As can be seen, this method saves the use of one capacitor as compared to standard lag-lead and lead compensation as shown in Figure 1.

But, most importantly, both methods are equally effective; i.e., a good wide-band amplifier below 17dB, with control over ringing and overshoot. For example, inverting and non-inverting amplifier circuits using Pin 12 are shown in Figure 5. The corresponding pulse response for each circuit is shown in Figures 6 and 7 for the network values recommended. As shown by the response photos, the overshoot and settling time can be controlled by adjusting R_C and C_C. In damping the overshoot, rise time is slightly decreased. Also, the non-inverting configuration (Figure 6) gives a very fast response time compared to the inverting mode.

If it is important to reduce output offset voltage and noise, an additional capacitor, C_O, can be added in series with the resistor (R_C) across the inputs. This should be a large value to block DC but not affect the benefits of the compensation components at high frequencies. A value of 0.01µF as shown in Figure 8 is sufficient.

INTERNAL CHARACTERISTICS OF THE NE/SE5539

In order to better understand the compensation procedure, a detailed discussion of the amplifier follows.

The complete amplifier schematic is shown in Figure 9. To clarify the effect of the compensation pin, the schematic is split into five main parts as shown in Figure 10.

Each segment in Figure 10 is defined as follows: starting from the non-inverting input, Section A_1 is the amplification from the input to the base of transistor Q_4. A_2 is from the base of Q_4 to the summation point at the collector of Q_3. Furthermore, A_3 represents the gain from the non-inverting input to the summation point via the common emitter side of Q_2 and Q_3. Finally, B_F is the feedback factor of the positive feedback loop from the collector of Q_3 to the base of Q_4.

From Figure 10, it can be seen that the total gain (A_T) is:

$$A_T = \frac{A_1 A_2}{1 - (B_F A_2)} \qquad A_3 (1 \qquad B_F A_2)$$

Each term in this equation plays a role at different frequencies to determine the total transfer function of the device. Of particular importance is the pole in A_3 (near 340MHz) which causes a roll-off of 12dB/octave and loss of phase margin just before unity gain. This can be seen in the Bode plot in Figure 11a. To overcome this pole, a capacitor and resistor are connected as shown in Figures 12a and 12b. The compensation pin is connected to the emitter of Q_5, which is in an emitter-follower configuration. Therefore, a reactance connected to Pin 12 acts essentially as if it were connected at the base of Q_5. Since the capacitor is connected here, it is now a component of B_F and a zero is added to the transfer function. The resistor across the input pins controls overall gain and causes A_T to cross 0dB at a lower frequency; the capacitor in the feedback loop controls phase shift and gain peaking.

To further explain, Bode plots of open-loop response using varying capacitor values and corresponding pulse responses are shown in Figures 13a through 13f. The changes in gain and phase can readily be seen, as is the effect on bandwidth.

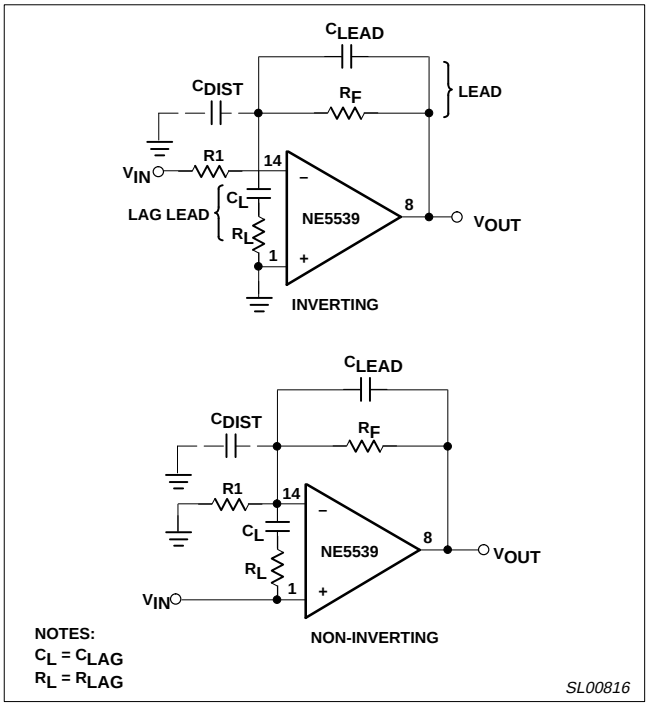
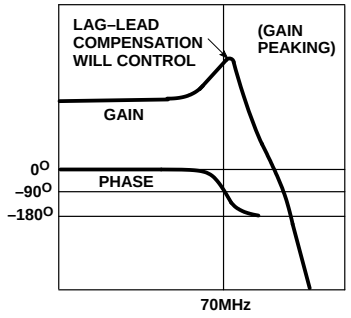
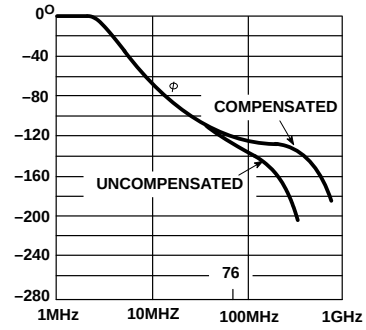


Figure 1. Standard Lag-Lead Compensation



a. Closed-Loop Inverting Gain of Seven Gain-Phase Response (Uncompensated)



b. Open-Loop Phase

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Figure 2.

COMPUTER ANALYSIS

The open-loop and pulse response plots were generated using an IBM 370 computer and SPICE, a general-purpose circuit simulation program. Each transistor in the part is mathematically modeled after actual device parameters, which were measured in the laboratory. These models are then combined with the resistors and voltage sources through node numbers so that the computer knows where each is connected.

To indicate the accuracy of this system, the actual open-loop gain is compared to the computer plots in Figures 14 and 15. The real payoff for this system is that once a credible simulation is achieved, any outside circuit can be modeled around the op amp. This would be used to check for feasibility before breadboarding in the lab. The internal circuit can be treated like a black box and the outside circuit program altered to whatever application the user would like to examine.

1. J. Millman and C. C. Halkias: Integrated Electronics: Analog and Digital Circuits and Systems, McGraw-Hill Book Company, New York, 1972.

2. A. Vladimirescu, Kaihe Zhang, A. R. Newton, D. O. Peterson, A. Sanquiovanni-Vincentelli: “Spice Version 2G,” University of California, Berkeley, California, August 10, 1981.

3. Philips Semiconductors: Analog Data Manual 1983, Philips Semiconductors Corporation, Sunnyvale, California 1983.

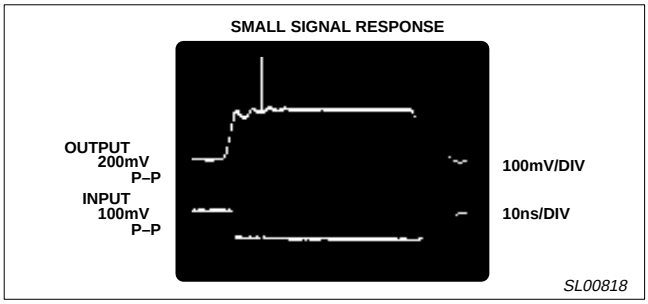


Figure 3. Compensated Pulse Response

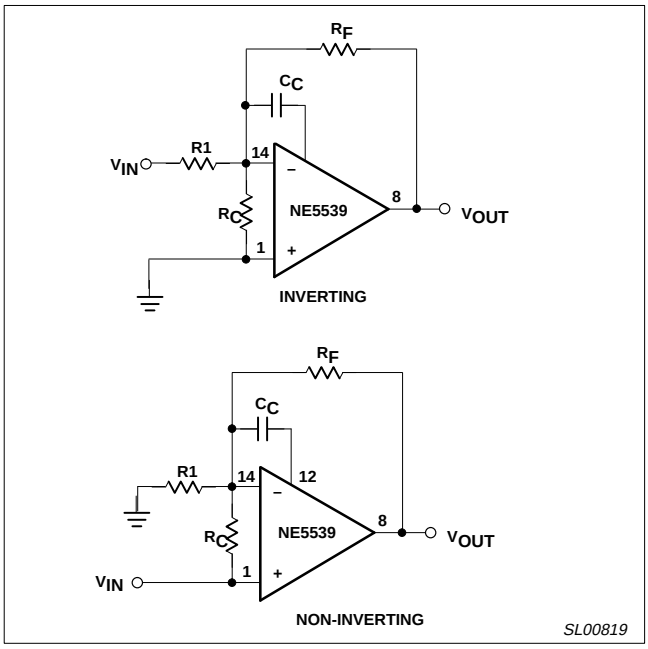


Figure 4. Pin 12 Compensation

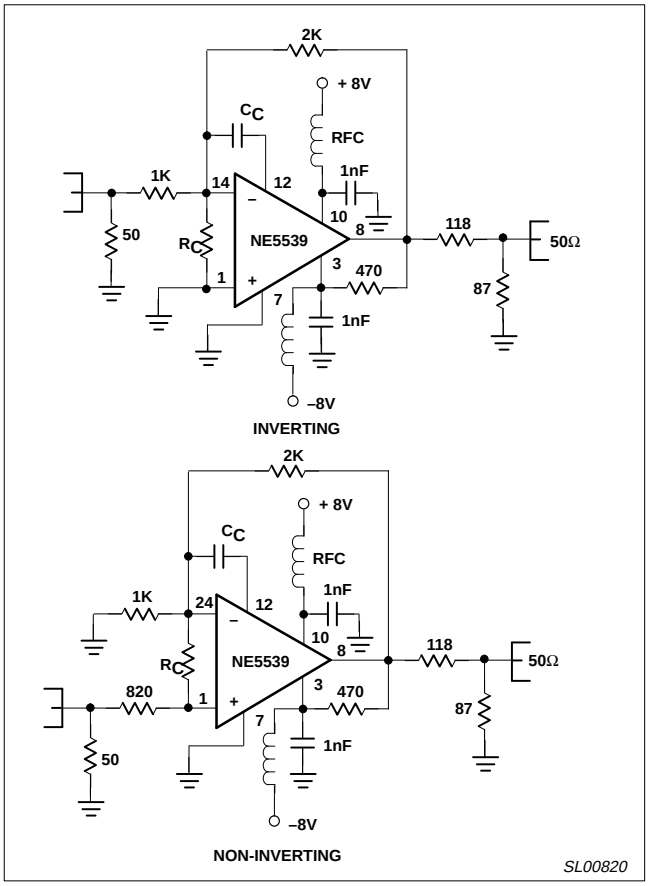


Figure 5. Pulse Response Test Circuits

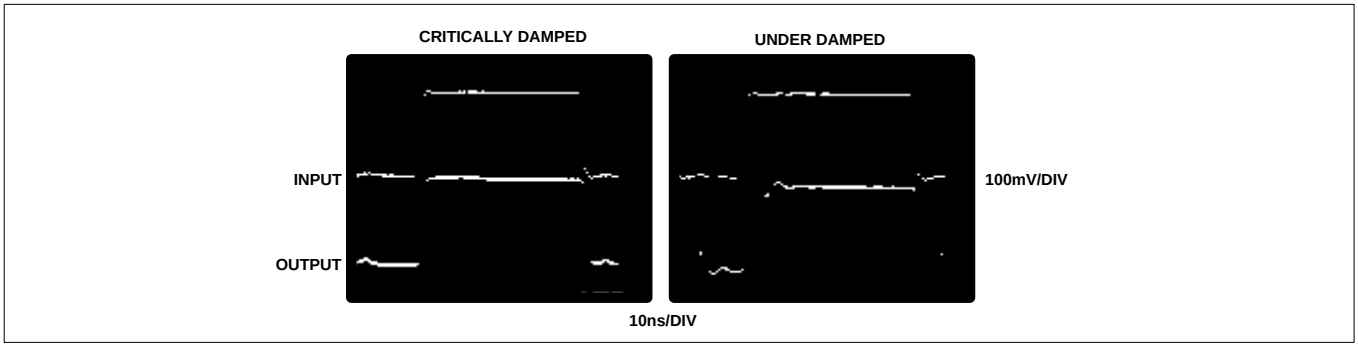


Figure 6. Small Signal Response – Non-Inverting

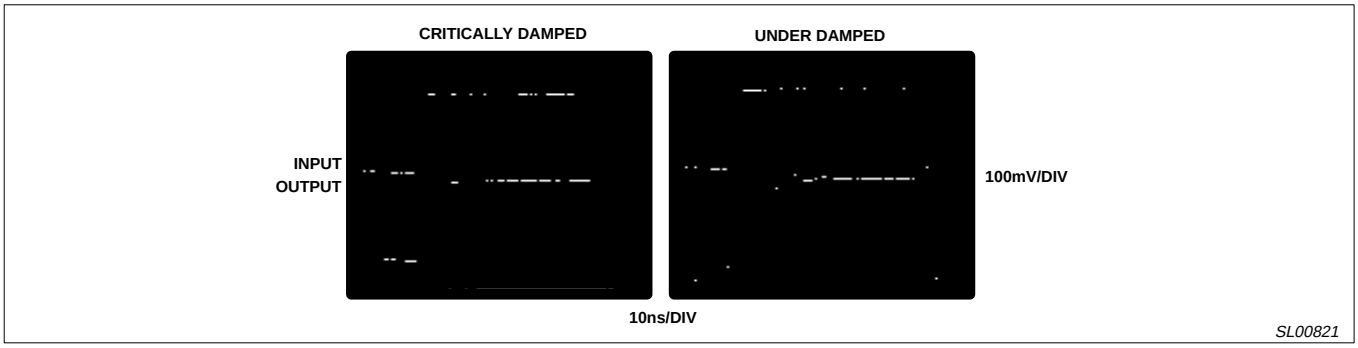


Figure 7. Small Signal Response – Inverting

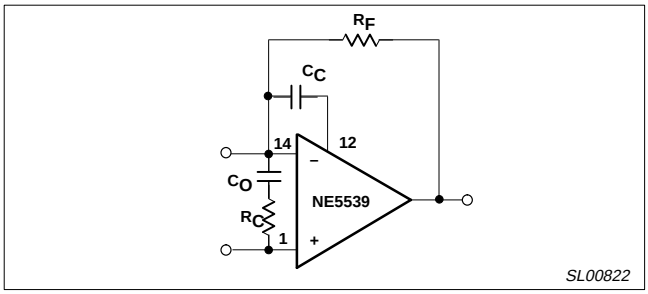


Figure 8. C_O Will Reduce Output Offset and Noise

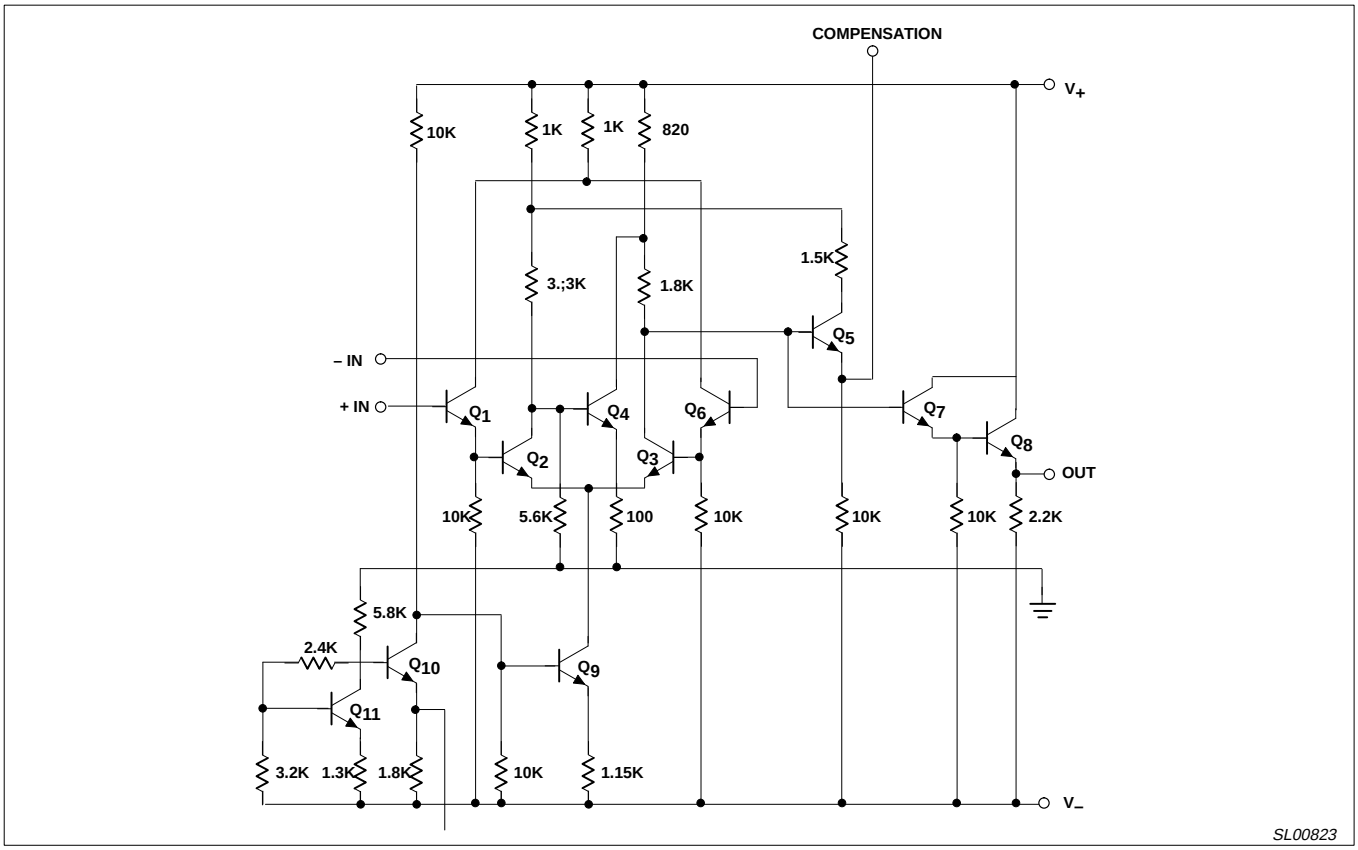


Figure 9. Complete Schematic of NE/SE5539

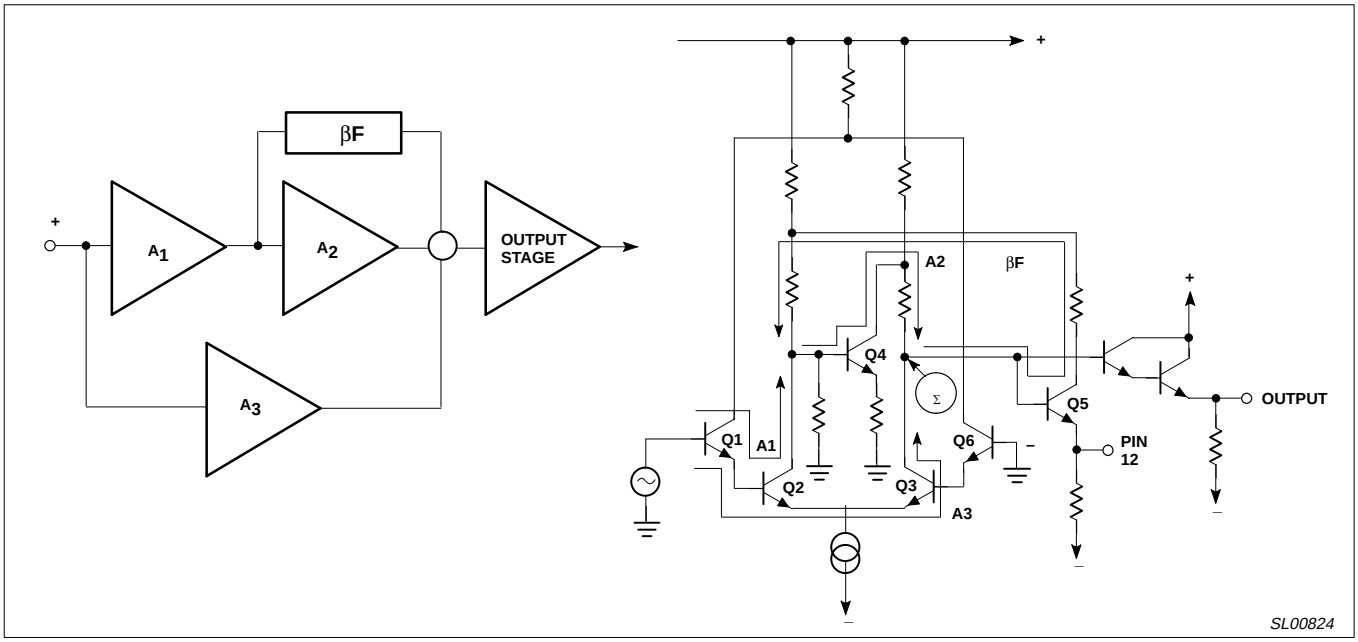
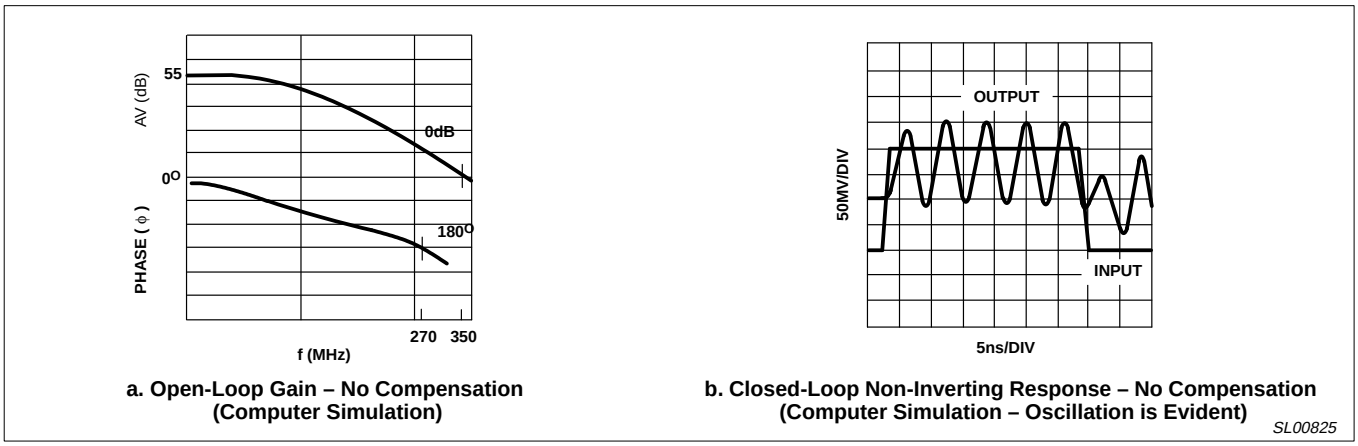


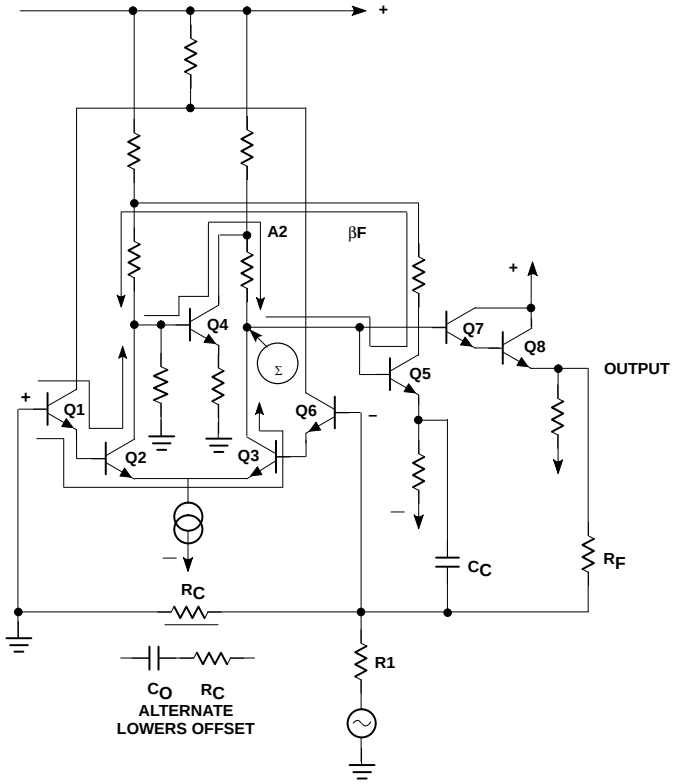
Figure 10. Internal Sections



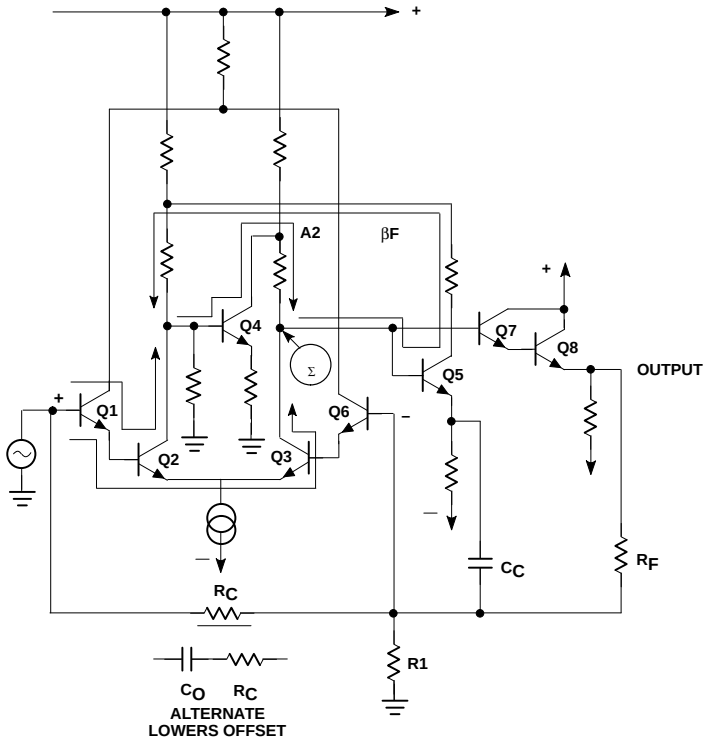
a. Open-Loop Gain – No Compensation (Computer Simulation)

b. Closed-Loop Non-Inverting Response – No Compensation (Computer Simulation – Oscillation is Evident)

Figure 11.



a. Pin 12 Compensation Showing Internal Connections – Inverting



b. Pin 12 Compensation Showing Internal Connections – Non-Inverting

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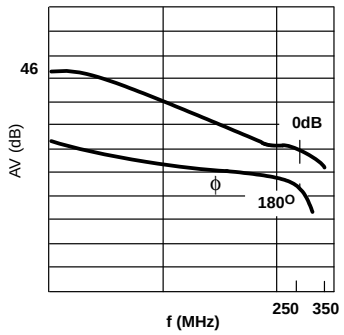
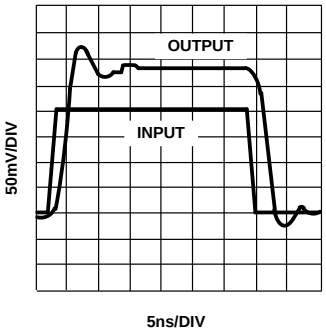
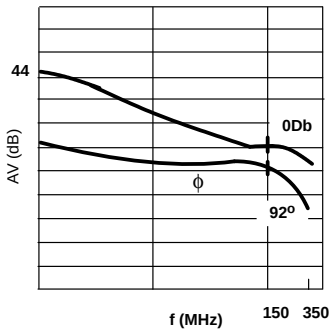
Figure 12.



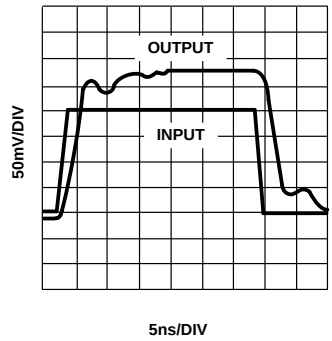
a. Open-Loop Pin 12 Compensation – R_C = 200Ω, C_C = 1pF, (Computer Simulation)



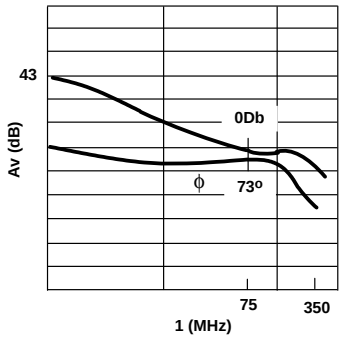
b. Closed-Loop Non-Inverting Pulse Response – R_C = 200Ω, C_C = 1pF, A_V = 3 (Computer Simulation – Underdamped)



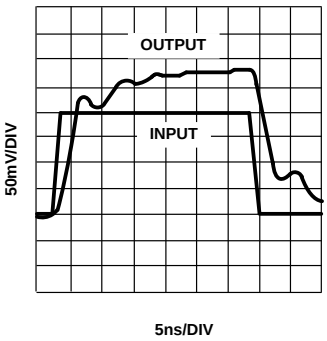
c. Open-Loop Pin 12 Compensation – R_C = 200Ω, C_C = 2pF (Computer Simulation)



d. Closed-Loop Non-Inverting Pulse Response – R_C = 200Ω, C_C = 2pF, A_V = 3 (Computer Simulation – Critically-Damped)



e. Open-Loop Pin 12 Compensation – R_C = 200Ω, C_C = 3pF, (Computer Simulation)



f. Closed-Loop Pulse Response – R_C = 200Ω, C_C = 3pF, A_V = 3 (Computer Simulation – Overdamped)

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Figure 13.

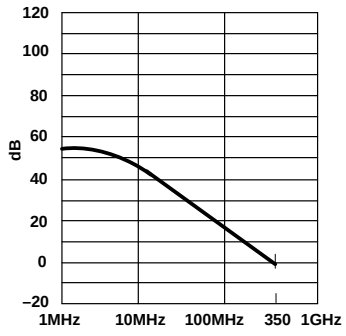

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Figure 14. Actual Open–Loop Gain Measured in Lab

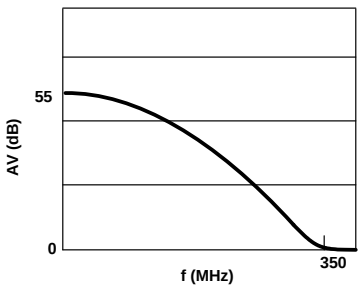

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Figure 15. Computer–Generated Open–Loop Gain