AN1265

Configuring the MPC2604GA Integrated L2 Cache with the MPC106

For a 256Kbyte L2 Cache

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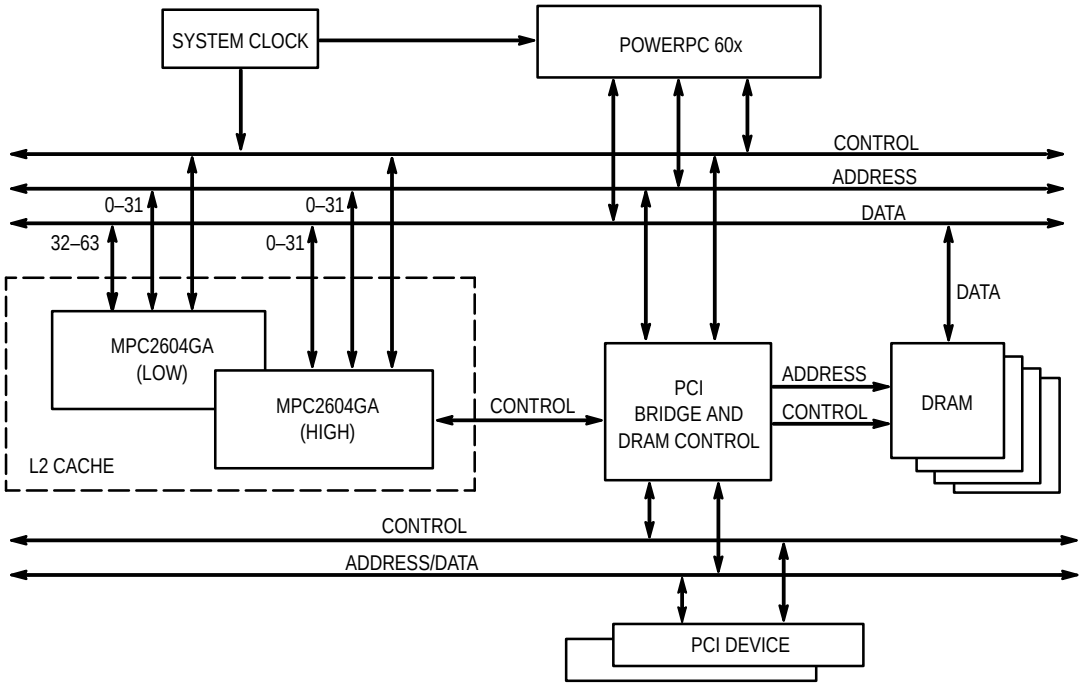
L2 cache is fast becoming a requirement for all computers, especially for RISC architectures such as the PowerPC™ family of microprocessors. Adding L2 cache to the system is one of the easiest ways to significantly increase the performance of the processor. Several factors contribute to the need for L2 cache: faster processor speeds that are multiples of the system bus frequencies so that an L1 miss results in several processor wait cycles while data are retrieved from main memory; larger applications with code or data that does not fit in the L1 cache; and larger penalties for going to main memory due to greater speed differences between DRAM main memory and SRAM L2 cache.

So, what is the best L2 cache design? Optimally, it would be one that never misses a processor read request, and one that can provide data as fast as the processor can handle it. This is not possible, realistically (at a reasonable cost, at least). However, a close approximation is possible with a good design. The MPC2604GA is an integrated secondary cache for PowerPC microprocessor based designs and has all the features that an optimally designed L2 cache should have. The MPC2604GA is the fastest L2 cache available for the PowerPC 60X bus. Due to its integration of logic, tag, and data on the same silicon, it can respond to a read hit with a 2–1–1–1 burst at 66MHz. This alone is a 17% read hit performance improvement over a 3–1–1–1 L2 cache. The MPC2604GA can also provide subsequent bursts as fast as 1–1–1–1. It is also a copy–back (write–back) design meaning that it will shorten a processor write to the speed of the L2 instead of the speed of main memory. Additionally, it is four way set associative which significantly increases the odds of a read hit over an equivalent sized direct mapped cache. The set associativity also decreases the odds of thrashing, a scenario in which the cache is constantly being rewritten from main memory because different main memory addresses are mapped to the same cache address.

SYSTEM BLOCK DIAGRAM



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MOTOROLA

CONNECTING THE MPC2604GA TO THE MPC106

The MPC2604GA is designed to work in conjunction with the Motorola MPC106 PCI Bridge/Memory controller. The following describes a two–chip MPC2604GA solution (256K bytes) in conjunction with a MPC106 chip and a single PowerPC processor. The MPC2604GA is configured for 2–1–1–1 mode.

Since the data bus on the MPC2604GA is 36 bits wide, the processor data bus is split into two for a 72 bit bus. The chip that receives the upper half is called the high chip, and the chip that receives the lower half is called the low chip. To configure this correctly, the CFG0 on the high chip must be tied high and tied low on the low chip. The CFG4 pin must be tied high on both chips. All other CFG pins on both chips are tied low.

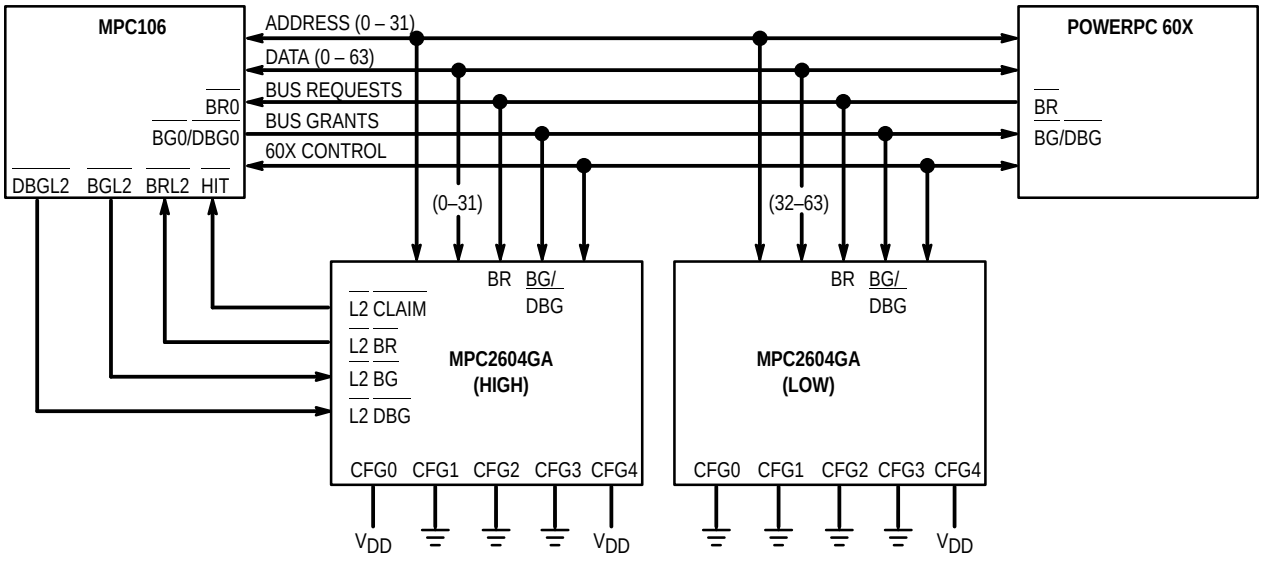
For the address lines, all 32 bits must be tied to both chips.

For the data lines, the upper 32 bits are tied to the high chip. The lower 32 bits go to the low chip in a similar way. For example, D63 on the processor bus is tied to D31 on the MPC2604GA.

Certain control lines are tied between the MPC106 and the high MPC2604GA chip. HIT, on the MPC106, is tied to L2 CLAIM on the MPC2604GA; BRL2 to L2 BR; BGL2 to L2 BG; and DBGL2 to L2 DBG.

The 60x control lines that must go to the MPC2604GA chips include: TS, TT0–4, TSIZ0–2, TBST, CI, WT, GBL, AACK, TA, XATS, ARTRY, SHD, and HRESET. All other input control lines may be tied high, unless other chips in the system use them.

SYSTEM BLOCK DIAGRAM FOR A 256KB MPC2604GA SOLUTION IN 2–1–1–1 MODE



SPECIAL CASES

1. If there is ROM present on the processor bus, then the parity bits should not be connected. The MPC106 uses the parity bits to address the ROM, therefore, they are not used as parity. They can be left open on the MPC2604GA.

2. If the system is using a 603 processor that is running in 1:1 bus mode, then the MPC2604GA must be forced to insert a lead–off wait state. This can be accomplished by tying the CFG3 pin high. CFG3 should otherwise be set low for optimum performance.

CONFIGURATION REGISTER BITS

Certain bits in the processor interface configuration register in the MPC106 have to be set to work with the MPC2604GA:

1. The bit named CF_APHASE_WS must be set low. The bit named CF_LOOP_SNOOP must be set high.
2. If CFG3 is low on the MPC2604GA, then the L2 hit delay bits on the MPC106 must be set to 1. If CFG3 is high, then the L2 hit delay bits must be set to 2.
3. If the system is in Fast L2 mode and CFG3 = 0, then the CF_DPARK must be set to 0.
4. The setting of CF_FAST_L2_MODE should be set to match the processor after a reset. To get into Fast L2 mode on the MPC2604GA, DRTRY must be asserted when HRESET goes high. This is the same procedure used to configure the processor into Fast L2 mode. Note that DBB on the MPC2604GA must be tied high to be in Fast L2 mode.
5. If the system is configured in normal bus mode, and the MPC2604GA is configured for 2–1–1–1 operation, the best performance is achieved by having the MPC106 park the data bus. This can be done by setting CF_APARK and CF_DPARK to 1 and setting CF_BREAD_WS to 0.
6. Since the MPC2604GA has its own cache controller, the controller on the MPC106 must be disabled. This is accomplished by setting bit CF_EXTERNAL_L2 = 1. For a uniprocessor situation, bits CF_L2_MP (1..0) = 10 to indicate a write back cache is being used. Bits CF_L2_SIZE (1..0) should also be set accordingly, 00 for 256K (2 MPC2604GA chips), or 01 for 512K (4 MPC2604GA chips).

The registers L2_CACHE_MISS_INHIBIT, L2_UPDATE_INHIBIT, and CF_FLUSH_L2 in the MPC106 have no effect on the MPC2604GA. To obtain this functionality on the MPC2604GA, they must be generated by some other device.

REFERENCES TO PCI SPACE

System software must insure that cache coherency is maintained for accesses to PCI. Because the MPC2604GA does not distinguish between accesses to PCI and main memory, the processor's WIMG status bits must either (1) inhibit the cache or (2) set the W and M bits to write through mode and coherency is maintained, respectively.

INITIALIZATION

To properly initialize the MPC2604GA, begin clocking with HRESET and TRST low for 16 clock cycles immediately upon power up. The MPC2604GA device will then begin an internal configuration which requires approximately 4096 clock cycles, and is idle during that time. If this is not done, improper device operation may occur.

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