AN1261

Use of 32K x 36 FSRAM in Non–parity Applications

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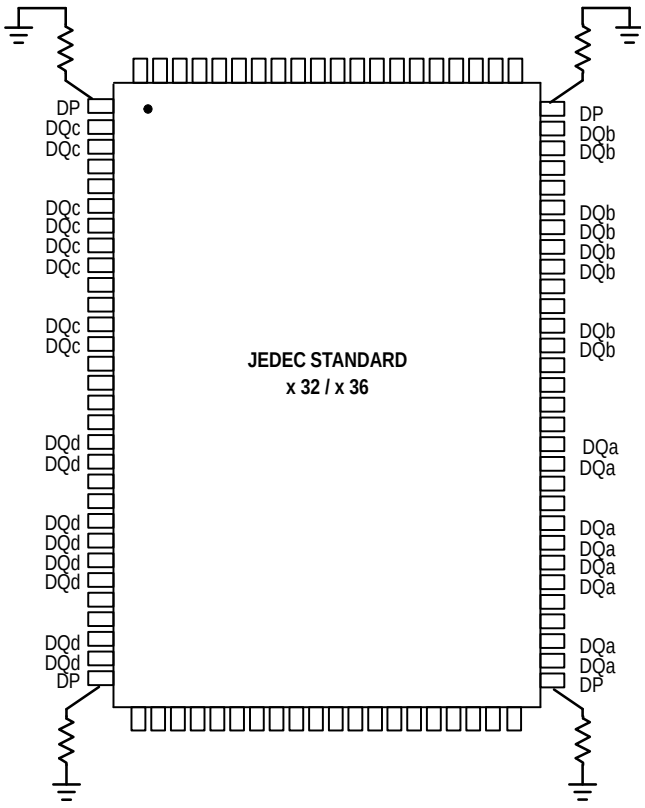
The MCM69F536 and MCM69P536 are synchronous fast static BurstRAMs™ that are organized as 32K words of 36 bits (or four bytes wide) each. The I/O pins contain byte parity. The JEDEC standard pin assignment for synchronous SRAMs defines the corner I/O pins of the 100 pin QFP/TQFP package as either a parity I/O or as a no connect. A RAM organized as 32 bits wide is achieved by making the corner I/O pins no connect.

Motorola's MCM69F536, MCM69P536, and future x36 BurstRAMs can be used in non–parity applications by simply making one of the following two design choices.

1. Connect pulldown (or pullup to 3.3 V V_{CC}) resistors to V_{SS} on the parity I/O pins. The recommended resistor value should be within the 1 kΩ to 10 kΩ range. This is the recommended design choice.

2. Allow the parity I/O pins to be left open circuit. This is not the recommended design choice. One might experience problems associated with floating I/O pins, such as an increase in I_{CC} current.

In general, the use of pulldown/pullup (strap) resistor values closer to 1 kΩ are preferred, since they provide a lower impedance to ac ground (V_{SS} or V_{CC}) and therefore less susceptible to its neighboring pin's noise. The drawback is slightly increased power consumption. However, this additional power is consumed only during the initial read/write cycles after power–up. The array bit pattern upon power–up will be random, so the resistor straps draw current only during read cycles in which the output drives to the opposite state of the strap voltage. During write cycles, the resistor straps insure the parity bits are written with a binary 0 or 1 dependent upon the strap voltage chosen. Subsequent read cycles will return the same binary value that was previously written by the resistor strap. After the entire 32K memory words have been written, no additional power is consumed by the SRAM due to the parity strap resistors.



JEDEC Standard Pin Assignment and Parity Bit Resistors Connected to Ground

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