AN1259

System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

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INTRODUCTION

As the high technology field advances, so do the problems from electromagnetic interference (EMI). EMI issues are increasingly problematic for the system designer as semiconductors in general become faster, more integrated, and, unfortunately, noisier. Engineers who design layouts with little regard for EMI issues are finding that their designs are not performing to specification or are not working at all. However, most EMI issues can be avoided in advance by using an appropriate system design approach coupled with proper printed circuit board (PCB) layout techniques.

Although the information provided here is not a cure-all for every EMI problem, this application note focuses on utilizing proven layout techniques to control EMI on MCU-based mixed-signal systems. It provides a practical approach rather than a theoretical discussion. EMI topics included in this application note are:

- A brief overview of EMI
- General layout guidelines
  - component placement
  - ground layout
  - power system layout and decoupling
  - signal layout
- Noise reduction checklist

For additional reading on electromagnetic interference and compatibility, consult the bibliography of this application note.

EMI OVERVIEW

Noise Definition

Noise is any electrical signal present in a circuit other than the desired signal. This definition does not apply to internal distortion, which is a by-product of non-linearities. A desired signal in one part of a circuit is considered noisy only if it is coupled to a signal from some other part of the circuit. All electrical systems have some noise. This noise is not a problem until it interferes with system performance. Noise sources can be grouped into three different categories:

1) Man-made noise sources — digital electronics, radio transmitters, motors, switches, relays, etc.
2) Natural disturbances — sunspots and lightning
3) Intrinsic noise sources — related to random fluctuations from physical systems such as thermal and shot noise

Noise cannot be eliminated totally. However, the magnitude and impact of noise can be reduced.

EMI Transmission

Understanding how noise is transmitted can help identify potential EMI problems in a circuit. For transmission to occur, noise has to be sourced, coupled, and received in a system. Figure 1 illustrates how EMI enters a system. All three elements must be present for any EMI problem to exist. Therefore, if any one of the three is minimized or taken out of the system, the interference is reduced or eliminated.

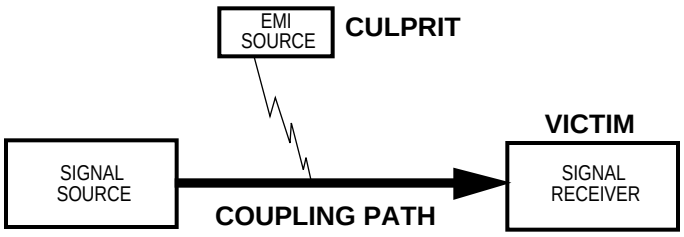

Figure 1. EMI Pathway

EMI Sources

Sources of EMI include microprocessors, microcontrollers, electrostatic discharges, transmitters, transient power components, AC supplies, and lightning. Within a microcontroller system, the digital clock circuitry is usually the biggest generator of wide-band noise, which is noise that is distributed throughout the frequency spectrum. With the increase of faster semiconductors and faster edge rates, these circuits can produce harmonic disturbances up to 300 MHz, which should be filtered out.

Coupling Paths

One of the more obvious ways noise can be coupled into a circuit is through conductors. If a wire runs through a noisy environment, the wire will pick up the noise inductively and pass it into the rest of the circuit. An example of this type of coupling is found when noise enters a system through the power supply leads. Once the noise is sourced in the power supply lines, it is then conducted to all circuits needing power. See Figure 2.

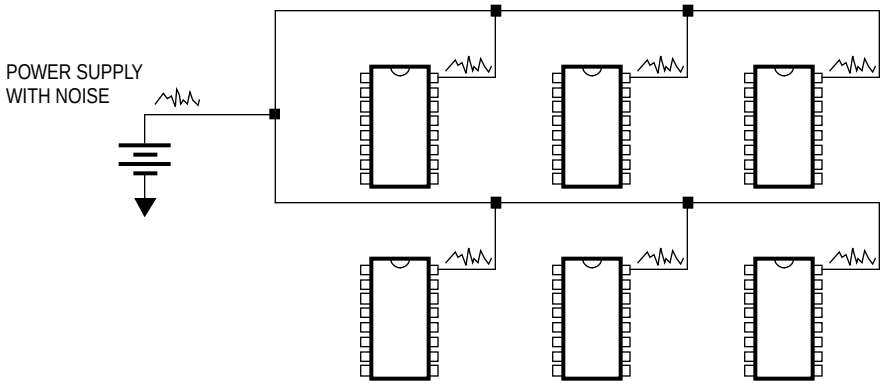

Figure 2. Conductor Coupled Noise

Coupling also can occur on circuits that share common impedances. For instance, Figure 3 shows two circuits that share the conductor carrying the supply voltage and the conductor carrying the return path to ground. If circuit one creates a sudden demand in current, circuit two's voltage supply will drop due to the common impedance both circuits share between the supply lines and the source impedance. This coupling effect can be reduced by decreasing the common impedance. Unfortunately, source impedance coupling is inherent to the power supply and cannot be reduced. The same effect occurs in the return-to-ground conductor. Digital return currents that flow from circuit two create high frequency digital noise in the common impedance of the return path. This noise creates ground bounce in circuit one's return path. An unstable ground will severely degrade the performance of low-level analog circuits, such as operational amplifiers and analog-to-digital converters, etc.

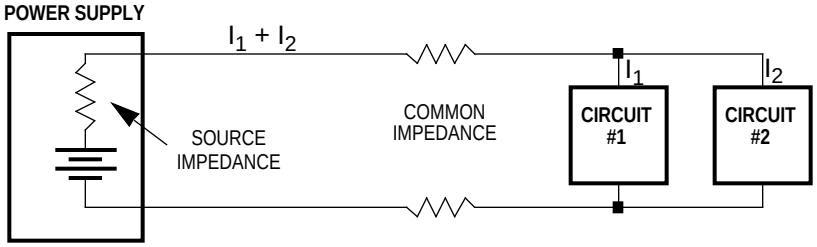

Figure 3. Coupling through Common Impedances

Coupling also can occur with radiated electric and magnetic fields which are common to all electrical circuits. Whenever current changes, electromagnetic waves are generated. These waves can couple over to nearby conductors and interfere with other signals within the circuit. See Figure 4.

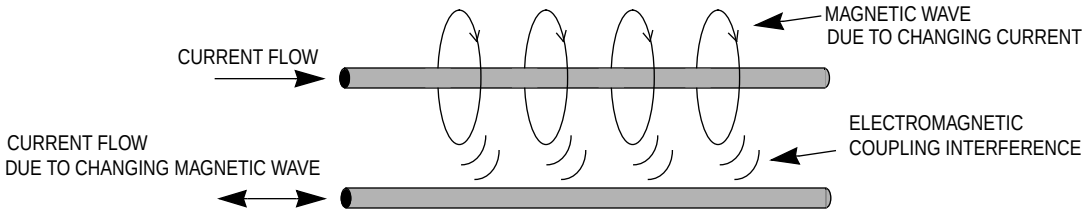

Figure 4. Coupling through Electromagnetic Radiation

Receptors

All electronic circuits are inherently receptive to EMI transmissions. Most EMI is received from conductive transients although some are received from direct radio frequency (RF) transmission. In digital circuits, the most critical signals are usually the most vulnerable to EMI. These include reset, interrupt, and control line signals. Analog low-level amplifiers, control circuits, and power regulators also are susceptible to noise interference.

Designing System Solutions for EMC

Electromagnetic compatibility (EMC) should be approached as a systems specification not as an afterthought. A circuit is electrically compatible if it does not affect or become affected by its environment. Some designers will ignore this potential problem unintentionally. In those cases, the design advances without consideration of EMI system design, although all bench tests pass and the design is ready to go to production. However, after the product has been produced and sent to the field, an unknown source of EMI is unexpectedly discovered. Finding a solution for the crisis is often frustrating and usually consists of undesirable add-ons and production delays, which consume time, money, and patience.

EMC should be designed into a system the same as any other legitimate system specification. In fact, some regulatory agencies have set standards for general computing equipment such as the Federal Communications Commission (FCC), the military, and international agencies. The designer should anticipate problems and resolve them in advance by using field-tested prototypes. With this approach, EMC is designed into the system up front rather than added on as a quick fix after a problem occurs. EMC system design quickly becomes an economically rewarding idea.

Although there are many remedies to EMC/EMI problems, they can be summarized by two different methods: decrease emissions and increase immunity. Emissions can be suppressed at the source through proper system design. But if the problem continues, investigate different methods of shielding to contain the emission. A circuit's susceptibility to noise can be decreased by hardening the circuit's design and using shielding to protect the circuit. The following discussion on layout techniques focuses on decreasing emissions and increasing noise immunity by applying general rules for sound PCB design.

GENERAL LAYOUT GUIDELINES

Component Placement

Before a PCB is layed out, care must be taken to place components properly on the PCB. Low-level analog, high-speed digital, and noisy circuits (relays, high-current switchers, etc.) must be separated to limit coupling between the subsystems to a minimum. When placing components, pay close attention to the potential routing of circuits between subsystems, including clocks and crystal circuits. A proposed layout should be examined for potential EMI problems. Iteratively review and correct layout until all EMI risks are addressed. Figure 5 illustrates the concept of separating components.

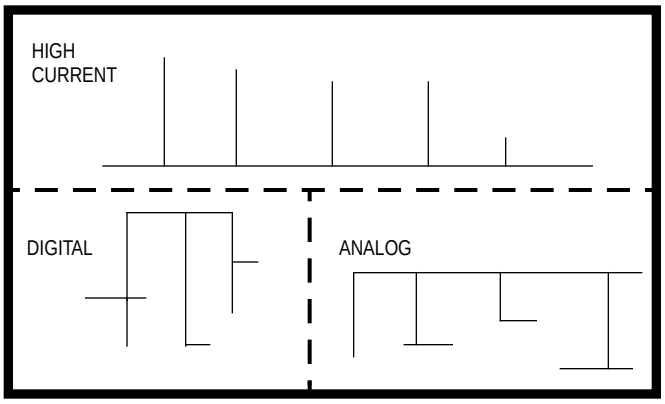

Figure 5. Separation of Circuits on a PCB

Ground Layout

Nothing is more important to the system design of a circuit than having a solid and complete power system. The ground layout is especially critical. In fact, the ground can be considered the foundation of all good PCB designs. Most EMI problems can be resolved by using practical and efficient grounding methods.

Defining Ground Noise

Understanding the mechanisms that generate ground noise is critical to minimizing ground interference. All ground paths have some finite impedance. As with all circuits, current flow must return to its source. Current flowing through finite impedance in the ground lines will cause a voltage drop. These voltage drops are the cause of interference in the ground system.

As system frequencies increase, the resultant interference in the ground system also increases. Elementary circuit theory says that a change in a conductor's current multiplied by the inductance of the conductor produces a voltage.

$$V = L \cdot \frac{di}{dt}$$

High-frequency digital systems create current spikes when transistors are switched on and off. Analog systems create current spikes when load currents change. As an example, consider a gate which is "on" and currently draws 4 mA of current. The gate is suddenly switched off and now draws 0.6 mA of current. The gate switched in 4 ns, and the conductor carrying the signal consists of 450 nH of inductance. The resulting voltage spike will be

$$L \cdot \frac{di}{dt} = 450\ \text{nH} \cdot \frac{\langle 4\ \text{mA} - 0.6\ \text{mA} \rangle}{4\ \text{ns}} = 0.383\ \text{V peak}$$

As noted earlier, faster systems produce faster rise times. Imagine if the next design in a product's life cycle incorporates faster logic. If the rise time of the new logic is twice as fast as the old, the noise in the redesign also will double in magnitude.

Most digital systems have a higher immunity to noise than analog. Low levels of noise in the ground system can severely affect the performance of low-level analog amplifiers, converters, etc. Noise can be coupled into other circuits by common impedance. Figure 6 illustrates the coupling problem.

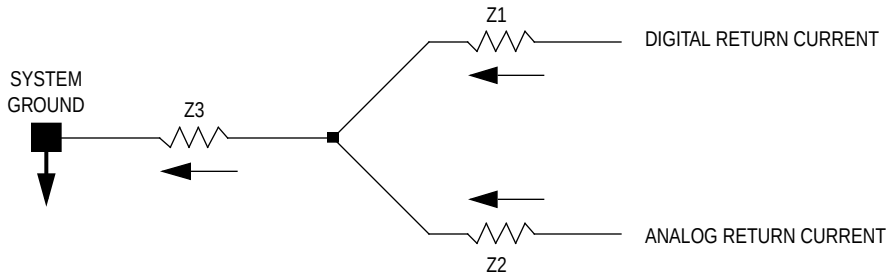

Figure 6. Common Impedance Coupling

The voltage at the summing point of the two signals is due to currents and inductances found in the analog and digital signals. The noise created is now shared due to common impedance, Z3, between the two signals. A DC offset is created between the system ground point and the summing point. In digital systems, this offset is dynamic and produces a high-frequency AC component of noise which will affect low-level analog circuitry.

Reducing Ground Noise

One advantage of a well-thought-out ground system is providing protection against unwanted interference without additional board cost except for engineering design time. The basic objective of a good ground system is to minimize noise voltage from currents flowing through ground impedances. In designing the ground system, it is important to ask: How does current flow in the system? Are quiet and noisy ground returns mixed together? Create signal grounds that have low-impedance paths to return to the source. This can be accomplished by determining the type of circuitry used and the operating frequency of the system.

Most MCU-based systems contain high-frequency digital logic and low-level analog circuits. Some systems may even have noisy relays and high-current switches. As mentioned earlier, these circuits should be separated and their ground returns should not be mixed together. Similar circuits should be placed together.

High-speed digital circuits must provide low-impedance pathways for all return signals. Design the ground system to include as many parallel pathways to ground as possible. This will decrease the inductance of the ground return. If this concept is taken to the limit, a ground plane will be created. Although ground planes are optimal, their use may not be desirable due to the added expense of a multi-layered PCB.

If a ground plane is uneconomical, then use single-point grounding. Single-point or star-point grounding ties all ground traces to the terminal ground point. This method lowers common impedance coupling between subsystems. Although this might be physically challenging due to space requirements, the decrease in common inductance and therefore coupled noise is worth the effort.

The inductance of a conductor is inversely proportional to the logorithm of the conductor's diameter or width but directly proportional to the length. To decrease the inductance, use as short and wide a trace as possible. Use 45-degree turns instead of 90-degree turns to decrease transmission reflections.

Remember that current will flow back to its source eventually. In some cases, the return path will create a large loop that is highly susceptible to electromagnetic radiation and will couple noise into the ground system. As a general rule, decrease the size of all ground loops as much as possible. Figure 7 shows an example of a single-point ground system on a 2-sided PCB.

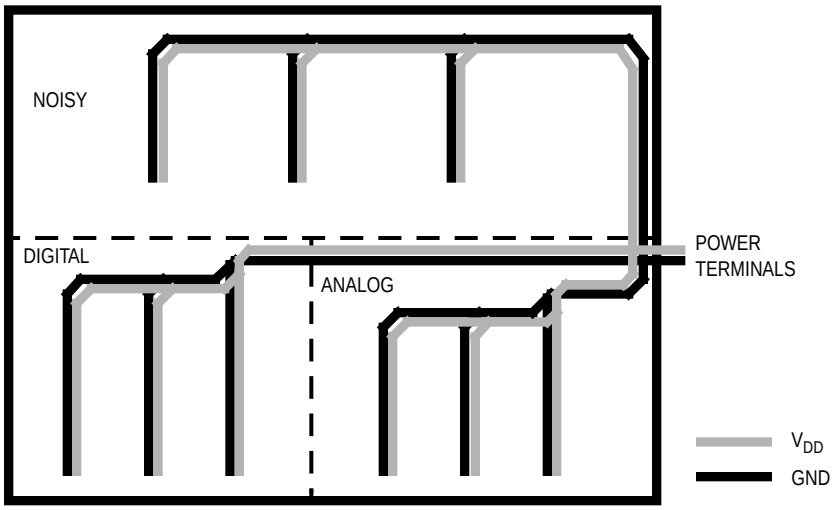

Figure 7. Single-Point Power System

Power System Layout and Decoupling

After a good ground system has been layed out on the PCB, the power system should be designed next. Power lines should run parallel to the ground lines if physically possible. If not, do not compromise the ground layout for the sake of the power layout. Power system noise can be decoupled with filters, but the ground system cannot. An example of a power layout is shown in Figure 7.

IC Power Decoupling

When a logic gate switches, a transient current is produced on the power supply lines. The impedance on the power supply lines along with the sudden current flow create a drop in voltage on the V_{DD} terminal. The inductance of the power supply lines can be reduced by using a multi-layer power plane. Fast switching speeds can be reduced by using slower logic. Usually, these solutions are not acceptable to system specifications. The current needed by an integrated circuit (IC) can be supplied from a nearby decoupling capacitor. This reduces the load on the power lines and removes unwanted glitches in the power system.

High-frequency, low-inductance axial glass or multi-layer ceramic capacitors should be used for decoupling ICs. Use a 0.1 µF capacitor for system frequencies up to 15 MHz. If the system frequency is above 15 MHz, use 0.01 µF capacitors Place the capacitor as close to the IC as possible. The standard of having the V_{DD} and GND pins at opposite ends of the chip creates a loop that is susceptible to EMI. The loop is considerably smaller if ICs have their power pins close together. Figure 8 illustrates capacitor placement for a typical logic IC. If the PCB has surface mount components, place the capacitor half way between V_{DD} and GND.

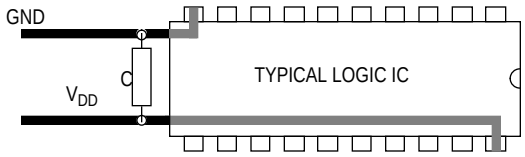

Figure 8. Decoupling Capacitor Placement

Bulk Decoupling Capacitor

The IC decoupling caps used for current glitches often deplete their charge reservoirs and must be recharged. This is done by using a bulk capacitor. The value of the bulk capacitor is not critical, but it should be able to recharge 15 to 20 ICs. If more ICs are on the PCB, bulk capacitors can be placed around the PCB to provide the needed charge.

For most MCU-based systems, one bulk capacitor is sufficient. The capacitor should have a small series inductance. Use tantalum electrolytic or metalized polycarbonate capacitors. Do not use aluminum electrolytic capacitors. The equivalent series inductance of an aluminum electrolytic is a magnitude higher than tantalum capacitors.

The bulk decoupling capacitor should be placed as close to the PCB power terminals as possible. A small 0.1 µF capacitor also should be used to decouple high frequency noise at the terminals. This capacitor should be placed as close to the power terminals as possible. Figure 9 illustrates power terminal decoupling.

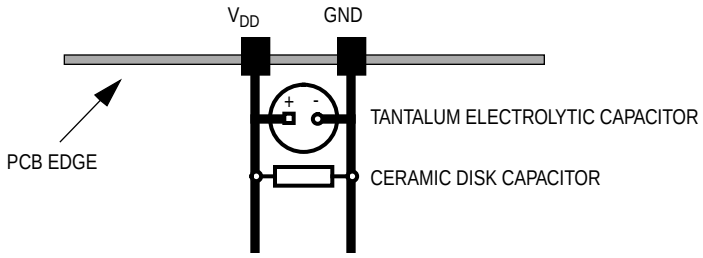

Figure 9. Power Terminal Decoupling Capacitor Placement

Isolating Circuits from Power Noise

If more filtering is needed to further isolate a circuit from noise on the power lines, use LC or Pi filters. Place the filters as close to the part as possible. Route all other signals around the filters. Figure 10 shows the filters schematics.

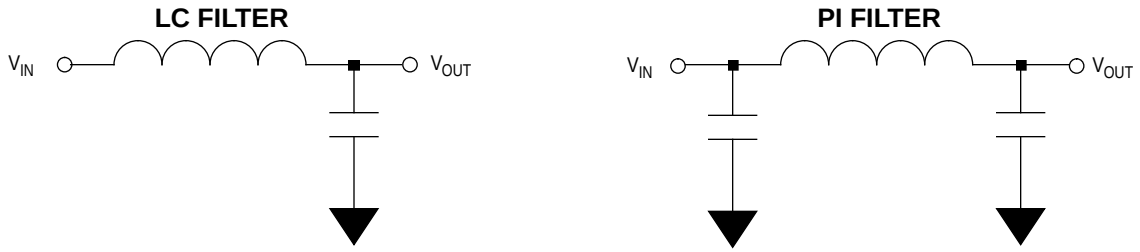

Figure 10. High Frequency Noise Filters

Ferrite beads also can be used to filter out unwanted system noise. They provide a relatively inexpensive way of adding high frequency loss without any power loss at DC or low frequencies. They are most effective at providing attenuation to signals above 1 MHz in low-impedance circuits such as power supplies and communication buses. Ferrite beads are cylindrical and are slipped over a conductor. The total impedance of a ferrite bead is limited to about 100 . When used on power supplies, place the beads near the power terminals of a PCB.

Signal Layout

After laying down the power and ground system traces, signal layout follows. When laying out mixed-signal boards, do not mix digital and analog signals together. Try to route sensitive lines first and be aware of potential coupling paths.

Digital Signals

The most sensitive signals in an MCU-based system are the clock, reset, and interrupt lines. The oscillator is especially sensitive during startup. Do not run these lines in parallel with high-current switching traces. They may become corrupted by electromagnetic cross-coupled signals. The effect could easily disrupt the MCU by interrupting code execution with an unexpected reset or interrupt. The clock could also jam, become out of phase, and bring the whole system out of sychronization. Because computer operating properly (COP) timers use the clock, do not rely on them to revive EMI hits.

If these signals are to go off the PCB, place the MCU near the off-board connector. If not, place the MCU where the trace lengths of these signals will be as short as possible.

The crystal or ceramic resonator clock is an RF circuit. The clock must be layed out to decrease its emission levels and susceptibility. Figure 11 shows an example of a crystal or ceramic resonator layout with a DIP package. Always place the circuit as close to the MCU as possible. If the crystal or ceramic resonator has a long body, lay it down flush with the PCB and ground the case. The ground signal of the crystal circuit should be connected to the ground pin of the part using the shortest trace possible. The power and ground pins should be routed directly to the power posts of the PCB.

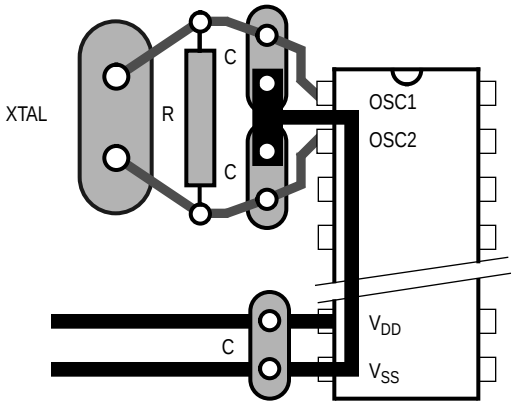

Figure 11. Crystal or Ceramic Resonator CIrcuit Layout

Analog Signals

Low-level signals can be corrupted easily by digital signals. If analog and digital signals have to be mixed, make sure the lines cross each other at 90-degree angles. This will reduce cross-coupling effects.

Analog-to-digital converter performance can be affected severely if the reference pins of the module are not separate from the digital power lines. Do not feed digital power and ground to analog-to-digital converter (ADC) reference lines. These pins should have reference voltages directly routed from the power terminals on the board. The voltage reference pin should be filtered with an RC circuit consisting of a 1-K resistor and a 1.0-µF capacitor

NOISE REDUCTION CHECKLIST

Listed below are details to check before a board goes to production. These are guidelines, not hard and fast rules to follow. This list was generated from collected field experience and the bibliography in this application note.

Suppressing the Noise Source

Use the lowest frequency clock and the slowest rise time that satisfy system specifications.

Place the clock circuit near the connector if the clock goes off the board. Otherwise, place the clock circuit at the center of the board.

Mount crystals flush to board and ground them.

Keep clock signal loop areas as close to zero as possible.

Locate I/O drivers near where they leave the board.

Filter all signals entering a board.

Filter all signals leaving a noisy environment.

Terminate unused op-amps in dual and quad packs by grounding the + input and connecting the - input to the output.

Provide relay coils some form of surge damping.

Use 45-degree angle trace turns instead of 90-degree angle trace turns to decrease radiation.

Reducing Noise Coupling

Separate circuits on a PCB according to their frequency and current switching levels.

Place chips for short clock runs.

Confine high speed logic to specific functions.

Place I/O chips next to the board edge and close to the connector.

If economically possible, use a multi-layer board to minimize power and ground inductance.

Use single-point power and ground layouts for single- and double-sided boards.

Use wide traces for power and ground.

Keep clock traces, buses, and chip enables separate from I/O lines and connectors.

Keep digital signal lines, especially the clock, as far away from analog input and voltage reference pins as possible.

When working with mixed-signal data converters, do not cross digital and analog lines. Route the signals away from each other.

Separate noisy and quiet leads.

Route clock signals perpendicular to I/O signals.

Keep clock circuits and leads away from I/O cables.

Keep the length of sensitive leads as short as possible.

Handle critical traces by fat traces and guardbanding with a ground on each side of the trace.

Do not run sensitive traces in parallel with high-current, fast-switching signals.

Minimize lead lengths on decoupling capacitors.

Keep high-speed lines short and direct.

Minimize trace length of clocks and other periodic signals.

Avoid running traces under crystals and other critically noise-sensitive circuits.

Filter any leads entering enclosures containing sensitive circuits.

When low-level signal leads and noisy leads are in the same connector, like a ribbon cable, separate them and place the ground leads between them.

Avoid ground loops in low-level, low-frequency circuits.

Twist noisy leads together to cancel mutual coupling.

Use all power and ground pins on an IC.

Reducing Noise Reception

Avoid all signal loops wherever possible; if not possible, minimize the loop area.

Use high-frequency, low-inductance ceramic disk or multilayer ceramic capacitors for IC decoupling.

Locate decoupling caps next to each IC in the system.

Use a bulk tantalum electrolytic or metalized polycarbonate decoupling capacitor to recharge the individual IC decoupling caps.

Bypass all electrolytic caps with small high-frequency caps.

If needed, supplement decoupling with ferrite beads in series.

Separate signal, noisy, and hardware power and grounds.

Use frequency selectable filters when applicable.

With tubular capacitors, connect outside foil end to ground.

Connect all unused inputs to power or ground or configure them as outputs.

Bypass all analog reference voltages.

Use series termination to attenuate transmission reflections.

Do not use sockets for high performance analog and mixed-signal ICs.

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