AN1248

Programmable Peripheral
Interfacing the PSD3XX to the MC143150

INTRODUCTION

Interfacing the PSD3XX to the MC143150 can increase the capability of the MC143150 without significantly increasing the board space and power consumption. The PSD3XX enhances the capabilities of the MC143150 by increasing both its I/O capability and memory capability. By using the PSD3XX, the I/O port capability can be expanded from 11 to 21 I/O ports. This two chip solution will also give the user up to 128 Kbytes of EPROM with built–in paging logic, 2 Kbytes of SRAM, and programmable logic for address decoding and integration of any glue logic. This application note describes the process of interfacing the PSD3XX to the MC143150.

The PSD311/311L is the 256K version and is not recommended for use with the MC143150. This document recommends: PSD312, PSD312L, PSD313, and PSD313L. The PSD312/312L and PSD313/313L contain 512K bits and 1M bits respectively.

A TYPICAL MC143150 DESIGN

Figure 1 shows a typical MC143150 node design before and after the use of a PSD3XX. The Before design includes an EPROM, SRAM, decoder to generate external chip selects, and an I/O port. For applications where space is critical, this implementation may be unacceptable. In the MC143150, memory locations E800 through FFFF are reserved for internal use. All external memory must be mapped from 0000 to E7FF. In order to take advantage of the full memory space, an external address decoder to the external memory devices must be incorporated. The After drawing shows a simpler smaller design.

MC143150 AND THE EXTERNAL MEMORY INTERFACE

The MC143150 provides an external memory bus to permit expansion of memory up to 58 Kbytes beyond the 512 Kbytes of EEPROM and 2 Kbytes of RAM resident on the chip. The MC143150 requires 16 Kbytes of external non–volatile memory to store its firmware. The remaining 42 Kbytes of external memory are available for user application program and data.

Assessing Memory Requirements

LONWORKS™ nodes based on the MC143150 use a combination of three different types of memory:

- Non–Volatile Memory for NEURON CHIP Firmware and, optionally, Application Code.
- Electrically Rewriteable Non–Volatile Memory for Network and Application Code and Data.
- Read/Write Memory for Packet Buffering, or, optionally, Application Code and Data.

A LONWORKS application node may include the external memory types described above by partitioning the available 58 Kbyte memory space into three distinct regions aligned on 256–byte page boundaries. The different memory types do not need to map to contiguous address space. However, the LONBUILDER™ NEURON C compiler enforces the ordering of the types of memory to be ROM/EPROM first, EEPROM second, and finally RAM. The NEURON C compiler and LONBUILDER linker locate parts of an application in appropriate memory regions (see Chapter 6 of the *NEURON C Programmer's Guide*).

Memory Interface Logical Description

Figure 2 shows the memory map of the MC143150. Memory locations from 0 to E7FF are external to the MC143150. Access to this memory is through an external memory bus consisting of eight bi–directional three–state data lines, 16 unidirectional address lines driven by the MC143150, and two control lines.

The two control lines used for the external memory interface are:

$\overline{E}$ — Enable Clock

This output is a strobe driven by the MC143150 to synchronize the external bus. Its frequency is one–half that of the input clock or crystal. $\overline{E}$ is low during the second half of the memory cycle, which indicates that the MC143150 is actively reading or writing data. During write cycles, the MC143150 drives the new data onto the data bus during the time $\overline{E}$ is low. During read cycles, the MC143150 clocks in the external data on the transition of $\overline{E}$.

R/$\overline{W}$ — Read/Write

This output indicates the direction of the data bus. It is set by the MC143150 to high during a Read cycle, and low on a Write cycle. R/$\overline{W}$ changes state during the time $\overline{E}$ is high, and is stable during the time $\overline{E}$ is low.

See the section on Special Timing Considerations for more information on the MC143150 memory interface requirements.

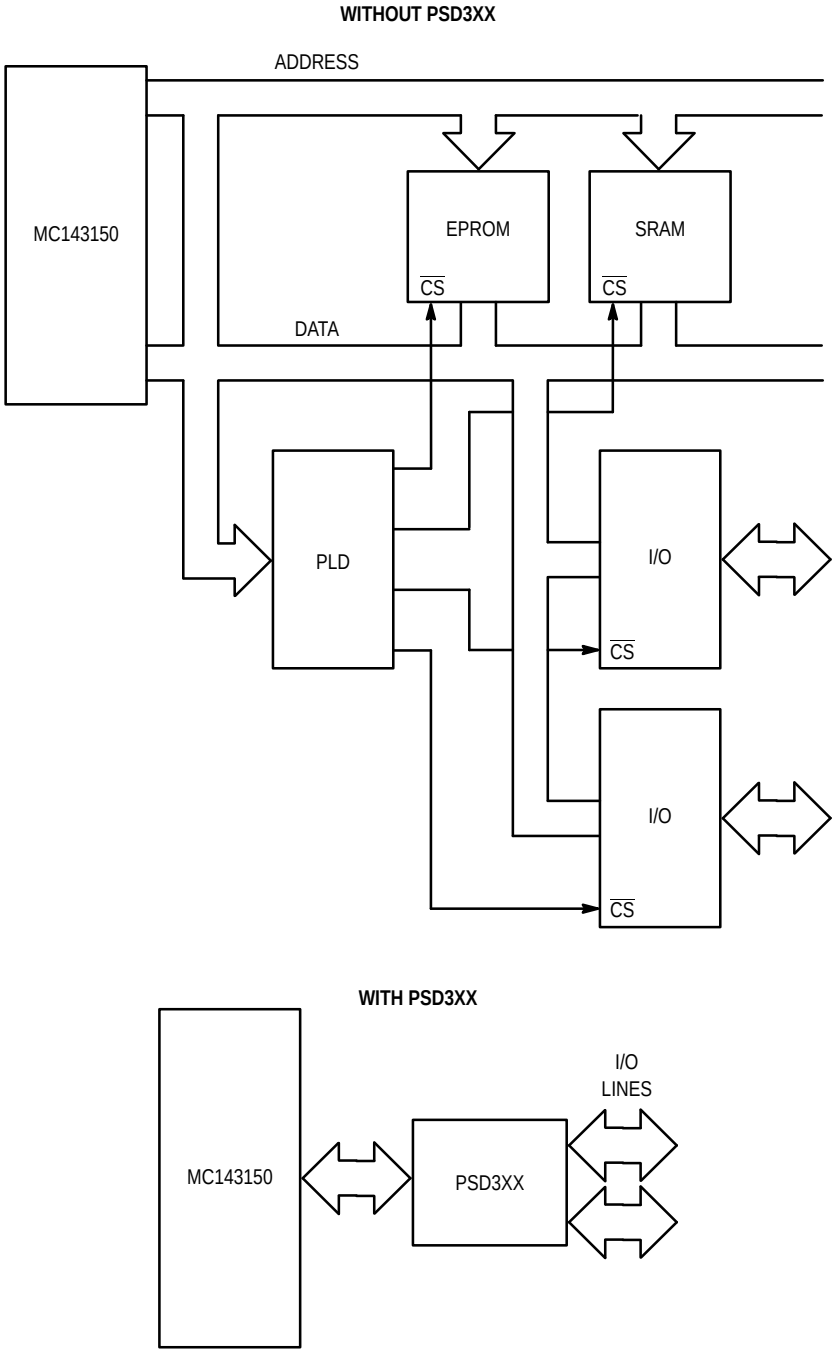


Figure 1. Before and After Interfacing to the WSI PSD3XX

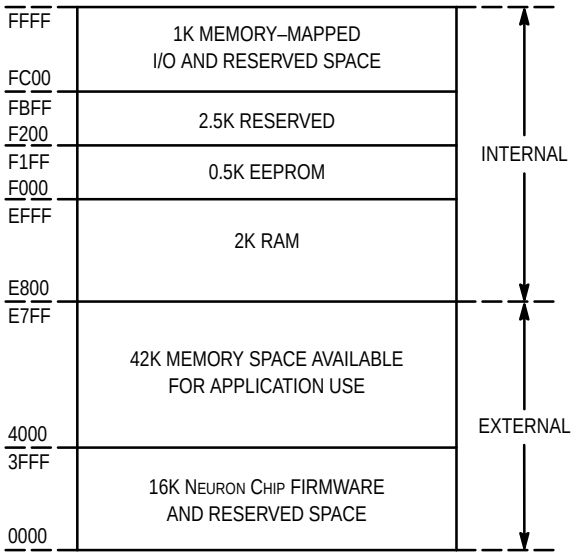


Figure 2. The MC143150 Memory Map

PSD3XX ARCHITECTURE

The PSD3XX integrates high performance user–configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks as shown in Figure 3 include two programmable logic arrays, Programmable Address Decoder (PAD A and PAD B), 256K bits to 1M bits of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD3XX is ideal for applications requiring high performance, low power, and very small form factors.

The PSD3XX offers a unique single–chip solution for users of the MC143150 that need more memory–mapped I/O, larger EPROM and SRAM size, external chip selects, and programmable logic. Table 1 summarizes the PSD3XX devices that can interface to the MC143150. The PSD3XXL devices can operate down to 3.0 V for low power applications.

As shown in Figure 4, WSI's PSD3XX can efficiently interface with, and enhance, the MC143150. This is the first solution that provides the MC143150 with port expansion, page logic, two programmable logic arrays (PAD A and PAD B), 256K bits to 1M bits of EPROM, and 16K bits of SRAM on a single chip. The PSD3XX does not require any glue logic for interfacing to the MC143150.

The PSD3XX on–chip PAD A enables the user to map the I/O ports, eight segments of EPROM (8K x 8 each) and SRAM (2K x 8) anywhere in the address space of the MC143150. PAD B can implement up to 4 sum–of–product expressions based on address inputs, control signals, and other external input signals.

The Page Register extends the accessible address space of the MC143150 from 64 Kbytes to 1 mbytes. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of the MC143150 by a factor of 16. Paging is not supported by the NEURON CHIP firmware or LONBUILDER tools and must therefore be managed entirely by the application program.

Figure 4 shows how to interface the PSD312 or PSD313 to the MC143150. The PSD3XX is operated in the Non–Multiplexed Address/Data Mode with 8–bit Data Bus. The low–order address/data bus (AD0/A0 – AD7/A7) is the low–order address input bus. The high–order address/data bus (A8 – A15) is the high–order address bus byte. Port A is the low–order data bus. External logic is required to interface with the PSD311. Therefore, it is recommended that the PSD312 or PSD313 be used.

Programmable Address Decoder (PAD)

The PSD3XX consists of two programmable arrays referred to as PAD A and PAD B. PAD A is used to generate chip select signals derived form the input address to the internal EPROM blocks, SRAM, and I/O ports.

PAD B can be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user. Figure 5 shows the PSD3XX PAD description.

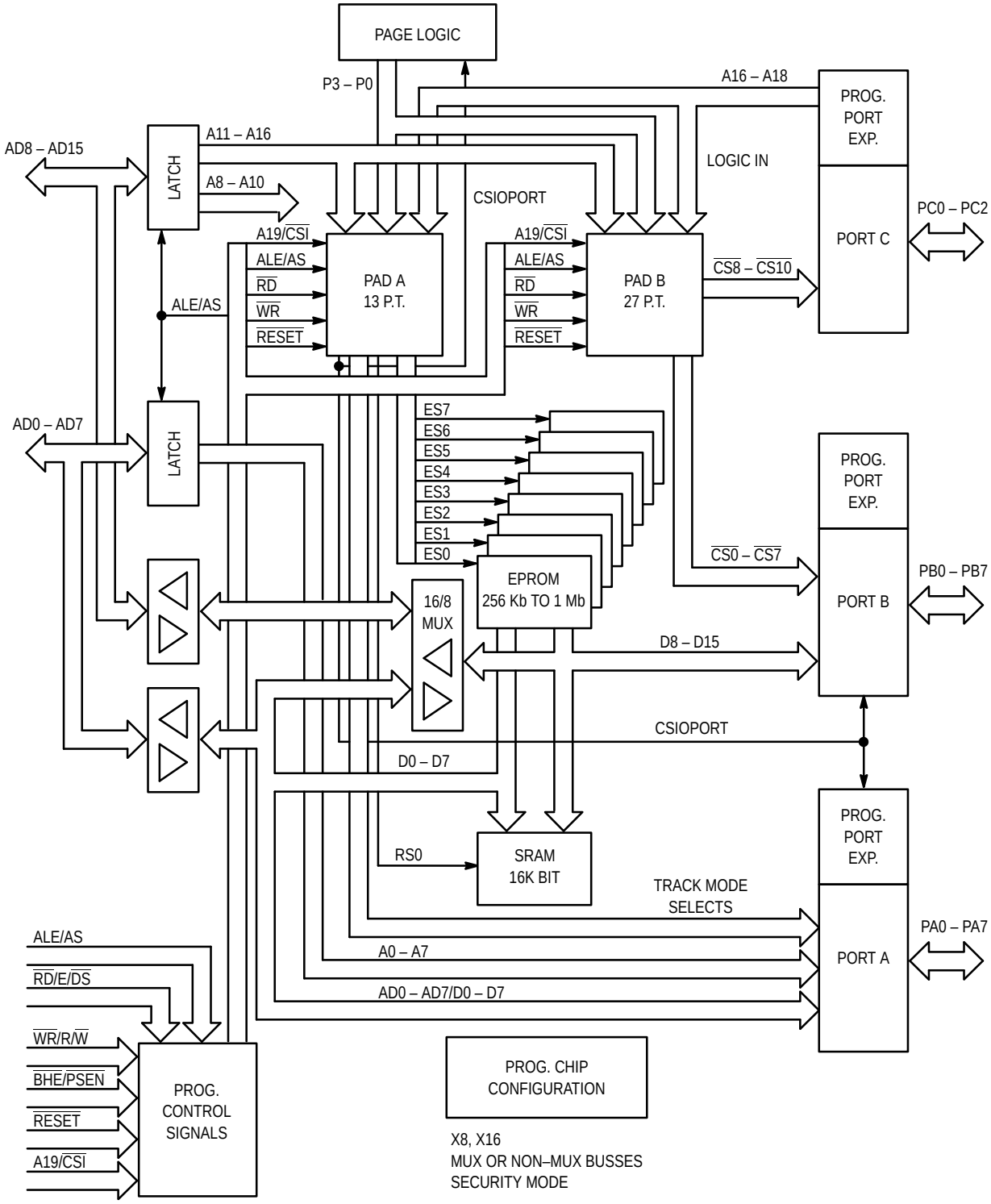
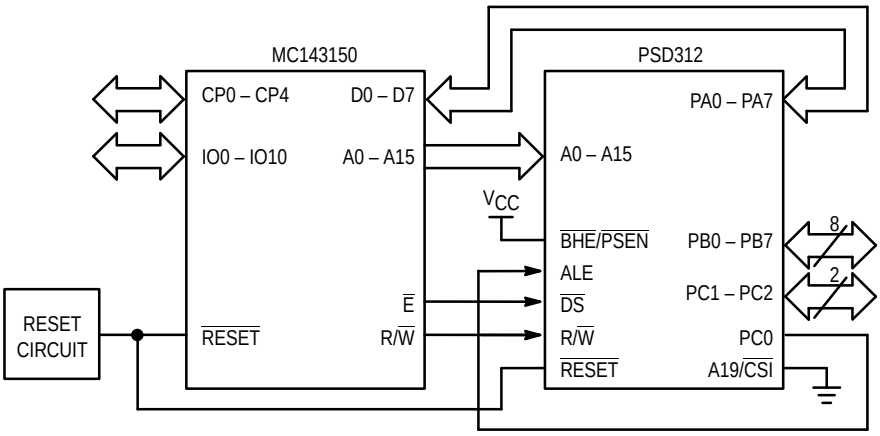


Figure 3. PSD3XX Architecture

Table 1. PSD3XX Devices

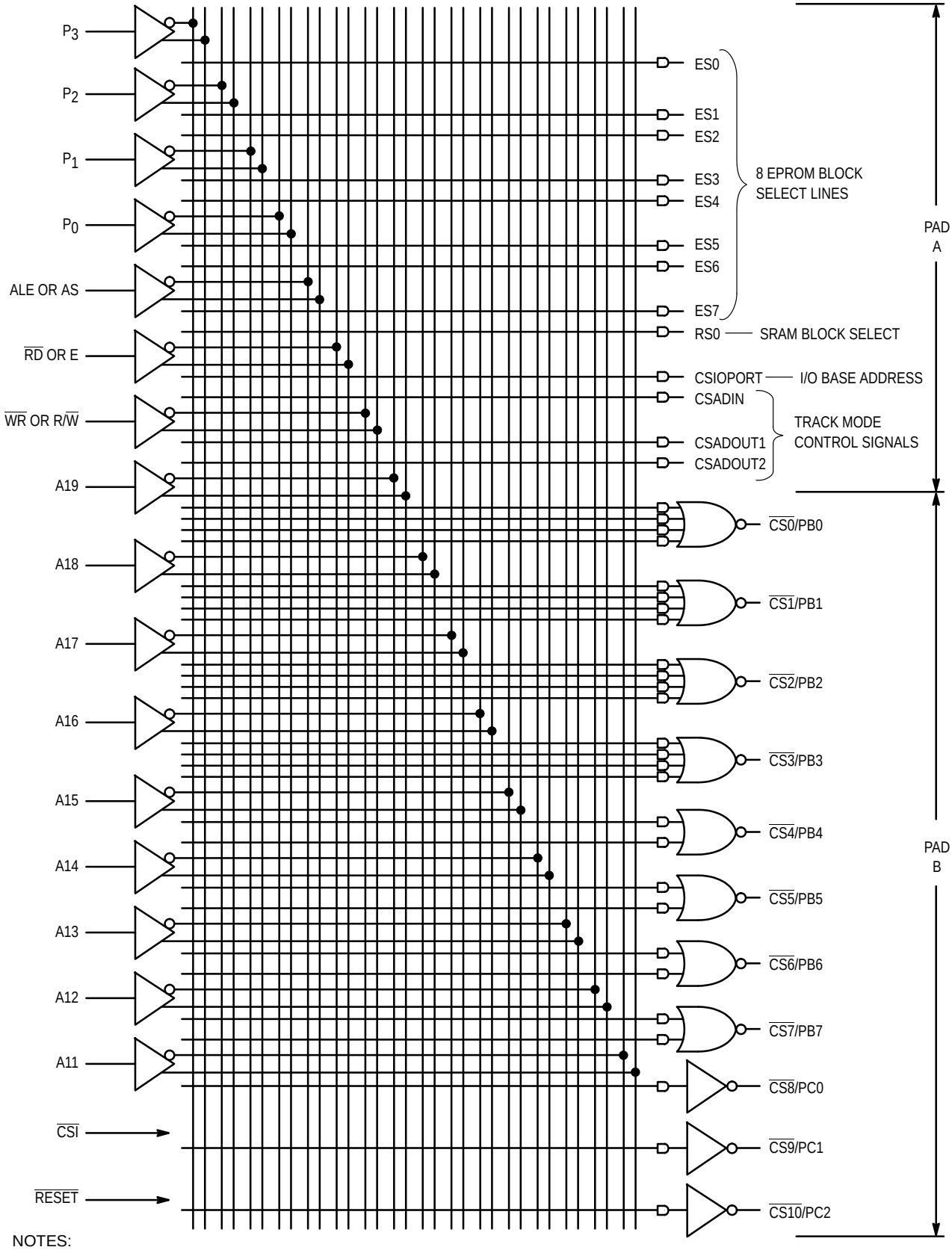
Device	I/O Ports	EPROM (Bits)	SRAM (Bits)	Data Path (Bits)	Supply Voltage
PSD312 PSD312L	19 19	512K 512K	16K 16K	8 8	5 V 3 V – 5 V
PSD313 PSD313L	19 19	1024K 1024K	16K 16K	8 8	5 V 3 V – 5 V



Integrating the PSD312 to the MC143150 adds:

- 10 Chip Selects or Data I/O Ports (in addition to the 11 I/O on the MC143150).
- 64 Kbytes of EPROM (expandable to 128 Kbytes).
- 2 Kbytes of SRAM.
- All Decode Logic for External Chip Selects and Internal Memory.

Figure 4. Interfacing the PSD312 to the MC143150



NOTES:

1. $\overline{CSI}$ is a power–down signal. When high, the PAD is in stand–by mode and all its outputs become non–active.
2. RESET deselects all PAD output signals.
3. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or CS10, A17 or CS9, and A16 or CS8 can be routed to the external pins of Port C. Port C can be configured as either input or output.

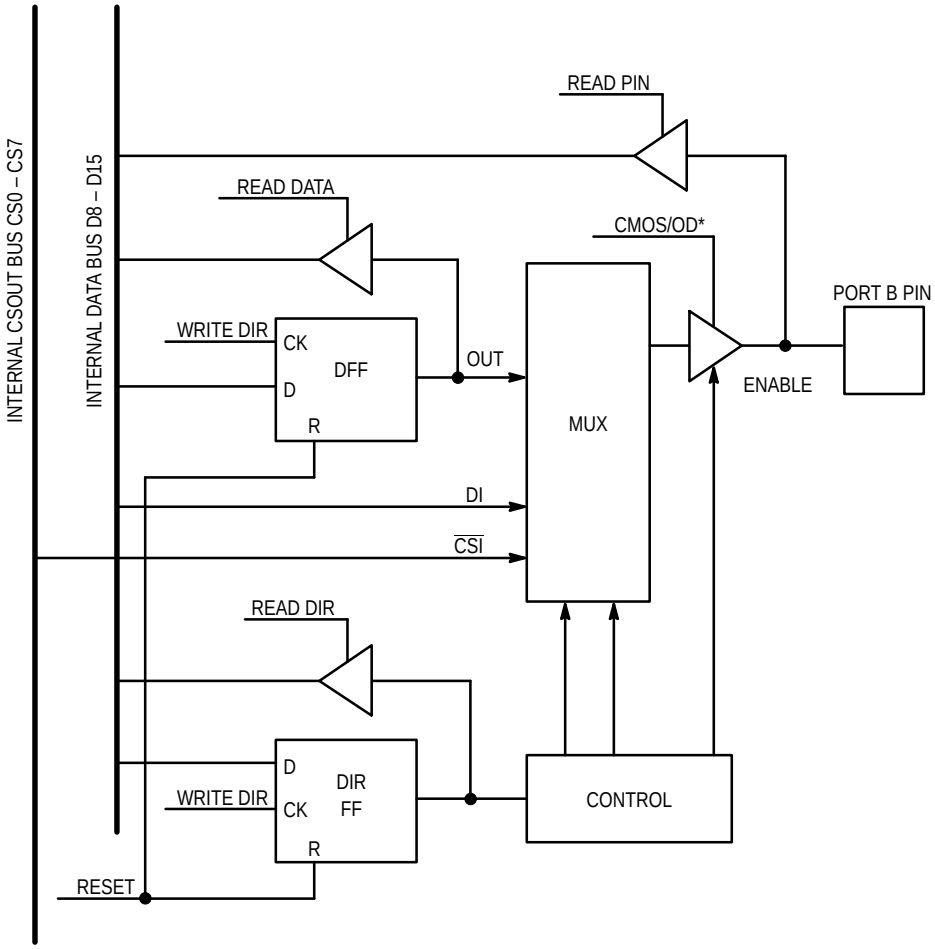
Figure 5. PSD3XX PAD Description

Port Functions

The PSD3XX has three I/O ports (Port A, B, and C) that are configurable at the bit level.

Port A — When interfacing to the MC143150, Port A is used for the lower order data bus.

Port B — The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin level can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull–up resistors. For addressing information, refer to Table 2.



*CMOS/OD determines whether the output is open drain or CMOS

Figure 6. Port B Pin Structure

Table 2. I/O Port Addresses in an 8–Bit Data Bus Mode

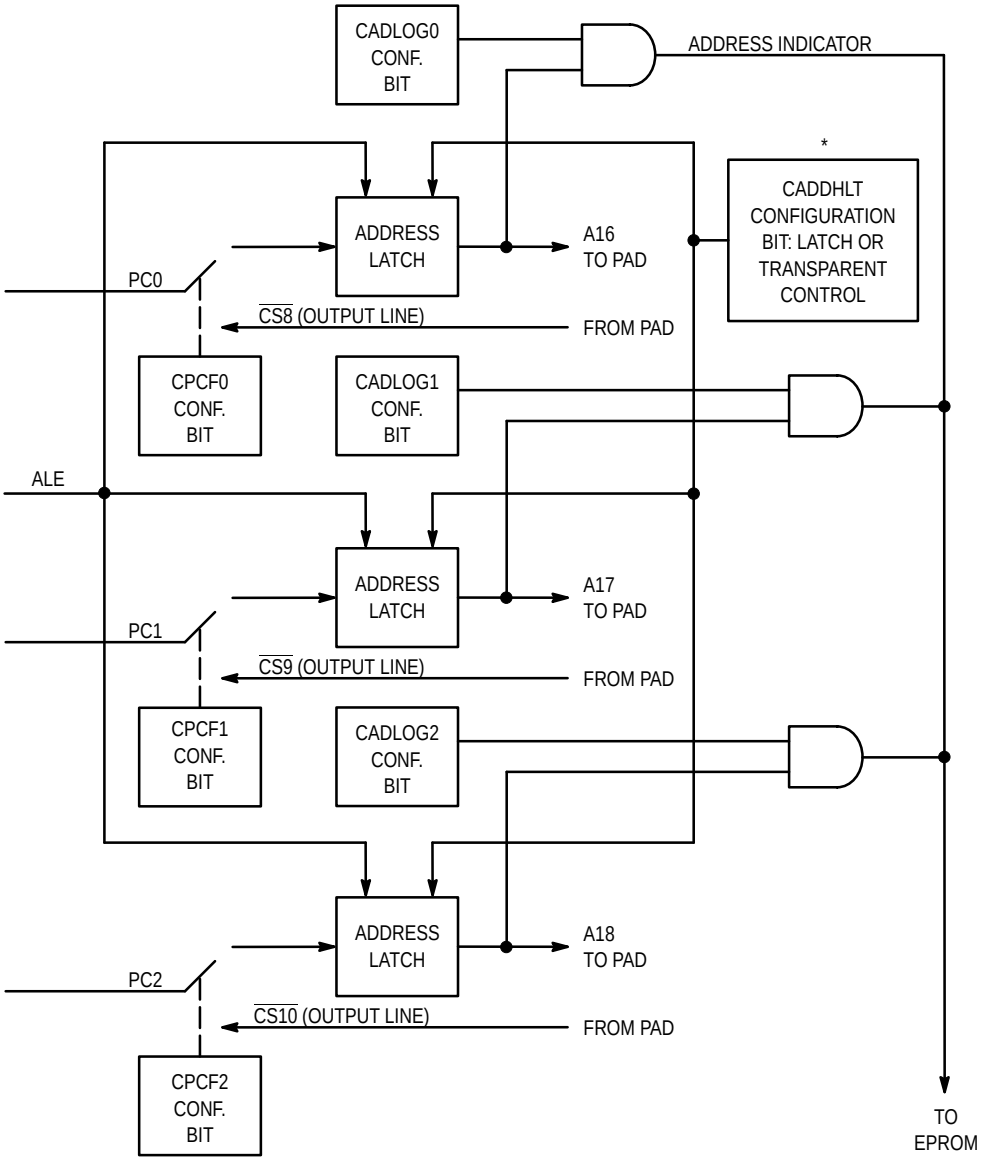
Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Alternatively, each bit of Port B can be configured to provide a chip–select output signal from PAD B, PB0 – PB7 can provide $\overline{CS0}$ – $\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$ – $\overline{CS3}$ is comprised of four product terms. Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$ – $\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Accessing the I/O Port — Table 2 shows the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in all Modes — Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16 – A18. Although the pins are given names of the high–order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8 – A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$ – $\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$ – $\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternatively, PC0 – PC2 can become $\overline{CS8}$ – $\overline{CS10}$ outputs, respectively, providing the user with more external chip–select PAD outputs. Each of the signals $\overline{CS8}$ – $\overline{CS10}$ is comprised of one product term.



* The CADDHLT configuration bit determines if A18 – A16 are transparent via the latch, or it they must be latched by the trailing edge of the ALE strobe.

Figure 7. Port C Structure

EPROM

The PSD3XX has 256K bits to 1M bits of EPROM and is organized from 32K x 8 to 128K x 8. The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0 – Bank7 can be selected by PAD outputs ES0 – ES7, respectively. The EPROM banks are organized from 4K x 8 to 16K x 8.

SRAM

The PSD3XX has 16K bits of SRAM and is organized as 2K x 8. The SRAM is selected by the RS0 output of the PAD.

Control Signals

The PSD3XX control signals are $\overline{WR}$ or R/$\overline{W}$, $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{PSEN}$, RESET, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of the MC143150.

$\overline{WR}$ or R/$\overline{W}$ — The $\overline{WR}$ or R/$\overline{W}$ pin is configured as R/$\overline{W}$. This pin works with the $\overline{DS}$ strobe of the $\overline{RD}$/E/$\overline{DS}$ pin. When R/$\overline{W}$ is high, an active low signal on the $\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active low signal on the $\overline{DS}$ pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$ — The $\overline{RD}$/E/$\overline{DS}$ pin is configured as $\overline{DS}$. This pin works with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write). The $\overline{DS}$ feature is not available on the PSD311 and PSD301. The E input must be used. To generate to correct polarity, an external inverter must be used. *To minimize board space and to meet critical timing requirements, it is recommended to use the PSD312 or PSD313 with the MC143150.*

ALE — To prevent a timing violation with the Address Hold time, the ALE input pin is used to latch the address into the PSD3XX. As shown in Figure 4, PC0 output signal from Port C on the PSD3XX is connected to the ALE input to the PSD3XX. The PC0 output signal is a delayed version of the $\overline{E}$ signal from the MC143150. Further information on this special timing condition is discussed after Figure 9.

$\overline{PSEN}$ — The $\overline{PSEN}$ signal is not used with the MC143150 and therefore must be connected to V_{CC}.

RESET — This is an asynchronous input pin that clears and initializes the PSD3XX/3XXL. On the PSD3XX, reset polarity is programmable (active low or active high). Whenever the PSD3XX reset input is driven active for at least 100 ns, the chip is reset. On the PSD3XXL, reset is a low signal only. This device is reset and operational only after the reset input is driven low for at least 500 ns followed by another 500 ns period after the reset becomes high. In either device, the part is not automatically reset internally during boot–up and an external reset procedure is recommended for best results. Tables 3 and 4 indicate the state of the part during and after reset.

A19/$\overline{CSI}$ — When configured as $\overline{CSI}$, a high on this pin deselects and powers down the chip. A low on this pin puts the chip in normal operational mode. For PSD3XX states during the power–down mode, see Tables 5, 6, and Figure 8. The contents of the SRAM is preserved during the power–down mode. There is an Application Note on the Power–Down Mode in the Programmable Peripherals Design and Applications Handbook from WSI.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line or as a general–purpose logic input. A19 can be configured as ALE dependent or as transparent input. In this mode, the chip is always enabled.

Table 3. Signal States During and After Reset

Signal	Configuration Mode	Condition
AD0/A0 – AD7/A7	All	Input
A8 – A15	All	Input
PA0 – PA7 (Port A)	I/O Tracking AD0/A0 – AD7 Address outputs A0 – A7	Input Input Low
PB0 – PB7 (Port B)	I/O $\overline{CS7}$ – $\overline{CS0}$ CMOS outputs $\overline{CS7}$ – $\overline{CS0}$ open drain outputs	Input High Tri–Stated
PC0 – PC2 (Port C)	Address inputs A16 — A18 $\overline{CS8}$ – $\overline{CS10}$ CMOS outputs	Input High

Table 4. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$ — $\overline{CS10}$	All = 1*
	CSADIN, CSADOUT1 CSADOUT2, CSIOPORT, RS0, ES0 — ES7	All = 0*
Data Register A Direction Register A Data Register B Direction Register B	N/A N/A N/A N/A	0 0 0 0

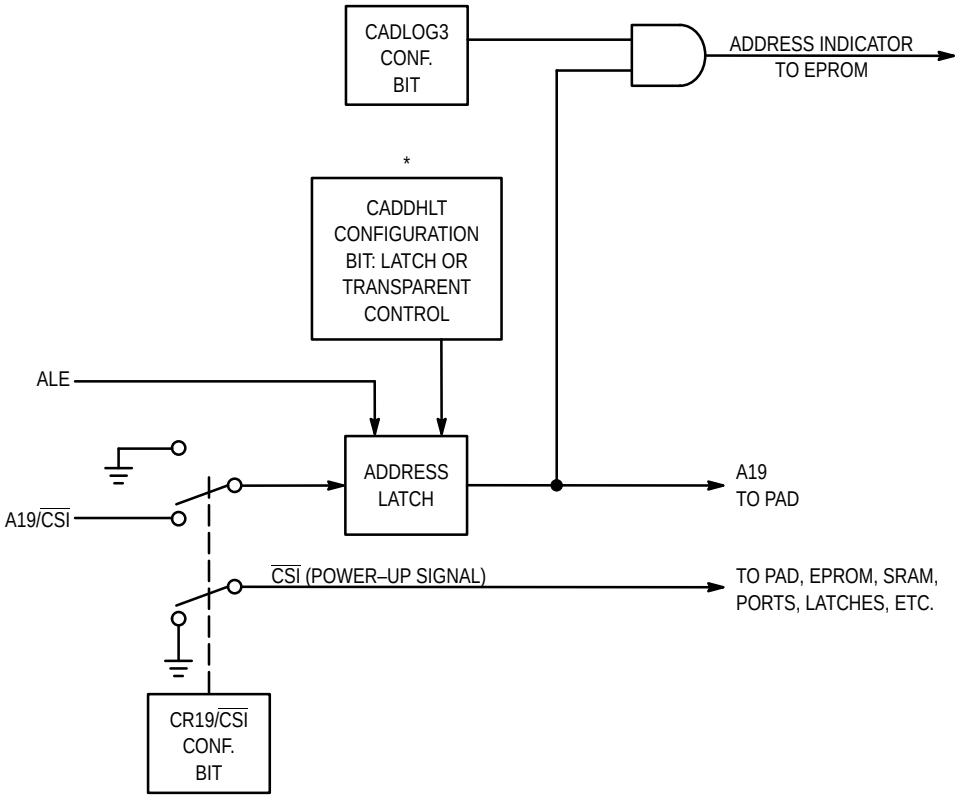
*All PAD outputs are in a non–active state.

Table 5. Signal States During Power–Down Mode

Signal	Configuration Mode	Condition
AD0/A0 – AD7/A7	All	Input
A8 – A15	All	Input
PA0 – PA7	I/O Tracking AD0/A0 – AD7 Address outputs A0 – A7	Unchanged Input All 1's
PB0 – PB7	I/O $\overline{CS7}$ – $\overline{CS0}$ CMOS outputs $\overline{CS7}$ – $\overline{CS0}$ open drain outputs	Unchanged All 1's Tri–Stated
PC0 – PC2	Address inputs A16 — A18 $\overline{CS8}$ – $\overline{CS10}$ CMOS outputs	Input All 1's

Table 6. Internal States During Power Down

Component	Signals	Contents
PAD	$\overline{CS0}$ – $\overline{CS10}$	All 1's (Deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0 – ES7	All 0's (Deselected)
Data Register A Direction Register A Data Register B Direction Register B	N/A N/A N/A N/A	All Unchanged



* The CADDHLT configuration bit determines if A19 – A16 are transparent via the latch, or f they must be latched by the trailing edge of the ALE strobe.

Figure 8. A19/CSI Cell Structure

PAGE REGISTER

The page register consists of four flip–flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3 – D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3 – P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 9. There is an Application Note from WSI that discusses how to use the Paging Register (see References). Because of the flexibility of the programmable logic in the PSD3XX, some blocks of EPROM can be common to each page while other blocks of EPROM can be unique to each page. The SRAM and I/O ports can be programmed to be either common to all pages or unique to a specific page. Since the paging logic is transparent to the MC143150, the NEURON C application program running on the MC143150 must be designed to use this feature.

SECURITY MODE

The Security Mode in the PSD3XX locks the contents of the PAD A, PAD B, and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In the window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD3XX contents cannot be copied on a programmer. Because the high integration of the address decoding, eight blocks of EPROM, and SRAM, it is difficult to copy the contents of the EPROM in–circuit. The SRAM can be mapped dynamically over the EPROM, protecting the contents of the EPROM. The internal page register can be used to map different EPROM blocks onto different pages. This would make it difficult for someone to externally sequence through the address space and capture the code on the MCU bus with a logic analyzer. Because of the flexibility of the PSD3XX, other protection schemes are possible to protect the contents of the EPROM along with the configuration of the PSD3XX from being copied.

SPECIAL TIMING CONSIDERATIONS

When interfacing the PSD3XX to the MC143150, a potential Address Hold time violation may occur (t_{AH} in Figure 10). The minimum Address Hold Time requirement of the PSD3XX is 15 ns. The maximum Address Hold Time of the MC143150 is 7 ns. To prevent this timing violation from occurring under worst case conditions, the $\overline{E}$ signal from the MC143150 is delayed through the PSD3XX and connected to the ALE input as shown in Figure 4. The $\overline{E}$ signal is connected to the $\overline{DS}$ input on the PSD3XX. This input is also used as a logic input to the PAD. The $\overline{E}$ signal is delayed for 15 ns by feeding it through the internal PAD, and out PC0. PC0 is connected to the ALE input in–order to latch and hold the address input and meet the internal Address Hold time requirement in the PSD3XX.

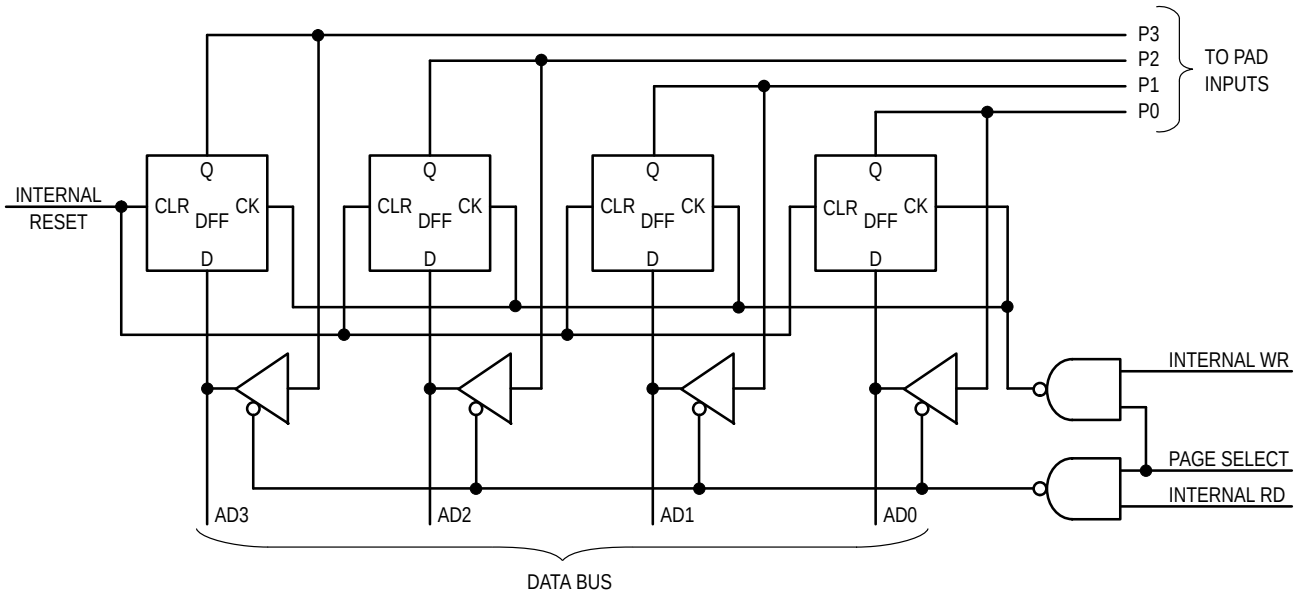


Figure 9. Page Register

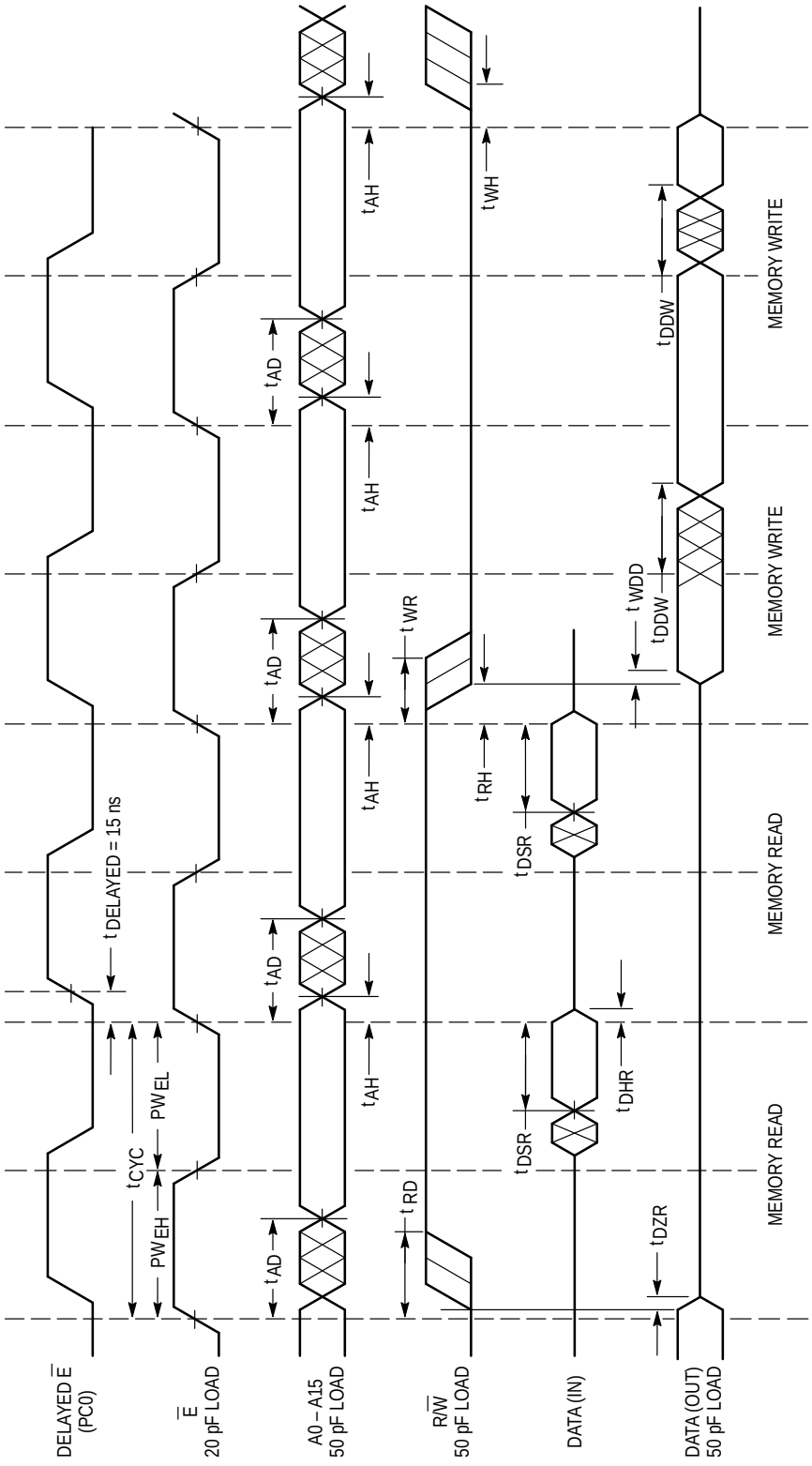


Figure 10. MC143150 Memory Interface Timing Diagram

DEVELOPMENT PROCESS

The PSD3XX features a complete set of System Development Tools. These tools provide an integrated, easy–to–use software and hardware environment to support PSD3XX device development. To run these tools requires an IBM–XT, –AT, or compatible computer, MS–DOS 3.1 or higher, 640 Kbyte RAM, and a hard disk.

The configuration of the PSD3XX device is entered using MAPLE software. The MAPLE output listing of a PSD312 configured to interface to the MC143150 is shown on the next few pages. Once the PSD3XX is configured, the configuration information along with the EPROM code is compiled into one file with an ".obj" extension. This file is used to program a PSD3XX device on WSI's MagicPro Programmer or on a third party programmer that supports the PSD3XX.

As shown on the MAPLE output listing "echelon.sv1":

PSD Selected:

PSD312

Bus Interface:

Non–multiplexed bus, 8–bit, with R/$\overline{W}$ and $\overline{DS}$, signals.

Port A:

PA7 – PA0 are used as the data bus interface (D7 – D0) on the MC143150.

Port B:

PB7 – PB0 can be used as Data I/O or Chip Selects. Each pin can be individually configured.

Port C:

PC2 – PC1 can be configured as Logic inputs, or Chip Select outputs. PC0 is used as a Chip Select output and is connected to the ALE input on the PSD3XX. The Chip Select equations is $\overline{CS8}$ = $\overline{DS}$. The E signal is only delayed through the PAD. The logic of this signal is not changed.

The PSD312 contains 64K x 8 of EPROM but only 54 Kbytes are used. The SRAM (RSO) and I/O Ports (CSP) can mapped over the EPROM. The portion of EPROM that overlaps the SRAM and I/O Ports cannot be used. Table 7 shows the defined Memory Map in this example.

Note that the upper 2 Kbytes of EPROM Block (ES6) is mapped in the same address space as the I/O Ports (in the range of D800 – DFFF). Because of the overlap, the portion of EPROM from D800 – DFFF cannot be accessed.

The MC143150's memory map is defined through the Memory Properties screen of the LONBUILDER Software. The amount of each type of memory used, ROM, EEPROM, RAM, and memory mapped I/O is entered in this screen so that they match the actual external memory connected to the MC143150. The values for this example entered into the Memory Properties screen are shown in Table 8. Refer to the *LONBUILDER User's Guide* for more information.

Table 7. Memory Map Example

Address Range	Size (Bytes)	Memory Type	Physical Location
0 – D7FF	54K	EPROM	PSD312
D800 – DFFF	2K	Memory–Mapped I/O	PSD312
E000 – E7FF	2K	SRAM	PSD312
E800 – EFFF	2K	RAM	MC143150
F000 – FIFF	0.5K	EEPROM	MC143150
F200 – FBFF	2.5K	Reserved	MC143150
FC00 – FFFF	1K	Memory–Mapped I/O and Reserved	MC143150

Table 8. Memory Properties Screen of the LONBUILDER

Memory Type	Number of Pages	Start Address	End Address
ROM	215	0000	D7FF
EEPROM	0	—	—
RAM	8	E000	E7FF
I/O	8	D800	DFFF

MAPLE OUTPUT LISTING

```
****************************** MAPLE 5.10 *********************************
PSD PART USED: PSD312
*************************PROJECT INFORMATION*****************************
  Project Name      : = Echelon WSi Integration
  Your Name         : = Dan Friedman
  Date              : = 10/8/92
  Host Processor    : = 3150
*************************************************************************
*********************************ALIASES*********************************
*************************************************************************
*************************GLOBAL CONFIGURATION*****************************
  Address/Data Mode   : NM
  Data Bus Size       : 8
  Reset Polarity      : LO
  Security            : OFF
  AS Polarity         : HI
  A15–A0 AS dependent (Y) or Transparent (N): Y
  Are you using PSEN ? (Y/N)                : N
*************************************************************************
***************************READ WRITE CONTROL******************************
R/(/W) and /DS
*************************************************************************
***************************Port A CONFIGURATION****************************
Port A is Data Bus D0–D7
***************************PORT B CONFIGURATION****************************
Pin    CS/IO     CMOS/OD
PB0     IO        CMOS
PB1     IO        CMOS
PB2     IO        CMOS
PB3     IO        CMOS
PB4     IO        CMOS
PB5     IO        CMOS
PB6     IO        CMOS
PB7     IO        CMOS
*************************************************************************
***************************PORT B CHIP SELECT EQUATIONS********************
*****************************PORT C CONFIGURATION**************************
Pin    CS/Ai    LOGIC/ADDR
PC0     CS8
PC1     CS9
PC2    CS10
A19     CSI
*************************************************************************
***************************PORT C CHIP SELECT EQUATIONS********************
/CS8  =  /(/DS)
*********************************ADDRESS MAP*********************************
        A   A     A   A   A   A   A   A   A    SEGMT  SEGMT FILE  FILE     File Name
        19  18    17  16  15  14  13  12  11    STRT   STOP  STRT  STOP
ES0      N   N     N   N   0   0   0   N   N      0    1fff   0   1fff   ECH_TEST.HEX
ES1      N   N     N   N   0   0   1   N   N   2000   3fff  2000  3fff   ECH_TEST.HEX
ES2      N   N     N   N   0   1   0   N   N   4000   5fff  4000  5fff   ECH_TEST.HEX
ES3      N   N     N   N   0   1   1   N   N   6000   7fff  6000  7fff   ECH_TEST.HEX
ES4      N   N     N   N   1   0   0   N   N   8000   9fff  8000  9fff   ECH_TEST.HEX
ES5      N   N     N   N   1   0   1   N   N   a000   bfff  a000  bfff   ECH_TEST.HEX
ES6      N   N     N   N   1   1   0   N   N   c000   dfff  c000  dfff   ECH_TEST.HEX
ES7      N   N     N   N               N   N
RS0      N   N     N   N   1   1   1   0   0   e000   e7ff  N/A   N/A        N/A
CSP      N   N     N   N   1   1   0   1   1   d800   dfff  N/A   N/A        N/A
*************************************END*************************************
```

```
**************************ADDRESS MAP (EQUATIONS)**************************
ES0 =  /A15 * /A14 * /A13
ES1 =  /A15 * /A14 * A13
ES2 =  /A15 * A14  * /A13
ES3 =  /A15 * A14  * A13
ES4 =  A15  * /A14 * /A13
ES5 =  A15  * /A14 * A13
ES6 =  A15  * A14  * /A13
RS0 =  A15  * A14  * A13  * /A12 * /A11
CSP =  A15  * A14  * /A13 * A12  * A11
*****************************************************************************
********************ADDRESSES OF I/O PORTS**********************************
Direction Register of Port A   :        D804
Data Register of Port A        :        D806
Pin Register of Port B         :        D803
Direction Register of Port B   :        D805
Data Register of Port B        :        D807
Page Register                  :        D818
*****************************************************************************
*****************************CONFIGURATION BITS******************************
CDATA=       0      CADDRDAT   =        0
CA19/(/CSI)= 0      CALE       =        0
CRESET =     0      (/COMB)/SEP)=       0
CPAF2 =      0      CADDHLT    =        0
CSECURITY =  0      CLOT       =        1
CRRWR =      1      CEDS       =        1
CADLOG19 =   0
CPAF1[0] =   1      CPACOD[0]  =        0
CPAF1[1] =   1      CPACOD[1]  =        0
CPAF1[2] =   1      CPACOD[2]  =        0
CPAF1[3] =   1      CPACOD[3]  =        0
CPAF1[4] =   1      CPACOD[4]  =        0
CPAF1[5] =   1      CPACOD[5]  =        0
CPAF1[6] =   1      CPACOD[6]  =        0
CPAF1[7] =   1      CPACOD[7]  =        0
CPBF[0] =    1      CPBCOD[0]  =        0
CPBF[1] =    1      CPBCOD[1]  =        0
CPBF[2] =    1      CPBCOD[2]  =        0
CPBF[3] =    1      CPBCOD[3]  =        0
CPBF[4] =    1      CPBCOD[4]  =        0
CPBF[5] =    1      CPBCOD[5]  =        0
CPBF[6] =    1      CPBCOD[6]  =        0
CPBF[7] =    1      CPBCOD[7]  =        0
CPCF[0] =    1      CPCF[1]    =        1
CPCF[2] =    1
CADLOG[0] =  0      CADLOG[1]  =        0
CADLOG[2] =  0
```

REFERENCES

WSI, *Programmable Peripherals Design and Applications Handbook,* 1992.

Jeff Miller, *Using Memory Paging with the PSD3xx,* Programmable Peripheral Application Note 015.

Echelon, *NEURON CHIP Data Book*.

Echelon, *NEURON C Programmer's Guide,* 29300.

Echelon, *NEURON 3150 CHIP External Memory Interface,* LONWORKS Engineering Bulletin, January 1995.

Echelon, *LONBUILDER User's Guide,* 29200.

Echelon, *LONWORKS Custom Node Development and Engineering Bulletin,* 005–0024–01.

Motorola, *NEURON CHIP Distributed Communications and Control Processor,* MC143150, MC143120.

This application note is reprinted here with the permission of WSI, 47280 Kato Rd., Fremont, CA 94538–7333.
Phone: 510–656–5400