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Thermal Performance of Plastic Ball Grid Array (PBGA) Packages for Next Generation FSRAM Devices

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ABSTRACT

Describing the thermal performance of Plastic Ball Grid Array (PBGA) packages by the traditional Theta JA obscures the performance characteristics of the package. When the package is designed with thermal vias and "thermal balls," the package is closely coupled thermally to the printed circuit board to which it is attached. The thermal performance of the package is dominated by the thermal performance, i.e. the temperature, of the printed circuit board. Since the thermal performance of the package is so closely coupled to the board, the thermal performance, $R_{\theta JA}$, should be expressed as a function of the temperature of the board. The thermal performance of the package is modeled as the junction to board and junction to case thermal resistances. Measured data is provided to validate the techniques. Measurements were taken on the 119 lead PBGA package on single component single and 4 layer printed circuit boards and on a simulated system daughter board with 8 or 16 packages in natural and forced convection environments.

INTRODUCTION

The use of wider bus structures for the static memories used for caches is driving the need for higher lead count packages for memory devices. Additionally, the faster clock and associated rise times highlight the need for multiple power and ground leads. As a result, the memory devices used for cache memories are being packaged into the higher lead count packages such as PLCC, QFP, and PBGA packages. For the range of devices that are being considered here, the PLCC package is physically too large to be acceptable. Hence, the packages of choice are the QFP and the PBGA.

The thermal performance of a 100 lead 14 x 14 mm plastic QFP package is compared to a 119 lead 14 x 22 mm PBGA package in Figure 1. Theta JA, $R_{\theta JA}$, is measured using the procedures of SEMI[1] G38–87 using a single layer printed circuit board (76 x 114 mm) as specified in SEMI G42–88 at natural convection. Normally this value is supplemented by the thermal resistance measurements over a range of forced convection. For illustration of the differences between the two parts consider the bar chart in Figure 1 of the thermal resistance at natural convection for the parts mounted on the standard single layer printed circuit board and parts mounted on a four layer printed circuit board which is included as an extension of the SEMI specification. While the two packages have very similar thermal performance as measured on the standard single layer printed circuit board, there is a substantial difference in the performance on the four layer boards. The higher thermal conductivity of the four layer board with two solid 1 oz. planes causes more of the board to act as a heat sink. The effect is enhanced for the PBGA packages because there is metal conduction path from the die pad to the ground plane of the printed circuit board. This path has much lower thermal resistance than the equivalent path for the QFP. Hence, the PBGA package is much more closely coupled to the printed circuit board and is more sensitive to its temperature and to power dissipation in other components on the board.[2,3]

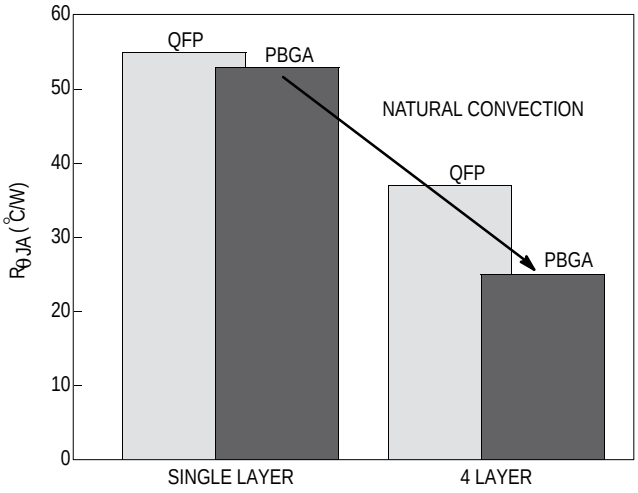

Figure 1. Type of Board on which Package is Mounted

The specific package being considered here is a 119 lead 14 x 22 mm PBGA package which is sketched in Figure 2. The thermal test vehicle packages tested for this characterization activity used a thermal die size of 4.37 x 7.32 mm (172 x 288 mil) mounted on a 7.5 x 11.1 mm die pad. There are 32 vias from the die paddle to the array of 21 thermal balls. The thermal balls are soldered to an array of pads that are connected to the ground plane in the printed circuit board with 32 vias. The planes in the circuit board are solid 1 oz. copper. Allowing the planes to be solid makes simulation easier and reflects the performance of the application boards which will have more than one ground plane.

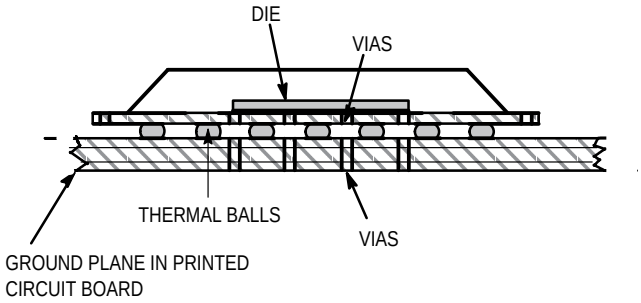

Figure 2.

This paper will address the following questions:
(1) How useful is $R_{\theta JA}$?
(2) Can the customer use the $R_{\theta JA}$ measured on a four layer-board to estimate performance on his multilayer board?
(3) How should the performance of the package be modeled?

Simplified Thermal Models for the PBGA

The heat flow in any package is actually a complicated three dimensional flow in which the path that the heat flow takes is dependent on how each of the surfaces of the package are cooled or heated by adjacent components. There are several approaches to deal with this difficulty including full finite element or finite difference models or the junction to case thermal resistance model of Bar–Cohen.[4] This paper will argue that the additional simplification of the multiple internal resistance models to only the two major thermal paths is valid based on measurement data that fits such a model. The proposed thermal model for a single component on a board is shown in Figure 3.

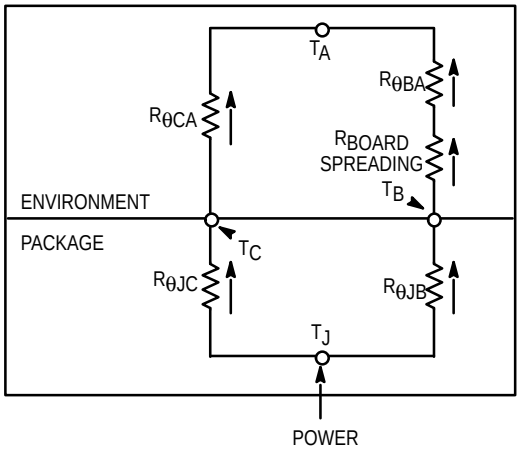

Figure 3.

In this model, the package is modeled as a junction to board thermal resistance, $R_{\theta JB}$, and a junction to case (top of package), $R_{\theta JC}$. These are the two major thermal paths from the package. The heat loss from the package to the environment is represented by the case to ambient thermal resistance, $R_{\theta CA}$; heat loss from the board is represented by a spreading resistance within the board and the board to ambient thermal resistance. For this model, the junction to ambient thermal resistance, $R_{\theta JA}$, can be calculated by series and parallel combinations of the resistance values of the model:

$$\frac{1}{R_{\theta JA}} = \frac{1}{R_{\theta JC} + R_{\theta CA}} + \frac{1}{R_{\theta JB} + R_{BS} + R_{BA}}$$

In most cases, there is not a clear separation between the spreading resistance in the board and the board to ambient thermal resistance. Usually, this equation will just be written in terms of an effective board to ambient thermal resistance.

$$\frac{1}{R_{\theta JA}} = \frac{1}{R_{\theta JC} + R_{\theta CA}} + \frac{1}{R_{\theta JB} + R_{BA}}$$

This analysis works for the single component on the board. If there are other heat sources on the board, the board temperature is not a function of only this one package. For the more general case, the effect of the other components can be represented as the temperature difference, T_{BA}, between the board and the ambient. This term, T_{BA}, is normally referred to as the board temperature rise above ambient. With this addition, the model of the package and board becomes:

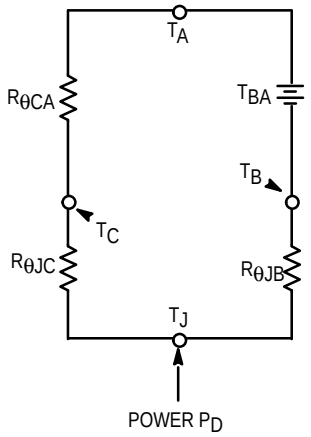

Figure 4.

This model is a simplified version of the model used by Andrews[4] with the junction to header thermal resistance neglected. If one uses this model to solve for the junction to ambient thermal resistance in terms of the thermal resistance values, board to ambient temperature rise, T_{BA}, and power P_d, then the following linear relationship is obtained:

$$R_{\theta JA} = \frac{(R_{\theta JC} + R_{\theta CA})\, R_{\theta JB}}{(R_{\theta JC} + R_{\theta CA}) + R_{\theta JB}} + \frac{(R_{\theta JC} + R_{\theta CA})}{(R_{\theta JC} + R_{\theta CA}) + R_{\theta JB}} \bullet \frac{T_{BA}}{P_D}$$

$$R_{\theta JA} = R_{\theta JA0} + S \bullet \frac{T_{BA}}{P_D}$$

This model predicts that the junction to ambient thermal resistance will be a linear function of the board temperature rise above ambient divided by the power dissipated in the component. The usefulness of the model can be verified by measuring the component thermal performance as function of the board temperature. Experimentally, this is easily accomplished using a silicone rubber heating pad under the printed circuit board. The results are shown in Figure 5.

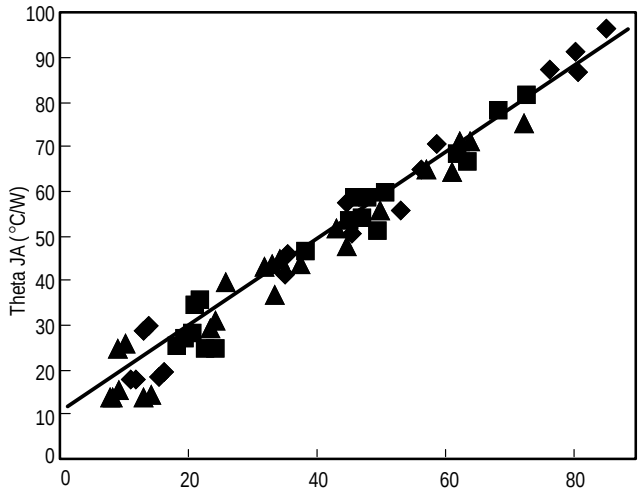

Figure 5. Board Temperature Rise Above Ambient Divided by Package Power

Measurements taken at natural convection, 1 m/s, and 2 m/sec forced convection are shown on the graph with all the data fitted to a single straight line. As predicted by our model, the thermal performance of this package is linearly dependent on the board temperature rise above ambient (divided by package power dissipation). The two resistor model of Figure 4 provides a good description of the thermal performance of the package. When an engineer is first introduced to this concept, one of the first questions is “why is the thermal performance the same at natural convection as at 2 m/s forced convection?” Actually, Theta JA is significantly different between natural convection and 2 m/s because the board temperature is significantly different. What is shown in the Figure 5 is that the junction temperature will be nearly the same at natural convection and at 2 m/s if the board temperature is the same. This would only happen if the power dissipation of the other components on the board forced the additional temperature rise in the board.

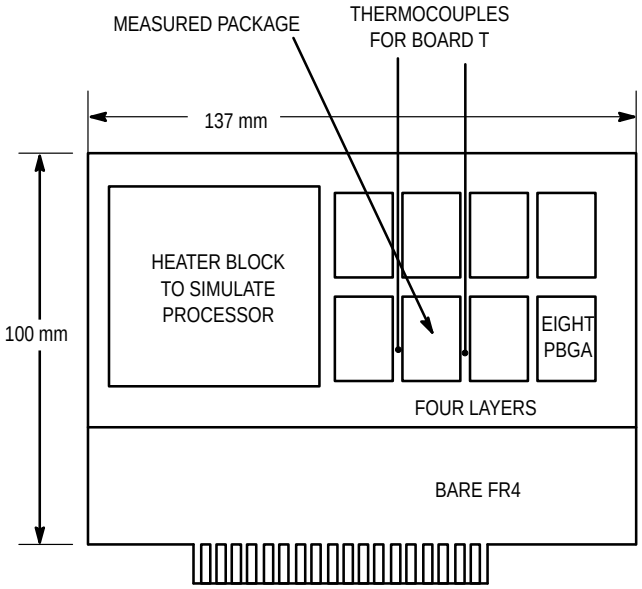

Figure 6.

This data shown above was taken with a single component on the board. The obvious question is: How well this model works in a system application? To answer this question, a simulated system daughter card was designed with an aluminum block with cartridge heaters to simulate a large microprocessor and with provisions for mounting either 8 or 16 PBGA packages. The board has an area of 69 x 137 mm that has four layers with two solid 1 oz planes. Two solid 1 oz. planes are approximately thermally equivalent to a board that would actually be used with perhaps 8 to 12 layers. The layout of the board is shown in Figure 6 with an array of 8 PBGA on one side of the board. The other 8 packages are mounted on the bottom of the board directly under the other ones. The package indicated by the arrow is the one for which data is reported; a package in the ”middle” of the array of devices was chosen because it would be representative of a typical package in middle of such an array. Junction temperatures were also measured for the other three devices in that row. The board temperature is measured with a thermocouple on each side of the package soldered into plated through holes which are connected to the ground plane. The thermal balls of the PBGA are connected to the one ground plane.

Results obtained from this board at natural convection, 0.5, 1, and 2 m/s with either 8 PBGA or 16 PBGA packages on the board powered at 1 or 2 watts each are combined with the earlier data taken on single and 4 layer boards and shown in Figure 7.

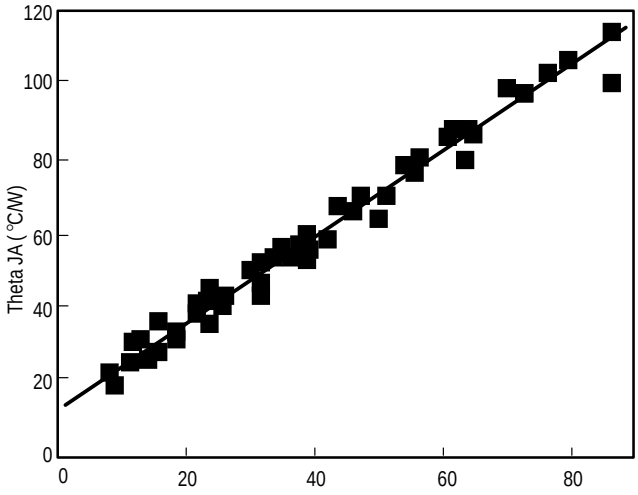

Figure 7. Board Temperature Rise Above Ambient Divided by Package Power

Again, the measured data on a wide variety of environmental conditions fit the linear relationship predicted by the two resistor model. As an example, suppose there is one watt being dissipated in the PBGA package and the board temperature has risen to 30°C above ambient. Then, one could determine from the graph that the Theta JA of the package in that environment would be 40°C/watt. As another example, suppose that the package was dissipating 2 watts and that the board temperature was 60°C above the ambient temperature. Then the board temperature rise divided by the package power would be 30 and the Theta JA would also be 40°C/watt. For an ambient temperature of 25°C, this would result in junction temperatures of 65°C and 105°C for the one and two watt examples, respectively. From this

discussion, it is evident that good thermal performance will require thermal management of the printed circuit board temperature.

While, the measured Theta JA can be plotted on the same curve for both natural convection and forced convection, a purist would point out that the percentage of heat lost between convection to the air from the package and conducted to the board will change with forced convection. In fact, if the data at natural convection and 1 m/s are separately fitted to a straight line, there will be small differences in the slope and intercept. As an example, the curve fits determined from the results with single component board are given in the following table:

	Intercept	Slope
Natural Convection	9.8	0.997
1 m/s	10.7	0.971
2 m/s	10.7	0.954

As the forced convection increases or a heat sink is placed on the package, a lower percentage of the heat is dissipated to the printed circuit board, and the junction temperature is slightly less coupled to the board temperature. For the typical range of forced convection used in desktop computers, reasonable accuracy for this package is achieved using the simplified expressions combining the results for the various conditions into a single relationship.

A more traditional way to examine the data is to use a table of Theta JA determined by a variety of techniques:

	Theta JA (°C/watt)	
Board Type	Natural Convection	1 m/s Forced Convection
Single Layer Board	52	41
4 Layer Board	24	19
8 Parts at 1 watt (System Board)	56 to 62	46 to 49
8 Parts at 2 watts (System Board)		45 to 49
16 Parts at 1 watt (System Board)	104	84

The junction temperature depends on the environment which includes the conductivity of the board and the power dissipation of surrounding components. The single component on a multilayer board represents one extreme with the other extreme represented by packages mounted closely together on both sides of the board.

The values obtained from the single component on a multilayer board would predict a lower value of the junction temperatures for most applications than would be observed in the typical case with substantial power dissipation in other devices on the board.

The doubling of the observed Theta JA when the packages are mounted on both sides of the board compared to the single sided mounting is a graphic example of the effect of the power density on the board and the resulting board temperature on the junction temperature. Mounting the packages on both sides of the board effectively halves the area available for power dissipation for each package. Incidentally, packages on the bottom of the board had very similar junction temperatures to the packages on top of the board. In natural convection at 1 watt, the package on the top of the board had a junction temperature of 121°C and the bottom package had a junction temperature of 120°C. For all practical purposes, those are identical values. This is explained by the close coupling of the junction temperatures to the board temperature which will be the same for the two packages mounted on opposite sides of the board.

The traditional Theta JA is useful for comparing package performance and as a preliminary estimate to determine whether further analysis is needed. It gives no information to account for the range of thermal performance given as examples in the table above.

The other frequently asked question about this formalism is: How is the board temperature determined? The effective doubling of the Theta JA when the packages are mounted on opposite sides of the board clearly indicates that historical board temperatures could be wrong. The answer to the determination of the board temperature is that a full board level thermal simulation will be required to determine both the thermal performance of the printed circuit board and the performance of each of the packages. There are a number of commercial software codes[6–8] that perform a board level thermal solution with varying degrees of sophistication. These range in sophistication from the 2 1/2 dimensional finite difference or finite element codes to the computational fluid dynamics codes that simultaneously solve the conduction and the fluid flow convection. For all these simulation codes, a simplified thermal model for the package is required. From a component manufacturer's viewpoint, a simple, general purpose model which could be broadly applied would be most helpful. It is our contention that the reduction of the measured data to a single straight line as predicted by the model demonstrates that the two resistor model meets the need for a reasonably accurate description of thermal performance. A proposed method for obtaining that model will be described in the following section.

CONDUCTION MEASUREMENTS TO DETERMINE PACKAGE MODELS

Having determined that the two resistor model will adequately describe the thermal performance, a method for obtaining the values in those models will be discussed. One of the basic premises is that the package model should describe the package behavior. As an example, the package model should not provide a case to ambient thermal resistance because it is not a package characteristic. The case to ambient thermal resistance is a function of whether natural convection can occur in a closed environment, degree of turbulence in forced convection, whether a heat sink is used, etc. Instead, the package model will provide a junction to case thermal resistance. The next level modeling tool can work from that junction to case thermal resistance to determine the total thermal resistance through the top of the case whether a heat sink is used or normal convection environments.

Unfortunately, there are several junction to case formalisms in use. The most confusing is the junction to all surfaces of the case thermal resistance as determined by the junction to a liquid bath measurement which is described in SEMI specification G43–87. One of the board level modeling tools uses this value coupled with the lead resistance as the junction to board measurement. Our position is that this definition is not extensible to the ceramic packages or thermally

enhanced packages on which a heat sink is likely to be used. Instead, the definition taken from the JEDEC[9] committee is used: The junction to case thermal resistance of a package is defined to be “the thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface.” Hence, the junction to case thermal resistance is the thermal resistance of the path from the junction to the surface on which a heat sink might be placed. As a result, the junction to case thermal resistance is the thermal resistance from the junction to the top surface of the PBGA. It is determined using a cold plate (infinite heat sink) to force “all” the heat to travel from the junction to the case of the package. The methods for making this measurement are described in the industry specifications: MIL–STD 883D, Method 1012.1 and SEMI G30–88. We deviate from the industry specifications in that the temperature of the cold plate is used instead of the case temperature. All of the techniques to put a thermocouple on the surface of the case using holes or slots in the cold plate or in the case itself will yield a warmer measurement and hence a more optimistic measure of the thermal resistance. Using the cold plate temperature as the “case” temperature creates a slightly conservative result.

A method for determining a junction to board thermal resistance is not defined in the industry. Of the suggestions that have been proposed, the most direct and simple method is the following: The package is soldered to a multilayer printed circuit board with solid power and ground planes to achieve a high thermal conductivity in the x–y plane. The higher thermal conductivity improves the accuracy of the measurement by minimizing the temperature gradients in the vicinity of the package while it is being tested. Any “thermal balls” are connected with vias to the ground plane within the printed circuit board. The printed circuit board is needed for the measurement to provide an easy method to make the necessary electrical connections to the package for the test. The component and printed circuit board are placed on the cold plate as shown in Figure 8 using thermal grease to minimize the thermal resistance between the board and the cold plate.

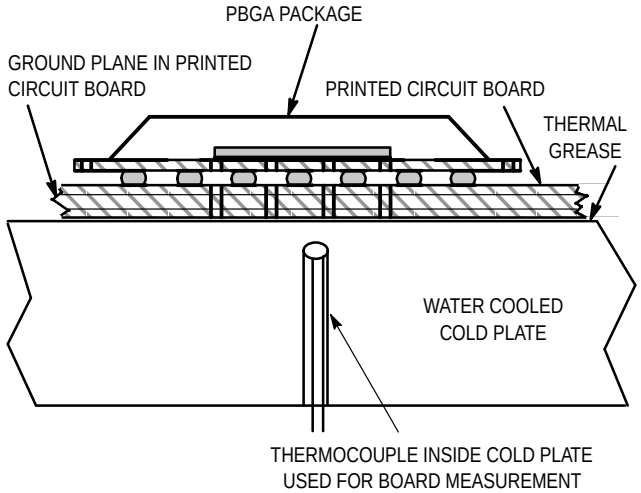

Figure 8.

The junction to board thermal resistance, $R_{\theta JB}$, is then determined by

$$R_{\theta JB} = \frac{(T_J - T_B)}{P}$$

where T_J and T_B are the junction and board temperatures respectively, and P is the power dissipated in the package. Again, a more consistent measurement is obtained by using the cold plate temperature as the board temperature.

The usefulness of the technique can be judged by comparing the junction to board thermal resistance results obtained by the slope and intercept of that data fitted to the two resistor model to the junction to board thermal resistance determined by the cold plate technique. For the two resistor model, the junction to board thermal resistance is determined from the data obtained by the straight line fitted to the data in Figure 7 by the relationship:

$$R_{\theta JB} = \frac{R_{\theta JA0}}{S}$$

To make the judgment easier, the results were compared for the 119 lead 14 x 22 mm, 225 lead 27 x 27mm, and the 357 lead 25 x 25 mm PBGA. The following table gives the junction to board thermal resistance as determined by the two methods for the three different PBGA packages:

Package	Two ResistorModel	Cold Plate
119 Lead	9.8	10.8
225 Lead	8.3	7.4
357 Lead	6.6	7.3

As can be seen, the two methods give a result that is within 1°C/watt. Hence, the choice of techniques should be determined by ease of use except for those cases where testing under the actual heat flow paths is necessary. Testing using actual application environments is appropriate for cases at the conditions of extreme power dissipation or unusual heat sink and convection configurations.

The cold plate method for determining the junction to board thermal resistance is quicker and easier since it is a relatively quick single point measurement instead of requiring some 4 to 8 wind tunnel measurements per sample tested. If it was necessary to test all parts using the two resistor model in the wind tunnel, more wind tunnels would be required within Motorola to meet the package test needs. More importantly, the cold plate technique represents a relatively easy environment to duplicate in simulation to verify the accuracy of simplified models being used in board level simulations. It is also a much easier test environment to explain to a customer.

CONCLUSION

Theta JA determined by the traditional methods provides a comparison of the thermal performance of a package. To be useful to calculate junction temperature, it must be referenced to the board temperature on which the package is mounted. Especially with the PBGA packages, the thermal performance is largely determined by the board temperature to which the package is mounted.

The two resistor thermal model is a simplification of the actual thermal performance of the package, but has been shown to provide an adequate description of the performance of the package over a wide range of environments. The components of the two resistor model can be measured or simulated using the cold plate environment to force essentially all of the heat flow along the path being measured. We are proposing that this two resistor model be made available to designers for use in board level modeling tools for their determination of the board temperatures, Theta JA, and junction temperatures in their application environment.

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7. Pacific Numerix, Scottsdale, AZ.
8. FLOTHERM, Flomerics, Westborough, MA.
9. JEDEC JC15.1 committee is currently writing specification for thermal characterization of surface mount integrated circuits.

NOTES

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