AN1209

The Motorola BurstRAM™

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This note introduces the MCM62486 32K x 9 Synchronous BurstRAM. The device was designed to provide a high-performance, secondary cache for the Intel i486™ microprocessor and future microprocessors with burst protocol. Four of these devices can supply a 128K byte direct-mapped bursting cache with parity support.

THE MCM62486

The 62486 is a synchronous device with input registers and address counters surrounding a standard 32K x 9 FSRAM core. The additional circuitry in the periphery enables the memory to uniquely interface with the i486. Like the i486, the timings are referenced to the rising edge of the clock (K). Signals generated by the processor and control logic must be stable during all transitions of clock from low to high. Output enable ($\overline{G}$) on the 62486 is the only asynchronous input.

The 62486 contains three burst-control inputs. They are $\overline{ADV}$, $\overline{ADSC}$, and $\overline{ADSP}$. These inputs are used by the cache controller to control the burst capabilities of the 62486 and to maintain synchronization with the i486 or other logic driving the cache.

USE WITH THE i486 PROCESSOR

The 62486 requires an ASIC or discrete PAL type of cache controller to work with the i486. This cache control logic must also include 8K x 16 of cache-tag comparator RAM and any other buffers needed for system operation.

Control signals are sourced as follows: K is driven by the system clock (CLK); $\overline{ADSP}$ is an output from the microprocessor; and $\overline{ADV}$, $\overline{ADSC}$ are generated from the cache control logic. The data bus and lower address bus may interface directly with the 62486 or the address bus may be buffered to improve its drive to the rest of the system. A simple block diagram of this setup is shown in Figure 2.

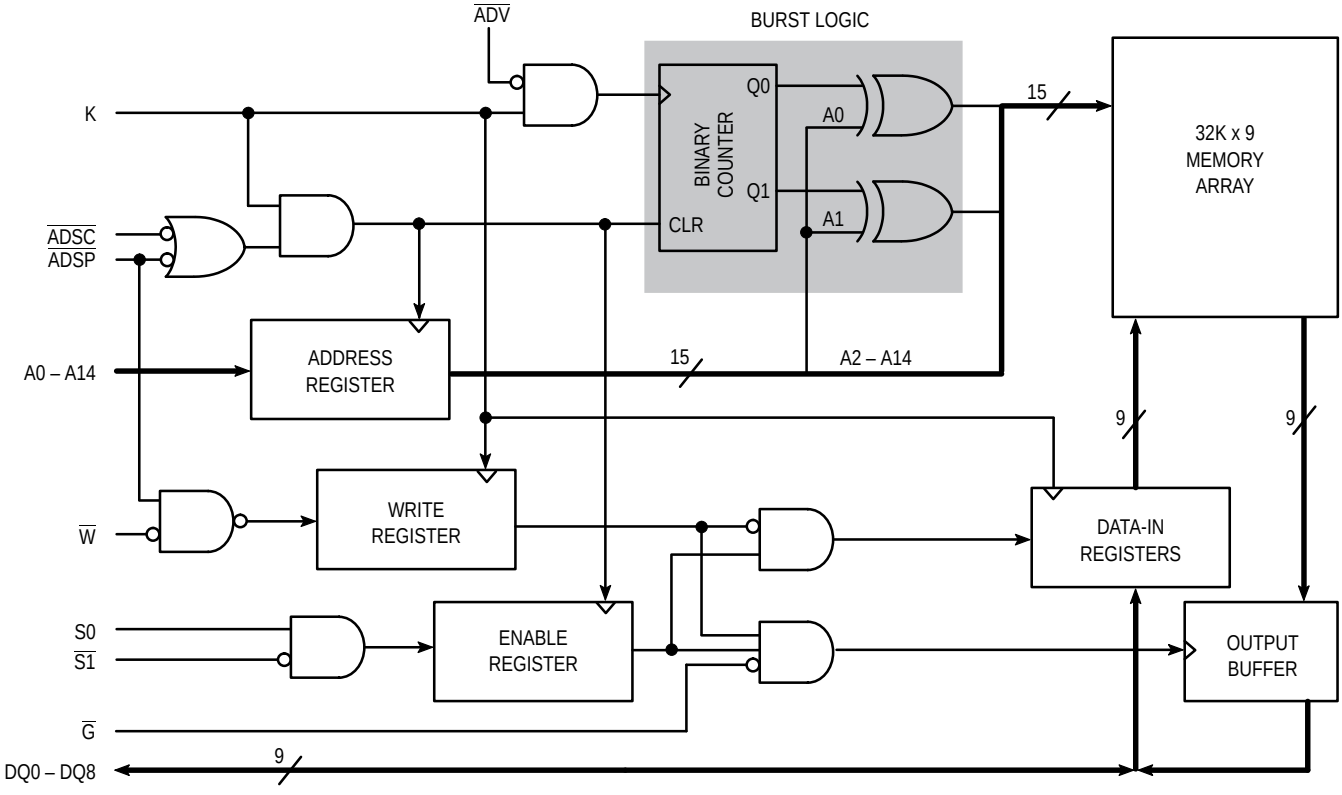

Figure 1. MCM62486 Block Diagram

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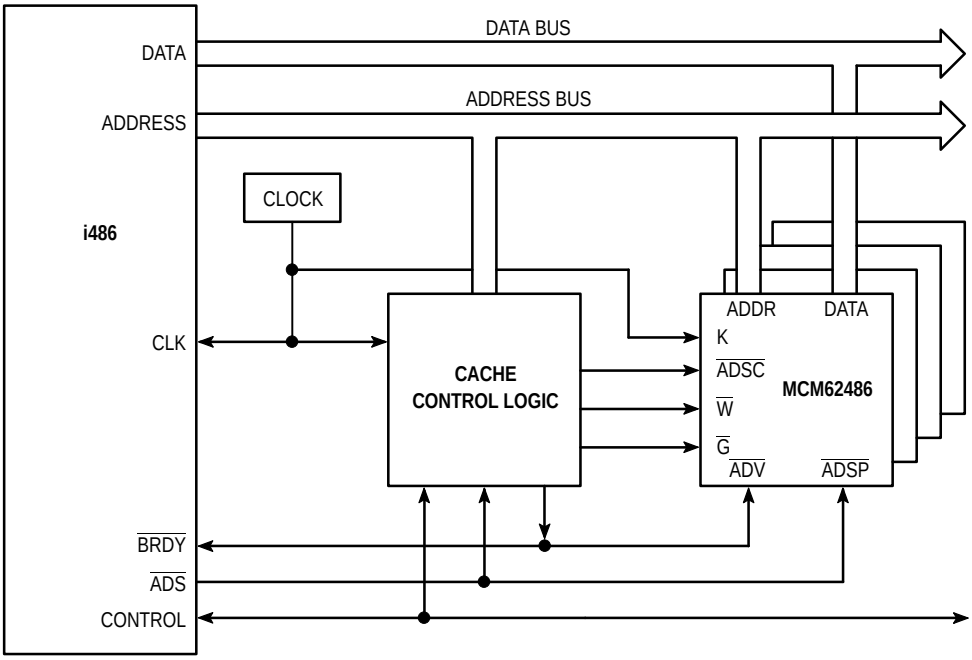


Figure 2. Typical System Block Diagram

INPUT PINS OF THE MCM62486

K is the clock input of the 62486. This should be tied to the system clock.

ADSP is one of two address status input pins that are supplied on the 62486. This input allows the microprocessor to initiate a cache bus cycle. For every processor access, to or from memory, the i486 will assert ADS for one transition of K from low to high. If ADS from the i486 is tied to ADSP on the 62486, the 62486 will register the correct address from the processor. During all "T2" cycles on the i486, ADS and ADSP should not be asserted as described in the i486 processor user manual.

ADSC is the second of two address status input pins supplied on the 62486. This input allows external logic to initiate or continue cache bus cycles. The purpose of this input is to give the cache controller its own input to regulate cache accesses. This gives the 62486 a good deal of system design flexibility. One use of ADSC is for burst extension. After four burst accesses have been generated by the 62486, the cache controller may supply an additional base address to continue the burst. This method works well with 72 bit data buses. This pin can also be used in a similar manner to facilitate a cache fill from other sources.

ADV is the burst advance input pin supplied on the 62486. The purpose of this pin is to acknowledge a successful read-from or write-to memory as determined by the cache control logic. The 62486 may then proceed to the next address. This input is a function of T2 (T2 cycle as defined by the i486 processor manual), KEN (from the processor), MATCH (from the cache tags), READ (from the processor) and MISS (a cacheable read miss from the control logic).

W is the synchronous write input pin supplied on the 62486. This signal must be valid for every clock cycle ADSP is not asserted.

A0 – A14 are the synchronous address pins supplied on the 62486. These must be valid for the transitions of K from low to high. If neither ADSC or ADSP is negated, or if the chip is deselected, the address inputs do not need to meet the required setup/hold times. For all other read/write operations, the setup/hold times **MUST** be met.

S0 and S1 are the synchronous chip selects supplied on the 62486. These must be valid whenever the addresses are required valid. These inputs can be used for address depth expansion without any external logic.

G is the asynchronous output enable supplied on the 62486. This pin changes the outputs from high impedance to active at any time that the SRAM is selected.

CACHE OPERATION

READ CYCLES

Cache operations of the 62486 are initiated with one of the two Address Status Pins mentioned. Figure 3 shows the read cycle timings when ADSP is tied to ADS. During the first cycle (T1) the i486 supplies an address and asserts ADS low. The 62486 responds to ADSP being asserted by registering the lower 15 addresses. The 62486 begins to perform a read access regardless of the state of its W input.3

During the next cycle (T2), the cache controller determines if the read access was a cache hit. If so, the controller should assert G and ADV on the 62486 as well as BRDY on the i486. The assertion of G will allow the 62486 to drive the data onto the data bus while BRDY will inform the processor that the data is correct. The assertion of ADV will cause the 62486 to begin on the next burst access. Subsequent burst access will be available without wait states in a similar fashion.

Single, non-burst reads behave in a similar manner as the first access of a read burst.

Note for timing diagrams: Q1, Q2, Q3, Q4 represent the data output from the first address (base address), second, third and fourth address. For example, if A in Figure 3 was #000C, Q1 would be the data from #000C, Q2 from #0008, Q3 from #0004 and Q4 from #0000. (This is the same burst sequence as in **Table 7.7. Burst Order** in the *i486 Microprocessor Data Book*).

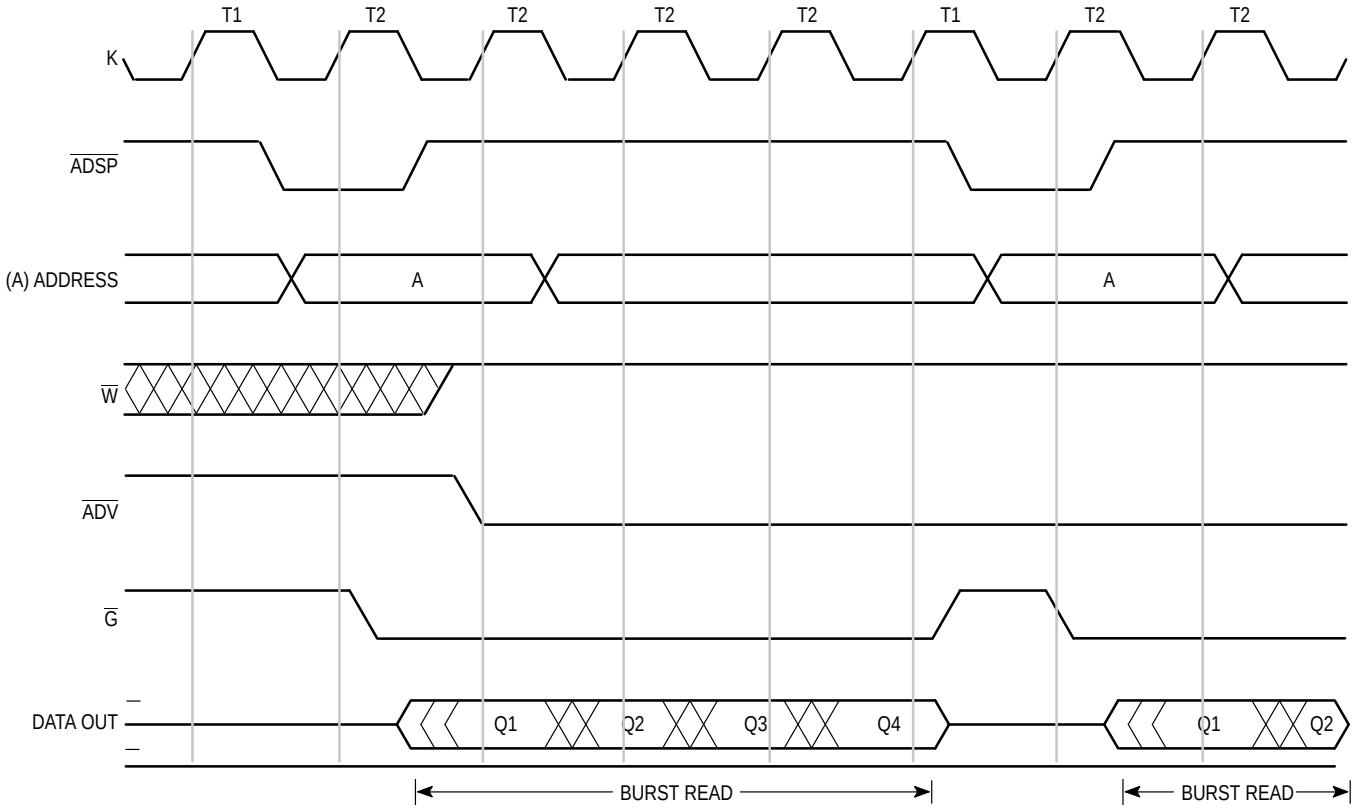


Figure 3. Cache Read Cycles

WRITE CYCLES

For a write to cache access, the initial T1 cycle will be the same as above. During the T2 cycle, the cache controller should assert $\overline{W}$ instead of $\overline{G}$. This will allow the 62486 to receive the data from the i486 and write it to memory. The i486 can burst write for 8 and 16 bit operations. The 62486 can support this action as described in the 62486 data sheet and Figure 4.

ADDRESS BUS LOADING

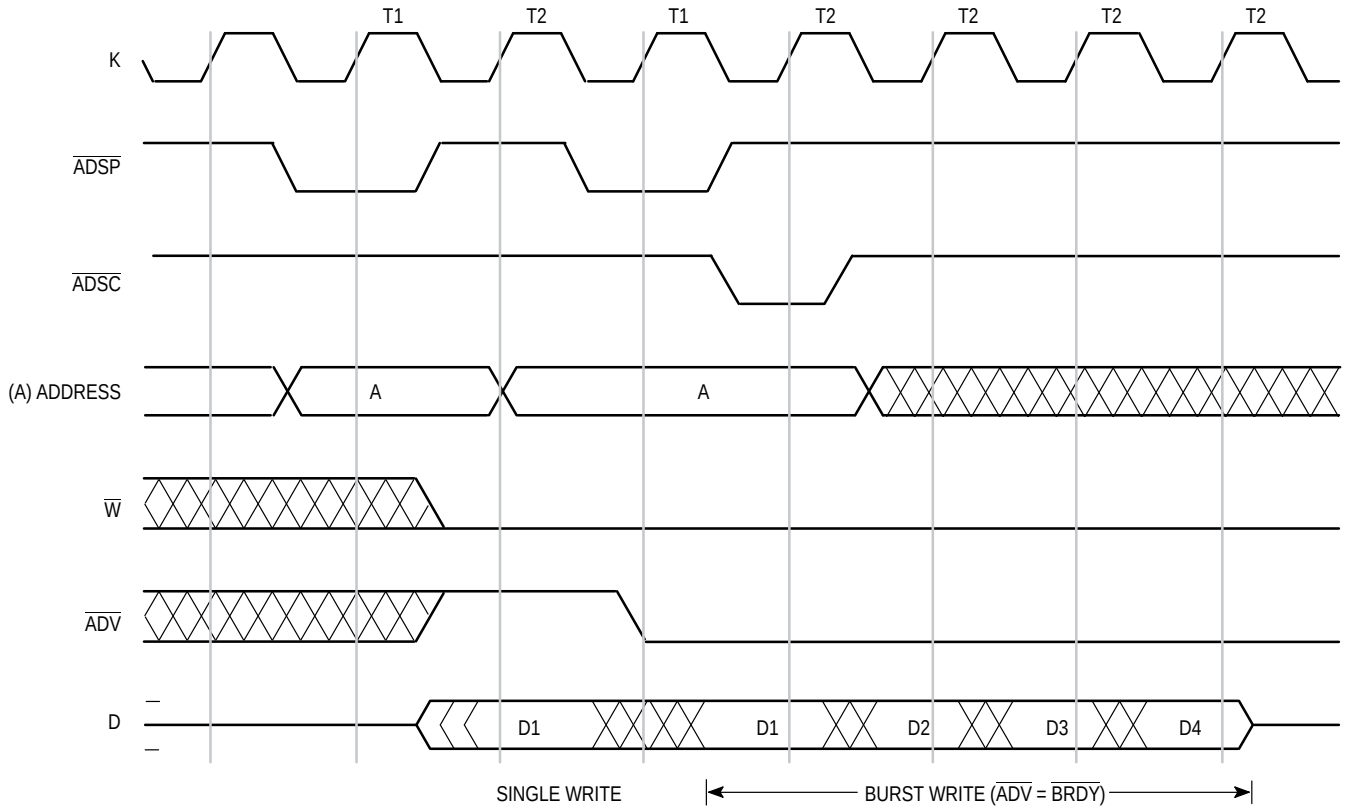
The 62486 has setup and hold timing that allow address buffers to be placed between the SRAM and the processor. The i486 is specified with 50 pF loads. Since the 62486 has a typical input capacitance of 2 pF, the i486 can be run without the buffer assuming the cache tags and other circuitry do not overload the bus.

ADVANTAGES OF THE 62486 OVER OTHER FSRAM SOLUTIONS

The 62486 is meant to replace a standard 32K x 9 FSRAM as well as some external logic. By incorporating this logic and RAM onto one chip, the system designer is given more board space, less power consumption, and most of all, easier design timing requirements. At 33 MHz, a discrete logic/SRAM solution would require a 7 ns PAL (for the burst counter) and an 18 ns SRAM [30 ns (period) – 5 ns (i486 setup) – 7 ns (PAL) = 18 ns].

This timing is even more difficult in write cycles. Closer examination of writes shows that the write signal and data from the processor do not correspond with the requirements of a standard 32K x 9 SRAM. A self-timed write SRAM is essential for high performance systems.

The 62486 represents the JEDEC standard for a 32K x 9 Synchronous SRAM for the i486. This pin-out provides enough power and ground pins to allow these devices to support systems running 50 MHz and faster. Also the 62486 represents the standard functionality descriptions for $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$. These same pins are used in the JEDEC standard 64K x 18 SRAM to be used with the i486 and the “P5”.



NOTE: The first T1/T2 cycle is a single write operation. This works the same as the first two cycles of a burst write. In this single write operation, $\overline{ADV}$ goes high for the T2 cycle, while the $\overline{RDY}$ signals on the processor must be asserted low. In this operation, the $\overline{ADV}$ and $\overline{RDY}$ signals behave differently. To match their behavior, examine the second T1/T2 cycles. This second write operation (the burst write) shows how the $\overline{ADV}$ signal may behave like the $\overline{RDY}$ signals. Note that the $\overline{ADSC}$ is asserted for the first T2 cycle, thereby reloading the base address. Had the $\overline{ADSC}$ remained high for this cycle, the data (D1) would have been incorrectly written to the second burst address. This second write operation shows both single and burst write operations with $\overline{ADV}$ and $\overline{RDY}$ both asserted low for all T2 cycles.

Figure 4. Cache Write Cycles

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