

# AN1004 APPLICATION NOTE

# WRITE PROTECT FUNCTION for 2Mb and 4Mb BOOT BLOCK FLASH MEMORIES

#### INTRODUCTION

The performance of the 2Mb and 4Mb Dual Voltage Boot Block Flash memories, M28F220, M28F420, M28F411, M28W431 has been enhanced by the introduction of a Boot Block Write Protect function using the WP pin.

This new function is coupled with the introduction of the SGS-THOMSON 20% shrink generation of the CMOS T6  $0.6\mu$  flash process (CMOS T6-U20).

The application note deals about the impact for existing and new boards designs.

The introduction of this new feature permits the optimization, cost and functionnality of existing and new designs by removing the circuitry overhead previously required to unprotect the Boot Block.

The new version of 2Mb and 4Mb Flash memories from SGS-THOMSON bring added application flexibility and functionality in line with the Intel SmartVoltage<sup>™</sup> products.

#### PRODUCTS

The generic part numbers impacted are listed in Table 1. The change applies for all speed classes, package options and temperature ranges.

The WP function has been introduced on the products taking into consideration their compatibility with Intel SmartVoltage™ products.

On TSOP40 package the  $\overline{WP}$  is located on pin 12; on SO44 it is located on pin 2; on TSOP48 it is located on pin 14. The new products pinouts are described in the Figures 1 to 6.

	Top Boot Block		Bottom Boot Block	
	5V/12V	3V/12V	5V/12V	
2Mb (x8,x16)	N. A.	N.A.	M28F220	
4Mb (x8)	M28F411	M28W431	N.A.	
4Mb (x8,x16)	M28F410	N.A.	M28F420	

#### Table 1. The Dual Voltage Boot Block Flash Memory Products

# **AN1004 - APPLICATION NOTE**



#### Figure 1. 2Mb (x8,x16) TSOP Pin Connections





Warning: NC = Not Connected.

44 🗖 RP 11) 43 🗖 W 42 🗖 A8 A7 🗖 4 41 🗖 A9 40 A10 A6 🗖 5 39 🗆 A11 A5 🗖 6 A4 🗖 7 38 🗖 A12 🗖 A13 A3 🗖 8 37 -19 🗖 A14 A2 🗖 36 110 35 ⊐ A15 A1 🗖 A0 🗖 11 34 🗖 A16 M28F220 Ē 🗖 12 33 BYTE

32 VSS

30

29

28 E

AI01299B

31 DQ15A-1

DQ7

**\_\_** DQ14

DQ6

27 DQ13

26 DQ5

25 DQ12

24 🗖 DQ4

23 VCC

#### Warning: NC = Not Connected.

V<sub>SS</sub> 🗖 13

DQ0 - 15

DQ9 - 18

DQ2 - 19

DQ10 20

DQ3 21

DQ11 22

DQ8

DQ1

16

17

Figure 4. 4Mb (x8,x16) SO Pin Connections



**S** 

Figure 2. 2Mb (x8,x16) SO Pin Connections

# **BLOCK PROTECTION SCHEME**

The blocks protection scheme, previously ensured by VPP and RP pins is now enhanced by the presence of the WP pin. The memory blocks protection thruth table, in Table 2, explains how the various blocks are protected or unprotected.

The new possible configuration offered by the  $\overline{WP}$  pin is highlighted in the table.

Table 2.	Memory	Blocks	Protection	Truth	Table
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V <sub>PP</sub>	RP	WP	Boot Block	Other Blocks
V <sub>PPL</sub>	Х	х	Protected	Protected
Vpph	VIL	Х	Protected	Protected
V <sub>PPH</sub>	V <sub>IH</sub>	VIL	Protected	Unprotected
Vpph	VIH	VIH	Unprotected	Unprotected
V <sub>PPH</sub>	V <sub>HH</sub>	х	Unprotected	Unprotected

Notes: <u>X'</u> = Don't Care RP is the Reset/Power Down/ Boot Block Unlock tri-level input.

 $V_{\text{PP}}$  is the program or erase supply voltage.

 $V_{IH}/V_{IL}$  are logic high and low levels.  $V_{HH}$  is specified from 11.4V to 13V.

V<sub>PPH</sub> is specified from 11.4V to 12.6V.

# THE WP FUNCTION

The connection change with respect to the previous version of the products is described in Table 3.

When VPP is at VPPL, the whole chip is protected and no write operation is possible. Write operations are permitted only with VPP at VPPH, specified from 11.4V to 12.6V, and the Write protect input works as described in Table 4.

More detailed information about the blocks protection scheme is available from the individual products datasheets. Please refer to those documents for a complete understanding.

# Table 3. WP Function and Pin Changes

Package	Pin Number	Previous Connection	New Connection	Intel Connection
TSOP40	12	DU	WP	WP#
SO44	2	DU	WP	WP#
TSOP48	14	NC	WP	WP#

Notes: DU = Don't Use. NC = Not Connected

#### **Table 4. Write Protect Pin Function**

VPP	WP Level	Description
Vpph	V <sub>IH</sub> or V <sub>CC</sub>	The boot block is unprotected $\overline{RP}$ can be either V <sub>IH</sub> or V <sub>HH</sub>
V <sub>PPH</sub>	V <sub>IL</sub> or V <sub>SS</sub>	The boot block is protected or unprotected depending on $\overline{RP}$ level
Vpph	Not Connected	The boot block protection is undetermined

## IMPACT AT THE APPLICATION LEVEL

The consequences of the implementation of the  $\overline{WP}$  function on the 2Mb and 4Mb Boot Block Flash memories allow designers to optimise the applications and reduce the cost of their board.

**Cost reduction.** The implementation of the  $\overline{WP}$  pin to unprotect the Boot Block is possible with a standard logical level, whereas it was previously necessary to have a V<sub>HH</sub> level (Specified from 11.4V to 13.0V) on the  $\overline{RP}$  pin to have the same function. Practically, this means that the circuitry needed to bring this V<sub>HH</sub> level to  $\overline{RP}$  can be removed. This circuitry could be as simple as a pull up to 12V or more elaborated like a full switch and its associated logic.

**Performance enhancement.** The introduction of the  $\overline{WP}$  now allows programming and erasure of the Boot Block in those applications that could not afford the additionnal circuitry needed to set  $\overline{RP}$  at V<sub>HH</sub>. On already developed boards, where the modifications are not wished, a check of the current connections of  $\overline{WP}$  pin should be carried out. An evaluation of the possible consequences based on this application note is recommended. In case  $\overline{WP}$  pin is not connected, the memory will operate the same way in read and write mode. The Boot Block protection will be undetermined as per Table 4.

5

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# **AN1004 - APPLICATION NOTE**

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