APPLICATION NOTE

AN051

Philips PLDs support live insertion applications

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There is an increasing demand for circuit boards that can be inserted into and extracted from a powered and operating system, without the need of switching off the power supply. Live insertion, hot injection, or hot swapping all refer to the insertion of an unpowered module onto a powered and active system bus. This feature is important in applications such as telecommunications, where circuit boards are frequently inserted into and removed from live systems; in power management applications, where a subsystem is turned off and then re-started in order to save power or increase battery life; and in fault tolerant systems, where problem boards are replaced without interruption to the system.

Careful attention must be given to all components incorporated in live insertion application designs. Philips has placed a great deal of consideration in the design and manufacturing of PLDs that meet the demands of such designs. This application note discusses the influence of programmable logic in live insertion applications, clarifies bus errors that can occur, and examines other important considerations when designing for live insertion.

Possible Problems

During live insertion, there are basically two types of bus errors that can occur—bus contention and bus glitches. Bus contention can occur during live insertion if the I/O of the board being inserted forces the opposite logic state from the existing bus logic state, or clamps the bus to V_{CC} or ground through internal structures such as intentional or parasitic forward-biasing diodes or resistors. Bus glitches are due to the capacitance on the circuit board charging or discharging through the line impedance on the system bus during live insertion. Depending on the amplitude and pulse width, glitches may be misinterpreted as relevant data that could upset bus operation. Both of these conditions must be eliminated in order to ensure a design that functions properly in live insertion applications.

Definite Solutions

Designed to prevent bus contention and glitches, the outputs of the Philips LVT22V10, LVT16V8, ABT22V10A5 and ABT22V10A7 PLDs are forced into a 3-State (high impedance) condition until V_{CC} reaches a predetermined level. In Figure 1, you can see that V_{CC} is applied to a power-up reset circuit. The output of the block diagram is logic 1 until V_{CC} reaches a level of 2.1 Volts, when V_{CC} reaches 2.1 Volts or greater, the output of the power-up reset circuit switches to a logic 0. Since the NOR-gate takes its inputs from the output of the power-up reset circuit and from the output enable pin, the output of the NOR-gate is now determined by the logic level of the $\overline{OE}$ pin. If the $\overline{OE}$ pin is active, (logic 0), then the output of the NOR-gate will be logic 1, which would in turn enable the output buffer and allow data to be propagated onto the bus. This technique assures that the outputs are completely isolated during the live insertion process and during the power-up and power-down procedure of a system utilizing power management methods.

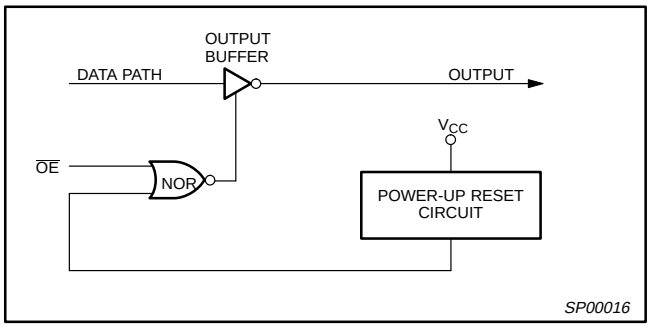

Figure 1. Block Diagram of Power-Up Reset Circuit and 3-State Output

Figure 2 elaborates on the power-up reset circuit described above. This circuit utilizes a bipolar transistor (T1) and two simple diodes (D1 and D2). During power-up, whether it be a switch that has been turned on or the instant that the V_{CC} and ground pins of an inserted board have made contact with the system's power terminals, the voltage starts its ramp-up from 0V to the V_{CC} value applied to the system. The transistor (T1) is not turned on until V_{CC} reaches a value equal to two diode drops (0.7V each) plus the 0.7V V_{BE} of the transistor, which is approximately 2.1V. Until the transistor is turned on, the power-up reset circuit output remains high (~V_{CC}), disabling the output of the NOR-gate shown in Figure 2. Once V_{CC} reaches 2.1V, the transistor turns on pulling the output down to V_{CE} of transistor T1, which is approximately 0.2V.

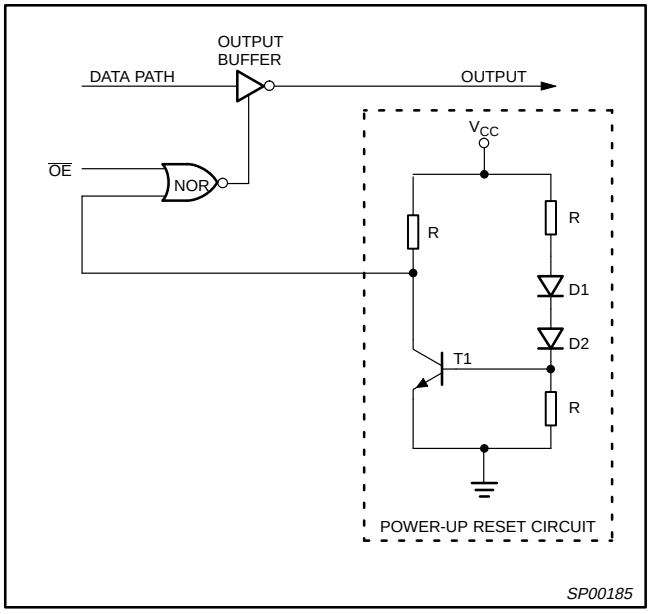

Figure 2. The Power-Up Reset Circuit Explained

Another common culprit of bus errors can be found in design architectures that incorporate intentional or parasitic paths between I/O pins and ground or V_{CC}. Philips Semiconductors 5V ABT Programmable Logic Devices utilize a bipolar output driver design that excludes the use of any intentional or parasitic forward-biasing diodes or resistors between I/O pins and V_{CC} or ground, thereby eliminating internal structures that could provide a path that would allow the bus to be clamped to V_{CC} or ground, resulting in bus contention. The Philips Semiconductors 3V LVT Programmable Logic family incorporates basically the same output driver design, however, it does include a parasitic diode junction between outputs and V_{CC} in order to accommodate rail-to-rail switching from 0V to 3.3V. Therefore, the design also incorporates a Schottky diode that blocks the parasitic diodes cathode, preventing the flow of current from all of the outputs to V_{CC}. These diodes are not forward-biased and are therefore irrelevant as far as bus contentions is concerned.

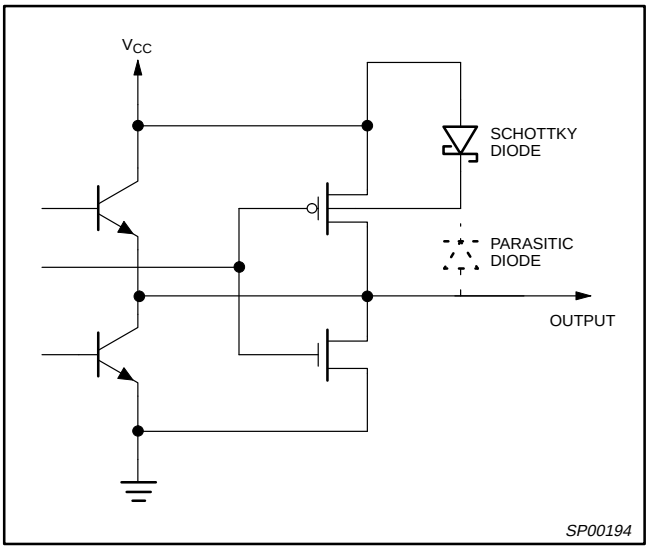

Figure 3. Parasitic and Schottky Diodes in the Output Stage

Summary

Philips Semiconductors is dedicated to providing our customers with the semiconductors that solve today's design challenges. We recognize the need for programmable logic devices that support both 5V and 3V designs. The LVT22V10, LVT16V8, ABT22V10A5, and ABT22V10A7 provide designers with a cost competitive means of achieving live insertion designs free from bus errors. Our BiCMOS QUBiC process allows us to manufacture PLDs that are ideal for use in live insertion applications by preventing outputs from being propagated onto the bus during power-up and power-down transitions, thereby eliminating any chance of bus errors due to bus contention or bus glitching.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381