APPLICATION NOTE

TJA1050
CAN High-Speed Transceiver

AN00020

Philips Semiconductors

PHILIPS

Abstract

The TJA1050 is an advanced CAN transceiver for use in automotive and general industrial applications. It supports the differential bus signal representation being described in the international standard for in-vehicle CAN high-speed applications (ISO11898). Controller Area Network (CAN) is a serial bus protocol being primarily intended for transmission of control related data between a number of bus nodes.

This application note provides information how to use the TJA1050 in CAN high-speed applications.

APPLICATION NOTE

TJA1050
CAN High-Speed Transceiver

AN00020

Author(s):
Thomas Suermann

Philips Semiconductors
Systems Laboratory Hamburg
Germany

Keywords

Transceiver, ISO11898, Physical Layer,
EMC, TJA1050, PCA82C250,
Controller Area Network (CAN)

Number of pages : 31

Date: 00-04-25

Summary

This report is intended to provide basic technical information on the implementation of the Physical Medium Attachment in a CAN network according to the ISO11898 standard, using the transceiver TJA1050 from Philips Semiconductors. This product supports bit rates up to 1Mbit/s over a two-wire differential bus line, which is the transmission medium being specified by the ISO11898 standard.

The report provides typical application information like aspects of EMC, supply voltage buffering, ground-offsets, unpowered transceiver, bus length and maximum number of nodes per network.

Contents

1. INTRODUCTION

ISO 11898 [1] is the international standard for in-vehicle high-speed communication using the Controller Area Network (CAN) bus protocol. The scope of this standard essentially is to specify the so-called Data Link Layer and Physical Layer of the communication link. The Physical Layer is subdivided into three sublayers as shown in Figure 1.1. These are:

- Physical Signalling bit coding, timing, synchronization
- Physical Medium Attachment driver and receiver characteristics
- Medium Dependent Interface bus connector

The implementation of the Physical Signalling Sublayer and the Data Link Layer is typically performed by integrated protocol controller products, like the SJA1000 [2] from Philips Semiconductors. The Physical Medium Attachment, interfacing the protocol controller to the physical transmission medium, is provided by transceiver products like the TJA1050 [3] or PCA82C250 [4] from Philips Semiconductors. This report focuses on the implementation of the Physical Medium Attachment Sublayer using the transceiver TJA1050.

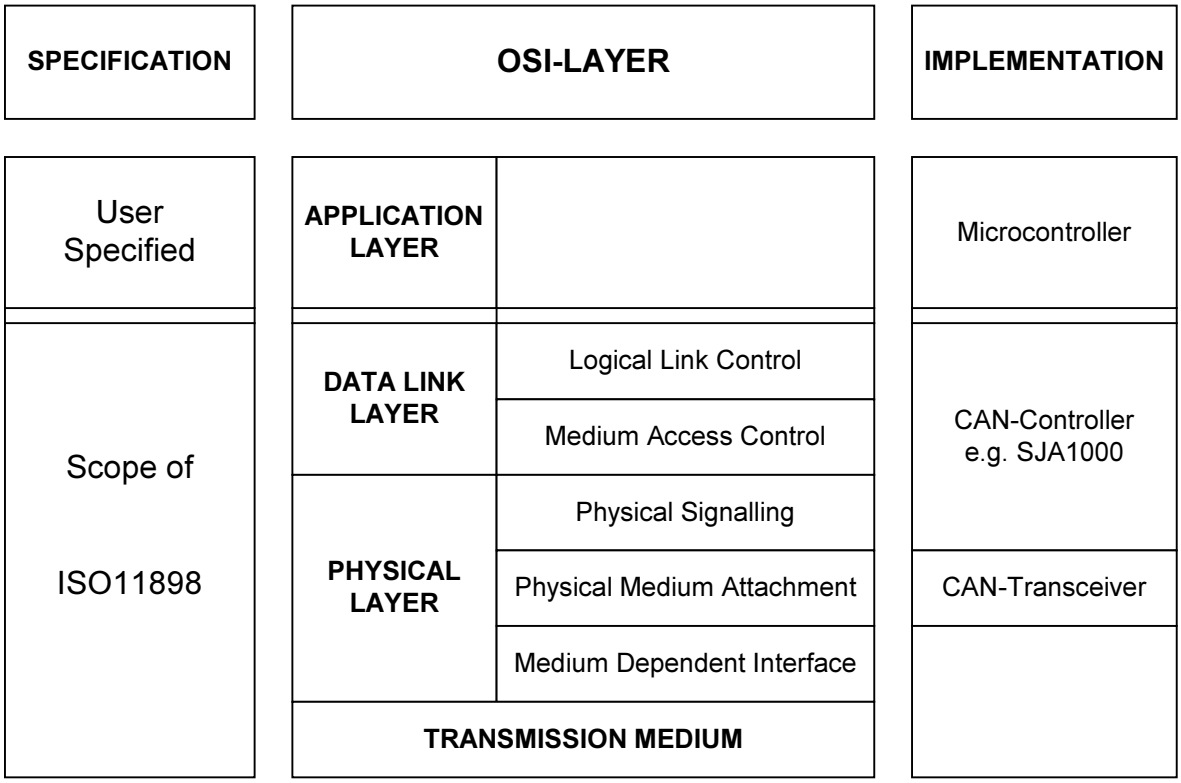

Figure 1.1 : Layered architecture of CAN

Like the PCA82C250, the TJA1050 is compatible to the ISO11898 standard. Thus, interoperability with other ISO11898 compliant transceiver products is ensured.

Electromagnetic Compatibility (EMC) has been the main design target of the TJA1050. Considering the critical AM-band, emission could be decreased by more than 20dB compared to the PCA82C250.

Besides EMC, another key item of the TJA1050 is its passive behaviour to the bus if unpowered. This makes the TJA1050 the preferred transceiver for clamp-15 nodes, which are unpowered when ignition is off. Continuously supplied nodes (Clamp-30) require a dedicated low-power mode in order to keep the overall system power consumption as low as possible. For these applications the PCA82C250 remains a good choice because of its standby mode. Very low power consumption with the TJA1050 for clamp-30 applications with remote wake-up capability can be achieved by unpowering the transceiver and using a separate line for remote wake-up.

Pin compatibility between the TJA1050 and the PCA82C250 allows using the TJA1050 in already existing applications without changing the PCB. Thus, the customer can immediately benefit from the outstanding performance of the TJA1050.

2. GENERAL APPLICATION OF CAN HIGH-SPEED TRANSCEIVER

A general application of a CAN High-Speed Transceiver is shown in Figure 2.1. A protocol controller is connected to the transceiver via a serial data output line (TxD) and a serial data input line (RxD). The transceiver is attached to the bus lines via its two bus terminals CANH and CANL, which provide differential receive and transmit capability. The pin "S" (8) is used for mode control. The reference output voltage V_{ref} provides a nominal output voltage of $V_{CC}/2$ usable as a reference level for CAN-controllers with analog Rx inputs. It is not needed for the SJA1000, which features a digital input. The transceiver is powered with a nominal supply voltage of +5V.

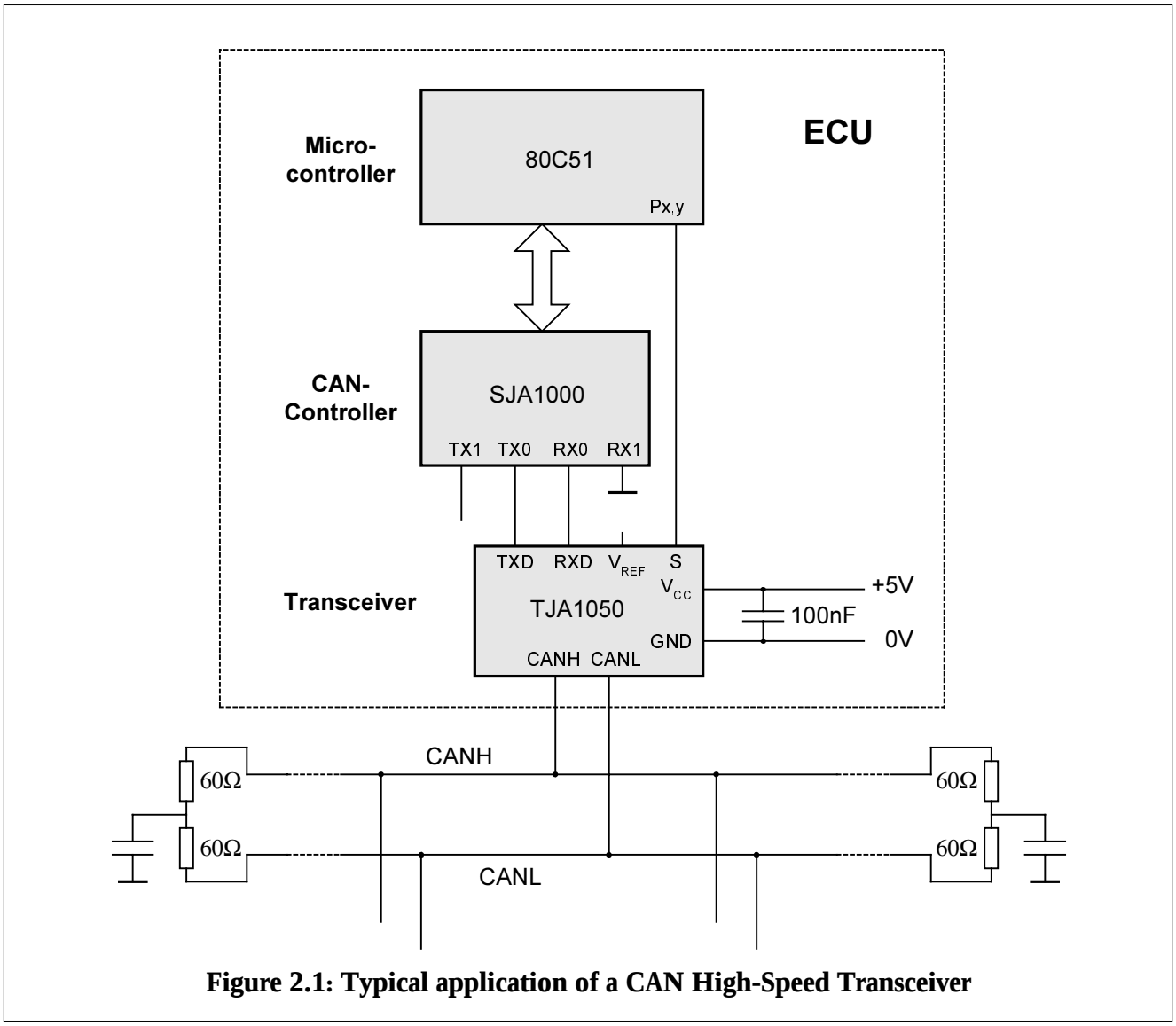

Figure 2.1: Typical application of a CAN High-Speed Transceiver

The protocol controller outputs a serial transmit data stream to the TxD input of the transceiver. An internal pull-up function sets the TxD input to logic HIGH i.e. the bus output driver is passive in open circuit condition. In the so-called recessive state (see Figure 2.3) the CANH and CANL inputs are biased to a voltage level of $V_{CC}/2$ via receiver input networks with a typical internal impedance of 25kΩ. Otherwise, if a logic LOW-level is applied to TxD, this activates the bus output stage, thus generating a

so-called dominant signal level on the bus lines (see Figure 2.3). The output driver CANH provides a source output from V_{CC} and the output driver CANL a sink output towards GND. As an example Figure 2.2 shows the block diagram of the TJA1050.

The bus is in recessive state if no bus node transmits a dominant bit. If one or multiple bus nodes transmit a dominant bit, the bus lines enter the dominant state thus overriding the recessive state (wired-AND characteristic).

The receiver comparator converts the differential bus signal to a logic level signal, which is output at RxD. The serial receive data stream is provided to the bus protocol controller for decoding. The receiver comparator is always active i.e. it monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit by bit arbitration scheme of CAN.

Typically the bus is set up with a pair of twisted wires. Considering a linear topology specified in ISO11898 the two bus ends are terminated with a resistor of nominal 120Ω. This results in the required bus load of nominal 60Ω. Close matching of the termination resistor with the cable impedance ensures that data signals will not be reflected at the bus ends.

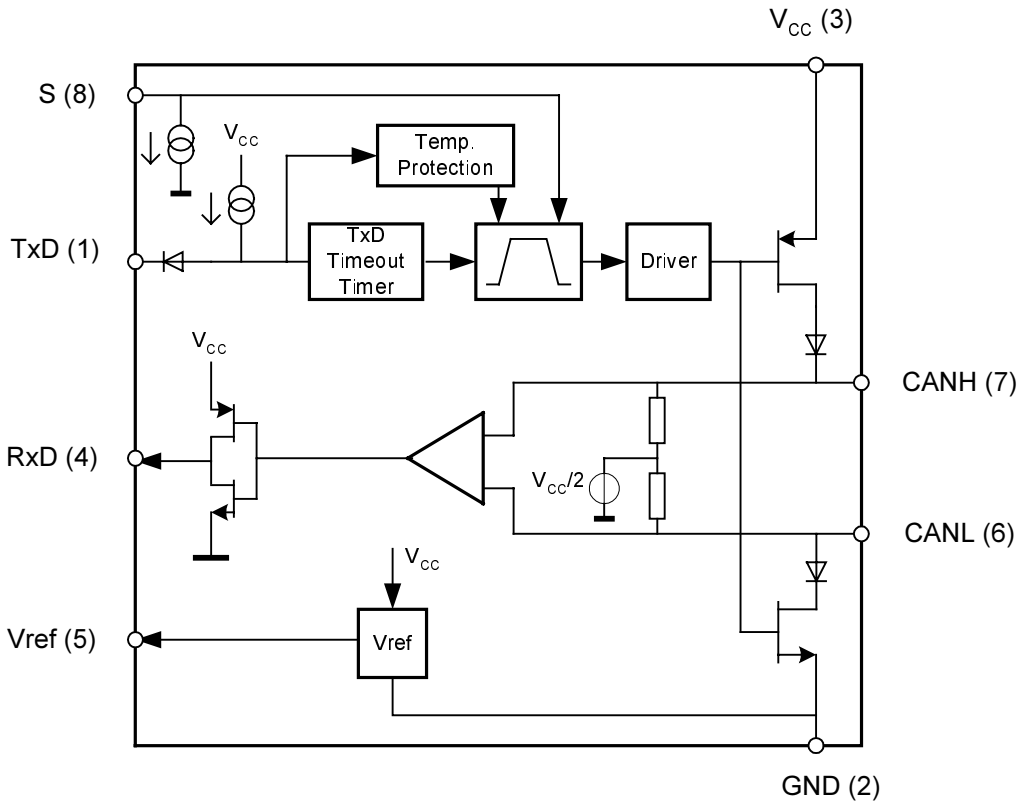

Figure 2.2: Block diagram of the TJA1050

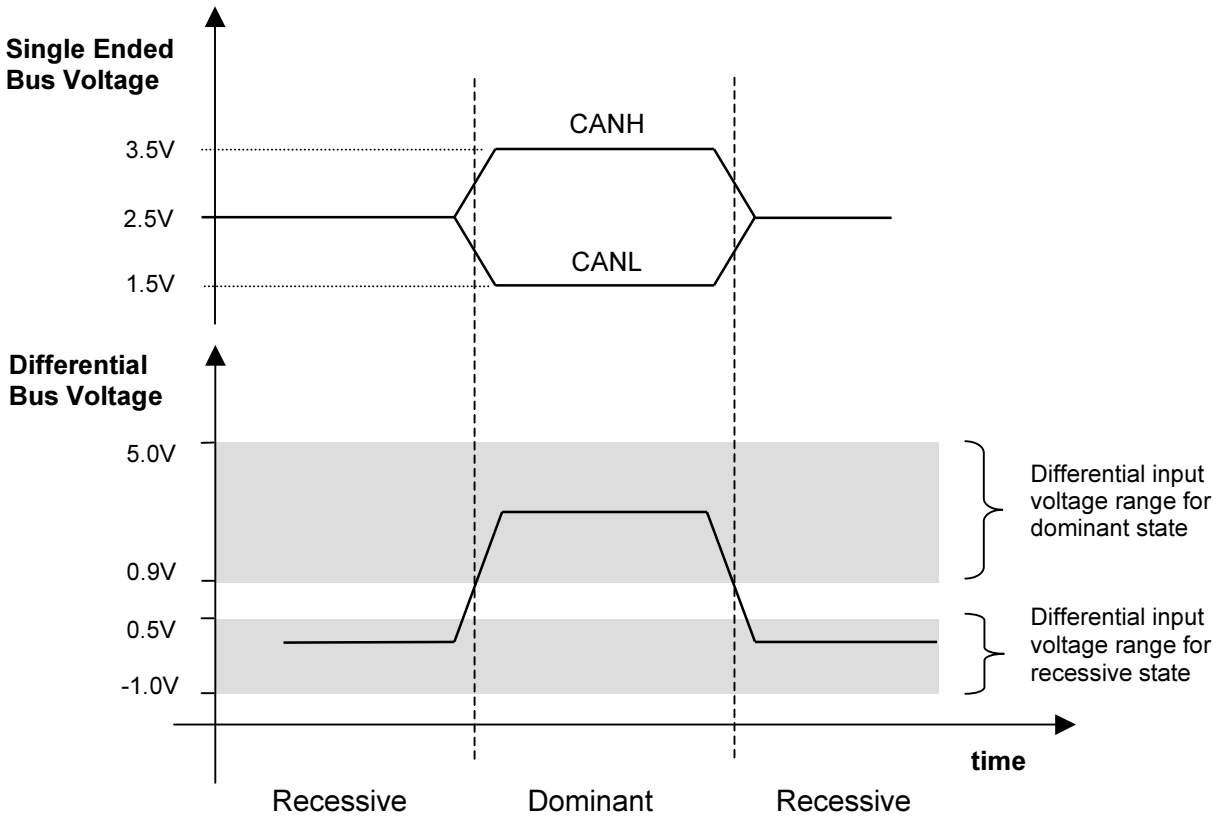

Figure 2.3: Nominal bus levels according to ISO 11898

3. THE TJA1050

3.1 Features

The main features of the TJA1050 are:

- Fully compatible with the ISO11898 standard
- High speed (up to 1Mbit/s)
- Very low Electromagnetic Emission
- Very high Electromagnetic Immunity
- An unpowered node does not disturb the bus lines
- Timeout protection at TxD against dominant bus clamping
- Silent mode providing Listen-Only mode and "Babbling Idiot" protection
- Bus pins protected against transients in an automotive environment
- Input levels compatible with 3.3V and 5V devices
- Thermally protected output drivers
- Short-circuit proof to battery and ground
- At least 110 nodes can be connected

3.2 Operation Modes

The TJA1050 provides two modes of operation, which are controlled by the pin "S".

- High-Speed Mode
- Silent Mode

A variable slope control known from the PCA82C250 is not supported. Rather the TJA1050 features a fixed slope. Even then the excellent output stage symmetry results in a much better EMC performance compared to previous products.

3.2.1 High-Speed Mode

The high-speed mode is the normal operating mode and is selected by connecting pin "S" to ground. Due to an internal pull-down function (see Figure 2.2) it is the default mode if pin "S" is unconnected.

In this mode the bus output signals are switched as fast as possible with a fixed slope. It is the appropriate mode for achieving a maximum bit rate and/or bus length and provides minimum transceiver loop delays.

3.2.2 Silent Mode

In silent mode the transmitter is disabled regardless of the TxD input signal. Thus the transceiver behaves as in non-transmitting state consuming the same supply current as in recessive state. The silent mode is selected with a HIGH signal at pin "S".

"Babbling Idiot" Protection

The silent mode allows setting a node in a state, where it is absolutely passive to the bus. It becomes necessary when a CAN-controller gets out of control and unintentionally sends messages ("babbling idiot"), which is claiming the bus. Activating the silent mode by the microcontroller allows releasing the bus even when there is no direct access from the microcontroller to the CAN-controller any more. Therefore, the silent mode is very useful in achieving high system reliability required by today´s electronic applications.

Listen-Only Mode

In silent mode RxD monitors the bus lines as usual. Thus, the silent mode provides a Listen-Only mode for diagnosis features. It ensures that a node does not influence the bus with dominant bits at all.

3.3 TxD Dominant Timeout

Besides the silent mode, the TJA1050 provides the TxD dominant timeout. This safety feature prevents an erroneous CAN-controller from clamping the bus to dominant level by a continuously dominant TxD signal.

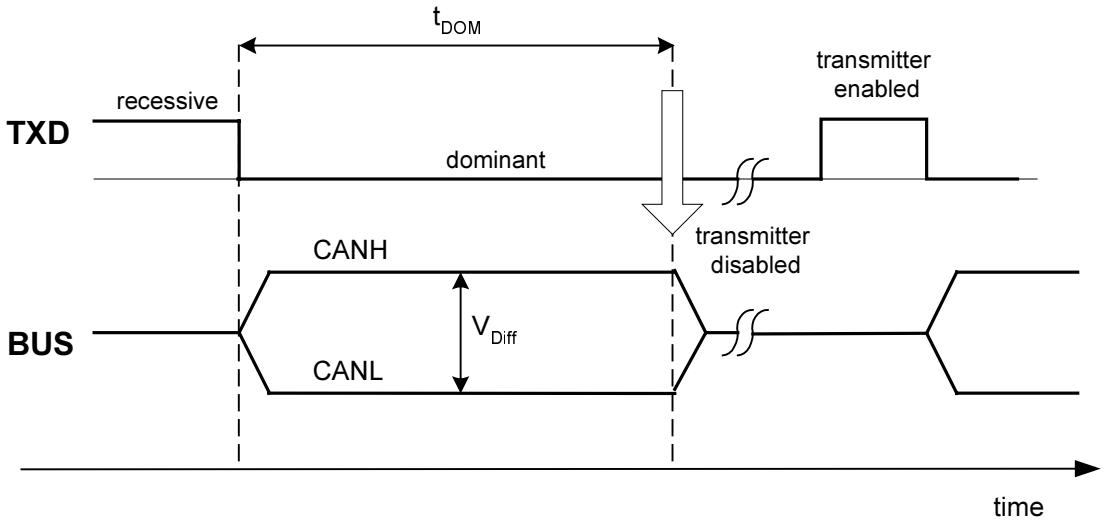

Figure 3.1: TxD dominant timeout feature

The function of the TxD dominant timeout is illustrated in Figure 3.1. After a maximum allowable TxD dominant time the transmitter will be disabled. The next dominant output drive is possible only after releasing TxD.

According to the CAN protocol [1], only a maximum of eleven successive dominant bits are allowed on TxD (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum allowable TxD dominant time, this will limit the minimum bit rate to 60kbit/s.

3.4 Compatibility with 3,3V Devices

Devices with supply voltages lower than 5V are increasingly migrating into automotive applications. The TJA1050 is able to communicate with 3,3V devices (like CAN-controller, µC) by providing reduced input thresholds to the TxD input and the input pin "S". It is suitable for 5V supplied µCs and CAN-controllers as well as for 3,3V supplied derivatives.

However, the 3,3V devices must be 5V tolerant with respect to RxD and TxD, because of a pull-up resistor to V_{cc} (5V) at TxD inside the transceiver and a V_{CC}-based push-pull stage for RxD.

4. EMC ASPECTS

Achieving a high EMC performance is not only a matter of the transceiver, a careful system implementation (termination, topology, external circuitry) is also very important. This chapter presents some application hints aiming to exploit the outstanding EMC performance of the TJA1050.

4.1 Split Termination Concept

Practice has shown that effective reduction of emission can be achieved by a modified bus termination concept called split termination. In addition this concept contributes to higher immunity of the bus system.

The split termination concept is illustrated in Figure 4.1. Basically each of the two termination resistors of the bus line end nodes is split into two resistors of equal value, i.e. two resistors of 60Ω instead of one resistor of 120Ω. As an option, stub nodes, which are connected to the bus via stubs, can be equipped with a similar split termination configuration. The resistor value for the stub nodes has to be chosen such that the bus load of all the termination resistors stays within the specified range from 50Ω to 65Ω[1]. Up to a number of 10 nodes (8 stub nodes and 2 bus end nodes) a typical resistor value is 1,3kΩ.

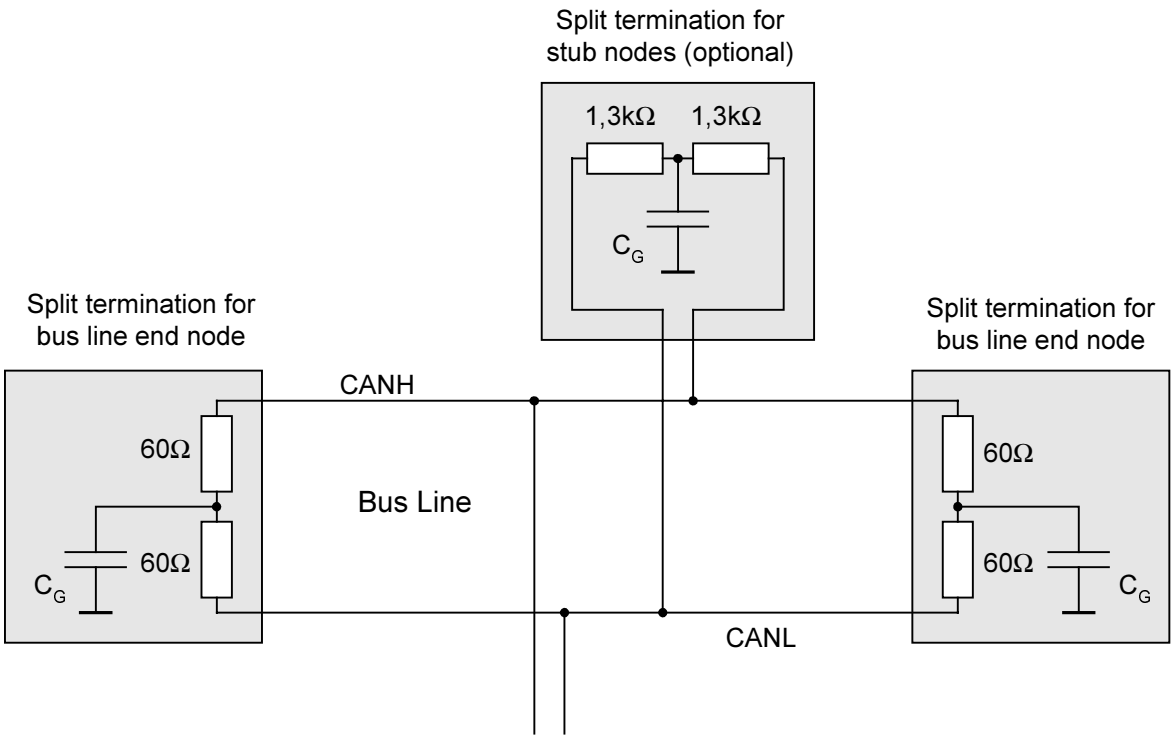

Figure 4.1: Typical split termination concept

The special characteristic of this approach is that the common mode signal is available at the centre tap of the termination. This common mode signal is terminated to ground via a capacitor C_G of e.g. 10nF to

[1] Review of ISO11898, planned to be published in 2000

100nF. However, it is obvious that the capacitor should be connected to a “quiet” ground level. For example a separate ground lead to the ground pin of the module connector with lowest inductance is recommended, if termination is placed inside of bus nodes.

The TJA1050 itself has reached such a high symmetry level that symmetry aspects of the two bus lines to reference ground become more and more important. Thus in order to exploit the excellent emission performance of the TJA1050, the matching tolerance between the split termination resistors at each ECU has to be considered.

It is worth to notice that the EMC performance of the TJA1050 has been optimized for use of the split termination without a choke. Hence, it is highly recommended to implement the split termination. The excellent output stage symmetry allows going without chokes as shown by different emission measurements. If, however, the EMC performance is still not sufficient, there will be the option to use additional measures like capacitors and common mode chokes.

4.2 Capacitors at CANH and CANL

Matching capacitors (in pairs) at the CANH and CANL output to GND (C_H and C_L) are frequently used to enhance immunity against electromagnetic interference. Along with the impedance of corresponding noise sources (RF), capacitors at CANH and CANL to GND are forming a RC low-pass filter. Regarding immunity the capacitor value should be as large as possible in order to achieve a low corner frequency. On the other hand, the overall capacitive load and the impedance of the output stage establish a RC low-pass filter for the data signals. Thus the associated corner frequency must be well above the data transmission frequency. This results in a limit for the capacitor value depending on the number of nodes and the data transmission frequency. Considering roughly 20Ω impedance for the output stage of the TJA1050 and a bus system of 10 nodes at 500kbit/s, the capacitor value should not exceed 470pF. Notice that capacitors are increasing the signal loop delay due to reducing rise and fall times.

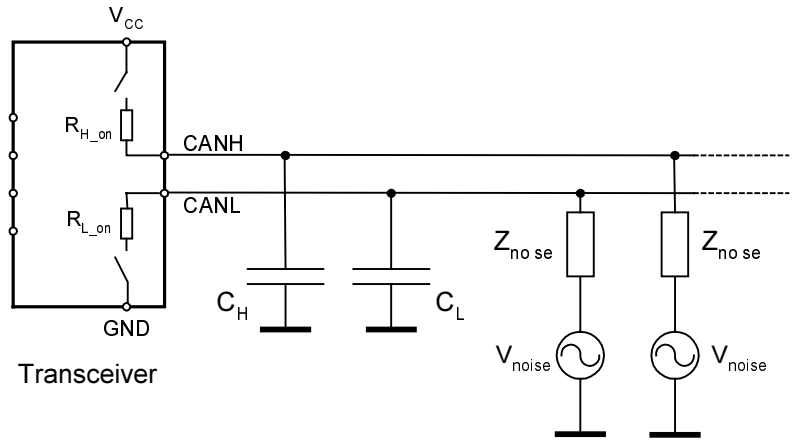

Figure 4.2: External capacitors forming RC low-pass filters

4.3 Common Mode Choke

A common mode choke provides high impedance for common mode signals and low impedance for differential signals. Due to this, common mode signals produced by RF noise and/or by non-perfect transceiver driver symmetry are damped significantly. Thus, common mode chokes help to reduce emission and to enhance immunity.

Figure 4.3 shows how to combine a common mode choke with the split termination and capacitors at CANH and CANL to GND. If priority is to enhance immunity, it is recommended to place the capacitors between the transceiver and the common mode choke. If, on the other hand, emission reduction is in focus, it is recommended to place the capacitors between the choke and the split termination (dashed line).

There is always a disadvantage facing with common mode chokes. The inductance of the choke may establish a resonant circuit together with pin capacitances. This can result in unwanted oscillations between the bus pins and the choke, both for differential and common mode signals. Oscillations of the differential signal can cause multiple switching of RxD.

Former transceiver products usually needed a common mode choke to fulfil the stringent emission and immunity requirements of the car manufacturers when using unshielded twisted-pair cable. The TJA1050 has the potential to build up in-vehicle bus systems without chokes. Whether chokes are needed finally depends on the specific system implementation like the wiring harness and the symmetry of the two bus lines (matching tolerances of resistors and capacitors).

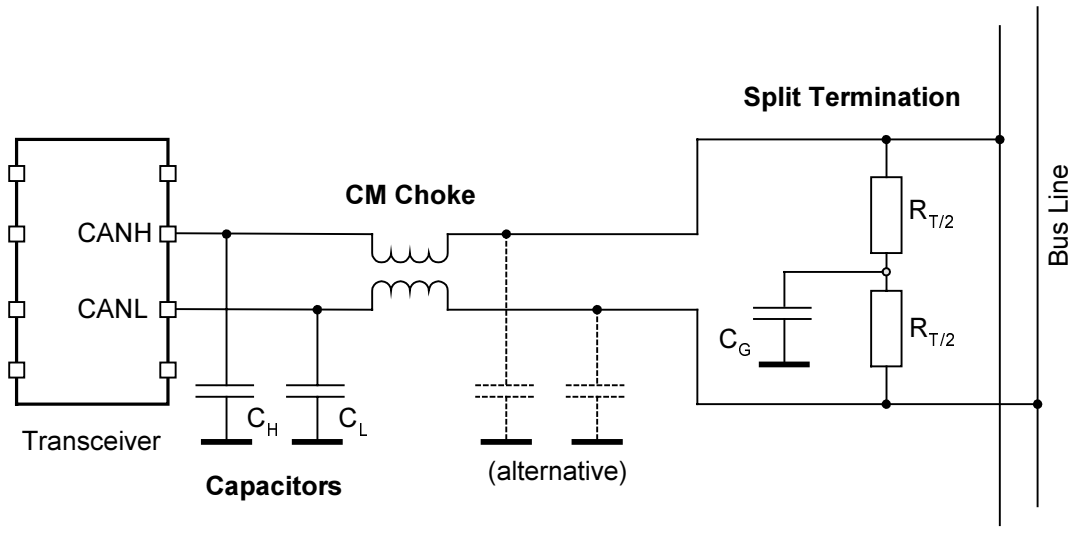

Figure 4.3: Bus node circuit combining split termination, choke and capacitors

5. POWER SUPPLY AND RECOMMENDED BYPASS CAPACITOR

Typically, a bypass capacitor is used for buffering the required supply voltage. A well-dimensioned bypass capacitor is also avoiding high current peaks flowing into the ground leads, thus establishing a “quiet” signal ground for the transceiver.

5.1 Average and Peak Supply Current

In order to properly dimension the V_{CC} supply of CAN High-Speed Transceiver two parameters have to be taken into account:

1. Average supply current
   The average supply current is needed to calculate the thermal load of the required V_{CC} voltage regulator. It is estimated with the assumption that a node is continuously sending messages with a duty cycle of 50%.
2. Peak supply current
   The peak supply current might flow in case of certain bus failure conditions for a certain time and thus has an impact on the power supply buffering.

The V_{CC} supply of the transceiver is recommended to support the characteristics shown in Table 5.1. These values have to be considered when calculating the thermal load of the required voltage regulator and the required bypass capacitor.

Condition	TJA1050		PCA82C250	
	Average I_{Vcc} (50% duty cycle)	Peak I_{Vcc} (Dominant, V_{TXD}=0V)	Average I_{Vcc} (50% duty cycle)	Peak I_{Vcc} (Dominant, V_{TXD}=0V)
Normal, 60Ω load	43mA	75mA	44mA	70mA
Worst case (CANH to GND short)	60mA	137mA	80mA	165mA

Table 5.1: Average and peak supply currents in normal and worst case

5.2 Bypass Capacitor

During the bit transition from recessive to dominant extra supply current is required to drive the bus. It can be calculated to

$$\Delta I_{CC} = I_{CC\_dom} - I_{CC\_rec},$$

where I_{CC_dom} denotes the supply current in dominant state and I_{CC_rec} the supply current in recessive state. Due to limited regulation speed of voltage regulators, a bypass capacitor is required to keep the supply voltage V_{CC} constant. Otherwise, V_{CC} might leave its specified voltage range (5V±5%) or at least show some oscillations due to the regulation behaviour of the voltage regulator. These oscillations are highly unwanted because these will increase electromagnetic emission. Considering normal operation, at least a capacitor value of 100nF is recommended for buffering. It is important to place the bypass capacitor close to the pin "V_{CC}" (3) and pin "GND" (2). Depending on the performance of the voltage regulator even higher capacitor values may be required.

6. GROUND-OFFSET ASPECTS

Bus systems in automotive have to deal with ground-offsets between the various nodes. This means that each node can "see" different single-ended bus voltages on the bus lines according to their own ground level, whereas the differential bus voltage remains unaffected.

According to the data sheet of the TJA1050 [3] the maximum allowable single-ended voltage of CANH is +12V, while the maximum allowable single-ended voltage of CANL is -12V. With single-ended bus voltages within this range, it is guaranteed that the differential receiver threshold voltage lies between 0.5 and 0.9V. The allowable single-ended voltage range is known as the common mode range of the differential receiver. ISO11898 calls for a common mode range from -2V to +7V. So, the TJA1050 provides an extended common mode range with respect to ISO11898.

Slightly exceeding the specified common mode range does not lead immediately to communication failures, but significant exceeding has to be avoided. Thus, there is a limitation for tolerable ground-offsets. The relation between the common mode range and the maximum allowable ground-offset is illustrated in Figure 6.1 and 6.2.

Figure 6.1 shows the case where the ground level of a transmitting node 2 lies above that of a receiving node 1. In this case the maximum allowable ground-offset corresponds to the maximum single-ended voltage of 12V for CANH with respect to the ground level of the receiving node. The maximum allowable ground-offset can be derived from Figure 6.1 to be 8V (GND_{Trans}-GND_{Rec}).

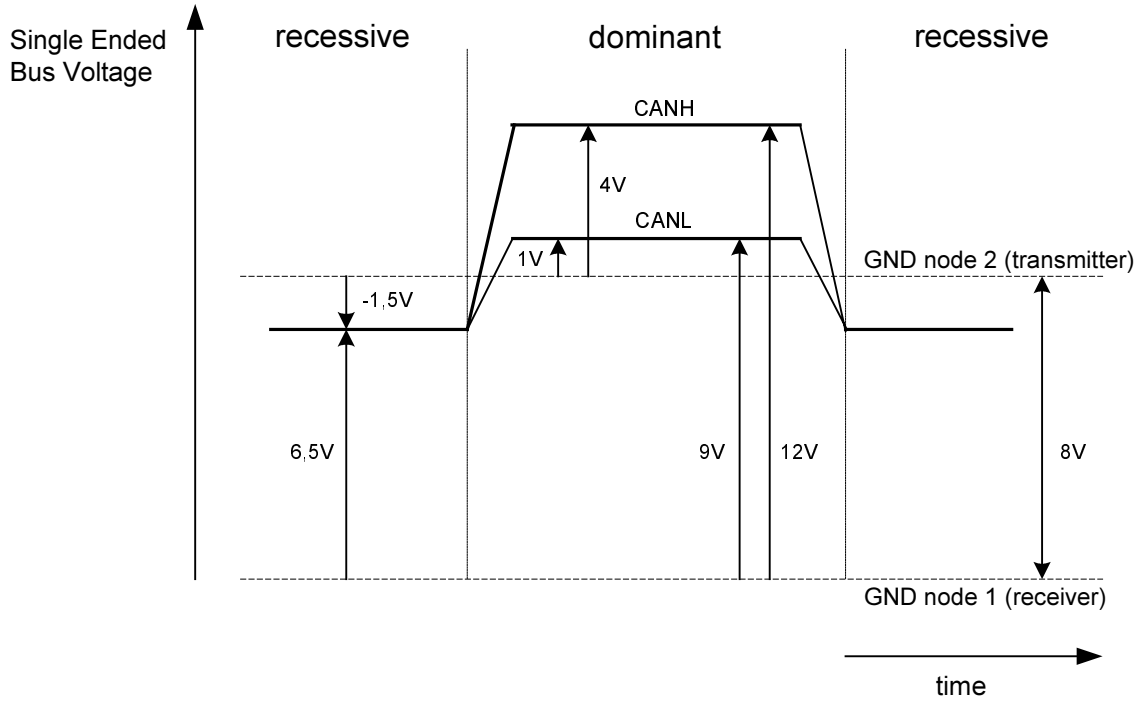

Figure 6.1: Ground level of the transmitting node 2 lies above that of the receiving node 1

Figure 6.2 shows the case where the ground level of the sending node 1 lies below that of the receiving node 2. In this case the maximum allowable ground-offset corresponds to the minimum single-ended voltage of -12V for CANL with respect to the ground level of the receiving node 2. The maximum

allowable ground-offset can be derived from Figure 6.2 to be -13V (GND_{Trans}-GND_{Rec}). As each node in a bus system acts temporary as transmitter, the maximum allowable ground-offset for the TJA1050 between any two nodes is limited to 8V.

In recessive bus state each node tries to pull the bus lines according to their biasing and ground level resulting in an average recessive bus voltage. In the example of Figure 6.1 the recessive bus voltage is found to be around 6,5V with respect to the ground level of the receiving node and -1,5V with respect to the ground level of the sending node.

The two examples in Figure 6.1 and Figure 6.2 indicate that ground-offsets in a bus system disturb significantly the symmetrical character of CANH and CANL with respect to the recessive voltage level. This implies the generation of unwanted common mode signals, which will increase electromagnetic emission. Since emission is very sensitive towards ground-offsets, appropriate system implementation has to be taken care of preventing ground-offset sources.

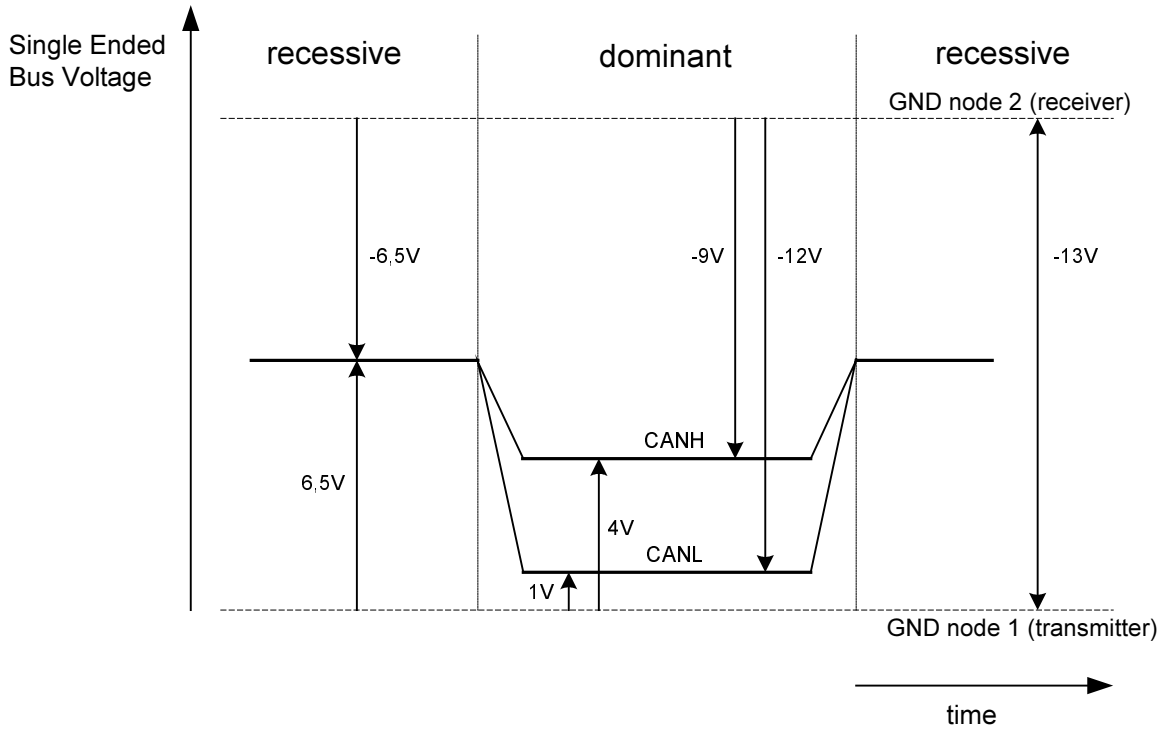

Figure 6.2: Ground level of the transmitting node 1 lies below that of the receiving node 2

7. UNPOWERED TRANSCEIVER

Today, automotive applications can be divided into systems, which are active only when ignition is on, and applications, which also have to work even when ignition is off, e.g. when the car is parked. This imposes a kind of partial networking realized by power supply either via clamp-15 (ignition) or clamp-30 (battery). Nodes at clamp-15 are unpowered when ignition is off, while nodes at clamp-30 are permanently supplied. A typical power supply configuration is shown in Figure 7.1.

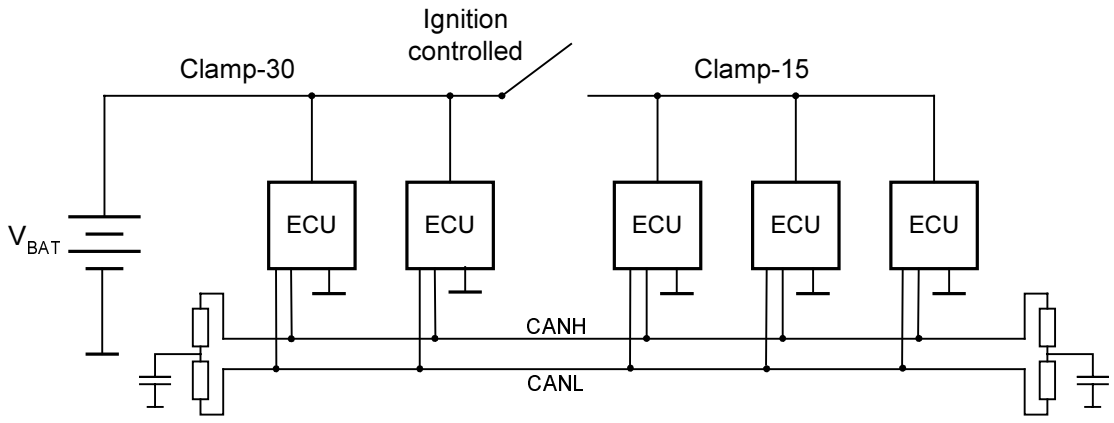

Figure 7.1: Typical power supply configuration

The above mentioned partial networking concept requires that unpowered clamp-15 transceivers must not degrade the system performance. Reverse currents flowing from the bus into unpowered transceivers have to be as low as possible. The TJA1050 is optimised with respect to low reverse currents and thus is predestined for clamp-15 nodes.

Transceivers have to deal with following issues when unpowered:

- Asymmetrical Biasing of the Common Mode Signal
- RXD Dominant Clamping
- Backward Supply towards V_{cc}

These issues will be discussed in the following chapters.

7.1 Asymmetrical Biasing of the Common Mode Voltage

In principle, a circuit like in Figure 7.2 provides symmetrical biasing of the common mode voltage with respect to the bus voltage levels in dominant state. Thus, in recessive state the bus voltages are biased to the symmetry voltage of $V_{CC}/2$.

In unpowered situation this internal biasing circuit is the reason for significant reverse currents flowing from each bus line into the transceiver. As a result the DC voltage level in recessive state and hence the common mode voltage falls below the symmetry voltage of $V_{CC}/2$. The TJA1050 has been designed to draw almost no current from the bus in unpowered case. Compared to the PCA82C250 reverse currents could be reduced by a factor of about 10.

The situation of earlier transceivers showing significant reverse currents is illustrated in Figure 7.3. It shows the single-ended bus voltages of CANH and CANL at the start of a message. The corresponding common mode voltage is also indicated.

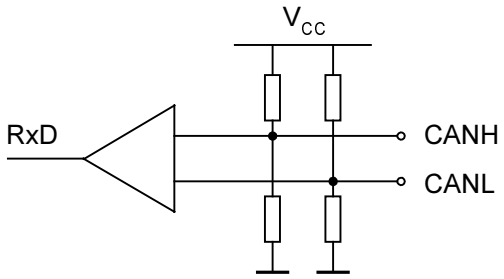

Figure 7.2: Simplified biasing circuit of a receiver input

After a long recessive bus state (bus idle) the common mode voltage is found significantly below the nominal value of $V_{CC}/2$. With the first dominant bit of a CAN message (Start of Frame bit) the common mode voltage recovers. Due to a relative large common mode resistance there is no significant common mode voltage drop for recessive bus states within a CAN-frame. That means that sharp common mode signals only appear at the start of CAN messages with the repetition frequency of CAN messages. These common mode signals will increase electromagnetic emission. The frequency of the dominant first harmonics is related to the repetition frequency of transmitted CAN messages. Due to very low reverse currents an unpowered TJA1050 transceiver will not degrade the emission performance.

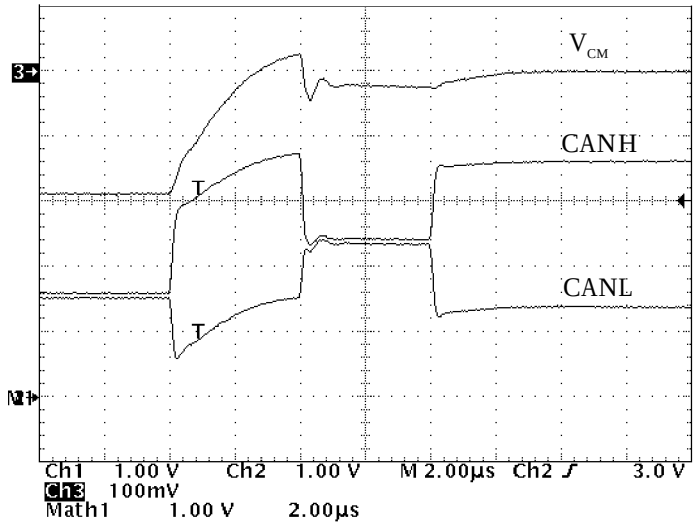

Figure 7.3: Bus voltages for earlier transceivers showing significant reverse currents

The effect of asymmetrical biasing of the common mode voltage becomes more visible, the more unpowered nodes are present within the system (larger total reverse currents). If there is a large number of unpowered nodes, it is recommended to additionally stabilize the nominal common mode voltage of $V_{CC}/2$

with an external biasing circuit in order to achieve an optimum EMC performance. Figure 7.4 illustrates the external biasing circuit, formed by the resistors R1 and R2, together with the split termination. The resistor values of R1 and R2 (respectively $R_{T/2}$) should match in pairs as close as possible. A reasonable value range for R1 and R2 is from 1kΩ to 2kΩ. The presented external biasing concept is only applicable to clamp-30 nodes because they are always powered.

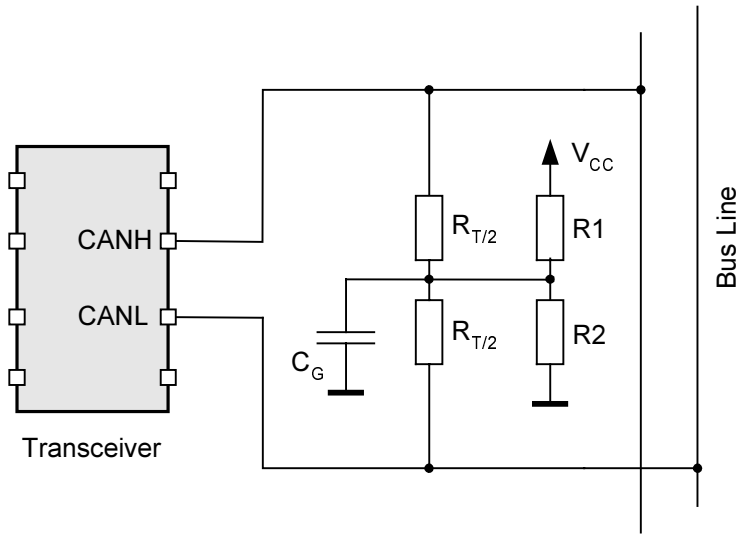

Figure 7.4: External biasing circuit

7.2 RxD Dominant Clamping

Another important issue with respect to an unpowered transceiver is illustrated in Figure 7.5. There are applications known where the transceiver is unpowered in order to achieve low power consumption, while the microcontroller/CAN-controller remains powered and is put into its standby mode.

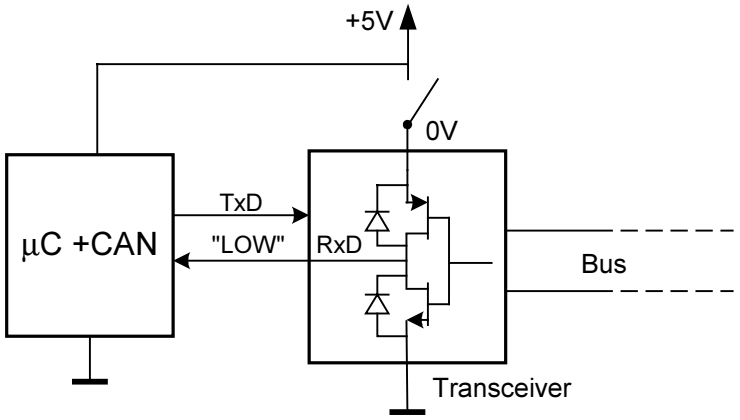

Figure 7.5: RxD Dominant clamping of unpowered transceiver

Normally, transceivers are pulling RxD to GND if unpowered, thus clamping RxD to dominant level. This will be recognised by the CAN-controller as a continuous wake-up signal. So it is not possible to put the CAN-controller into its standby mode when the transceiver is unpowered.

The TJA1050 overcomes this RxD dominant clamping by making the RxD-pin floating in unpowered case. Now an integrated RxD pull-up resistor in the CAN-controller is sufficient to pull RxD recessive. It is also possible to add an external pull-up resistor if desired.

7.3 Backward Supply towards V_{CC}

Reverse currents flowing into unpowered transceivers generally provide an unwanted backward supply towards V_{CC}. This might cause some unwanted behaviour. Considering a situation where the transceiver is unpowered while the microcontroller/CAN-controller remains powered, there are mainly four reverse current paths possible.

- Reverse currents from a High level at RxD to V_{cc}
- Reverse currents from a High level at TxD to V_{cc}
- Reverse currents from a High level at pin "S" to V_{CC}
- Reverse currents from the bus lines to V_{CC} and GND

The first three paths have been eliminated completely with the TJA1050. Reverse currents from the bus lines have been reduced significantly. As a result the possible backward supply voltage at V_{CC} lies significantly below that of the PCA82C250. It is expected that the remaining backward supply voltage is not capable of initiating some undefined behaviour of devices supplied by the same V_{CC}.

8. REPLACING THE PCA82C250 BY THE TJA1050

Because of a general pin and functional compatibility an easy migration of existing PCA82C250 applications towards the TJA1050 is possible. Using the TJA1050 instead of the PCA82C250 in existing bus systems needs consideration of two different aspects: Interoperability and compatibility. Interoperability means the ability of the PCA82C250 and the TJA1050 to work together in the same bus network, while the term compatibility includes issues like pinning, operation modes, supply voltage range, interfacing to the bus and to the CAN-controller, external circuits etc.

Since both, the PCA82C250 and TJA1050, are compatible with the ISO11898 standard, it is guaranteed that both transceivers are interoperable and thus are able to work together in the same bus network. Compatibility issues are discussed in the following subchapters.

8.1 Pinning

The PCA82C250 and TJA1050 have the same pinning. Thus PCBs which had been initially developed for the PCA82C250 can be used in most cases for the TJA1050 as well.

8.2 Operation Modes

Both transceivers use pin 8 for mode selection. The slope control mode of the PCA82C250 is not supported by the TJA1050. A resistor at pin 8 formerly used in PCA82C250 applications to adjust the slope is not needed any more. A HIGH signal at pin 8 activates the standby mode in case of the PCA82C250 with reduced current consumption [4]. Similar to this standby mode, now the silent mode of the TJA1050 offers the possibility to disable the transmitter but without reducing the current consumption. It will be selected in the same way with a HIGH at pin 8. Both transceivers are set into high-speed mode with a LOW at pin 8.

8.3 Slope Control Resistor

Whether the slope control resistor has to be removed depends on the application. There are two different cases:

1. If the slope resistor is directly connected to GND, this resistor does not need to be removed.
2. If the slope resistor is connected to an output port of the microcontroller allowing the previous application to switch between slope control and standby mode (with the PCA82C250), this resistor has to be removed in order to allow switching between high-speed and silent mode (with the TJA1050).

8.4 Interfacing

The interfacing to the controller is performed as usual via the serial digital input TxD and the output RxD. Notice that the TxD and pin "S" input thresholds have been decreased in order to guarantee that 3,3V supplied controllers are able to drive the inputs of the TJA1050. Conventional 5V supplied controllers are supported as usual.

The following Table 8.1 summarizes the compatibility issues, which have to be taken into account when replacing the PCA82C250 by the TJA1050.

Features	TJA1050	PCA82C250
Interoperability/ISO11898	√	√
Pin Compatibility	√	√
Operation Modes: - HIGH at pin 8 - LOW at pin 8 - Resistor at pin 8 to GND - Floating pin 8	 Silent Mode High speed High speed High speed	 Standby Mode High speed Slope Control High speed
Supply Voltage Tolerance	±5%	±10%
Passive if unpowered	Yes	No
TxD Dominant Protection	Yes	No
Minimum Bit Rate	60kbit/s	0kbit/s
3,3V I/O Compatibility	Yes	No

Table 8.1: Comparison between the TJA1050 and the PCA82C250

9. BUS NETWORK ASPECTS

This chapter deals with items like the maximum number of nodes, the maximum bus line length and topology aspects. Especially the topology appears to have a significant influence on the system performance.

9.1 Maximum Number of Nodes

The number of nodes, which can be connected to a bus, depends on the minimum load resistance a transceiver is able to drive. The TJA1050 transceiver provides an output drive capability down to a minimum load of $R_{L.min}$ = 45Ω for V_{CC} > 4.75V. The overall bus load is defined by the termination resistance R_T, the bus line resistance R_W and the transceiver´s differential input resistance R_{diff}. The DC circuit model of a bus system is shown in Figure 9.1. For worst case consideration the bus line resistance R_W is considered to be zero. This leads to the following relations for calculating the maximum number of nodes.:

$$\frac{R_{T.\min} \times R_{diff.\min}}{n_{\max} \times R_{T.\min} + 2R_{diff.\min}} > R_{L.\min} \Rightarrow n_{\max} < R_{diff.\min} \times \left(\frac{1}{R_{L.\min}} - \frac{2}{R_{T.\min}} \right)$$

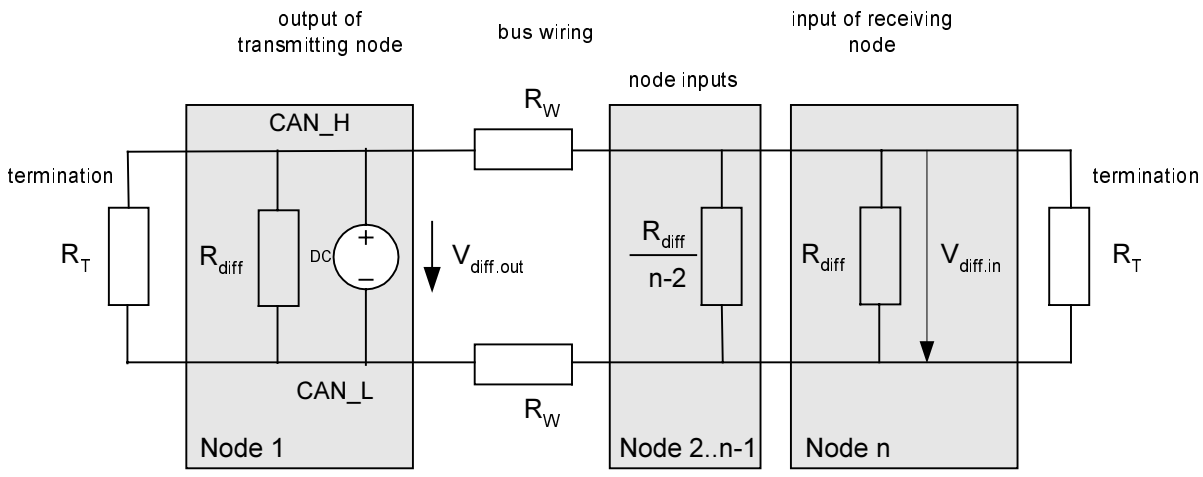

Figure 9.1: DC circuit model for a bus system according to ISO11898

Table 9.1 gives the maximum number of nodes for two different termination resistances. Notice that connecting a large number of nodes requires relatively large termination resistances.

Transceiver	$R_{Diff.min}$ (kΩ)	$V_{CC.min}$ (V)	$R_{L.min}$ (Ω)	Number of Nodes ($R_{T.min}$=118Ω)	Number of Nodes ($R_{T.min}$=130Ω)
TJA1050	25	4.75	45	131	170
		4.9	39	217	256
PCA82C250	20	4.9	45	105	136

Table 9.1: Maximum number of nodes

9.2 Maximum Bus Line Length

The maximum achievable bus line length in a CAN network is determined essentially by the following physical effects:

1. The loop delays of the connected bus nodes (CAN controller, transceiver etc.) and the delay of the bus line
2. The relative oscillator tolerance between nodes
3. The signal amplitude drop due to the series resistance of the bus cable and the input resistance of bus nodes (for a detailed description refer to [6])

Effects 1 and 2 determine a value for the maximum bus line length with respect to the CAN bit timing [5]. Effect 3, on the other side, determines a value with respect to the output signal drop along the bus line. The minimum of the two values has to be taken as the actual maximum allowable bus line length. As the signal drop is only significant for very long lengths, effect 3 can often be neglected for high data rates.

Specification	Data Rate	
	500kbit/s	250kbit/s
SAE J2284	30m	-
DeviceNet	100m	250m
TJA1050	**107m**	**270m**

Table 9.2: Maximum bus line length for some standards and the TJA1050

Table 9.2 gives the maximum bus line length for the bit rates 500kbit/s and 250kbit/s, along with values specified in some standards associated to CAN. The calculation is based on effects 1 and 2 assuming an oscillator tolerance of better than 0.15%. Notice that the stated values apply only for a well terminated linear topology. Bad signal quality because of improper termination can lower the maximum allowable bus length.

9.3 Topology Aspects

The topology describes the wiring harness structure. Typical structures are linear, star- or multistar-like. In automotive, shielded or unshielded twisted pair cable usually functions as a transmission line. Transmission lines are generally characterized by the length-related resistance R_{Length}, the specific line delay t_{delay} and the characteristic line impedance Z. Table 9.3 shows the physical media parameters specified in the ISO11898 and SAE J2284 standard [7]. Notice that SAE J2284 specifies the twist rate in addition.

Parameter	Notation	Unit	ISO 11898			SAE J2284		
			Min.	Nom.	Max.	Min.	Nom.	Max.
Impedance	Z	Ω	108	120	132	108	120	132
Length-related resistance	R	mΩ/m	-	70	-	-	70	-
Specific line delay	t_{delay}	ns/m	-	5	-	-	5.5	-
Twist rate	r_{twist}	twist/m	-	-	-	33	-	50

Table 9.3: Physical media parameters of a pair of wires (shielded or unshielded)

9.3.1 Ringing due to Signal Reflections

Transmission lines must be terminated with the characteristic line impedance, otherwise signal reflections will occur on the bus causing significant ringing. The topology has to be chosen such that reflections will be minimized. Often the topology is a trade-off between reflections and wiring constraints.

CAN is well prepared to deal with reflection ringing due to some useful protocol implementations:

1. Only recessive to dominant transitions are used for resynchronization.
2. Resynchronization is allowed only once between two sample points, and only if a recessive bit was sampled.
3. The sample point is programmable to be close to the end of the bit time.

9.3.2 Linear Topology

Generally the CAN high-speed standard ISO11898 defines a single line structure as network topology. The bus line is terminated at both ends with a single termination resistor. The nodes are connected via unterminated drop cables or stubs to the bus. In order to keep the ringing duration short compared to the bit time, the stub length should be as short as possible. For example the ISO11898 standard limits the stub length to 0,3m. The corresponding SAE standard, J2284, recommends keeping the stub length below 1m. To minimize standing waves, ECUs should not be placed equally spaced on the network and cable tail lengths should not all be the same length [7]. Table 9.4 along with Figure 9.2 illustrates the topology requirements of the SAE J2284 standard.

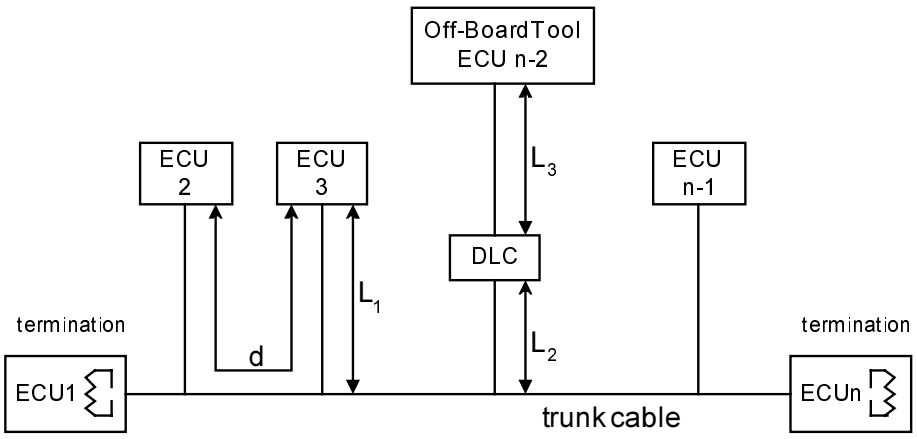

Figure 9.2: Topology requirements of SAE J2284

In practice some deviation from that stringent topology proposals might be necessary, because longer stub lengths are needed. Essentially the maximum allowable stub length depends on the bit timing parameters, the trunk cable length and the accumulated drop cable length. For a rule of thumb calculation of the maximum allowable stub length refer to [6].

The star topology is neither covered by ISO11898 nor by SAE J2284. However, it is sometimes used in automotive applications to overcome wiring constraints within the car. Generally, the signal integrity suffers from a star topology compared to a linear topology. It is recommended to prove the feasibility of a specific topology in each case by simulations or measurements on a system set-up.

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
ECU Cable Stub length	L1	m	0	-	1
In-Vehicle DLC Cable Stub Length	L2	m	0	-	1
Off-Board DLC Cable Stub Length	L3	m	0	-	5
Distance between any two ECUs	d	m	0.1	-	30

Table 9.4: ECU topology requirements of SAE J2284

10. REFERENCES

[1] Road Vehicles . Interchange of Digital Information - Controller Area Network (CAN) for high-speed communication, ISO11898, International Standardization Organization, 1993 (Review planned to be published in 2000)

[2] Data Sheet SJA1000, Stand-alone CAN Controller, Philips Semiconductors, January 2000

[3] Data Sheet TJA1050, High Speed CAN transceiver, Philips Semiconductors, May 2000

[4] Data Sheet PCA82C250, CAN Controller Interface, Philips Semiconductors, January 2000

[5] Application Note AN97046, Determination of Bit Timing Parameters for the CAN Controller SJA1000, Philips Semiconductors, 1997

[6] Application Note AN96116, PCA82C250/251 CAN Transceiver, Philips Semiconductors, 1996

[7] High Speed CAN (HSC) for Vehicle Applications at 500kbps, SAE J2284, 1999