



AFE1115

# HDSL/MDSL ANALOG FRONT END WITH VCXO

## FEATURES

- COMPLETE HDSL ANALOG INTERFACE
- E1, T1 AND MDSL OPERATION
- VCXO AND VCXO CONTROL CIRCUITRY

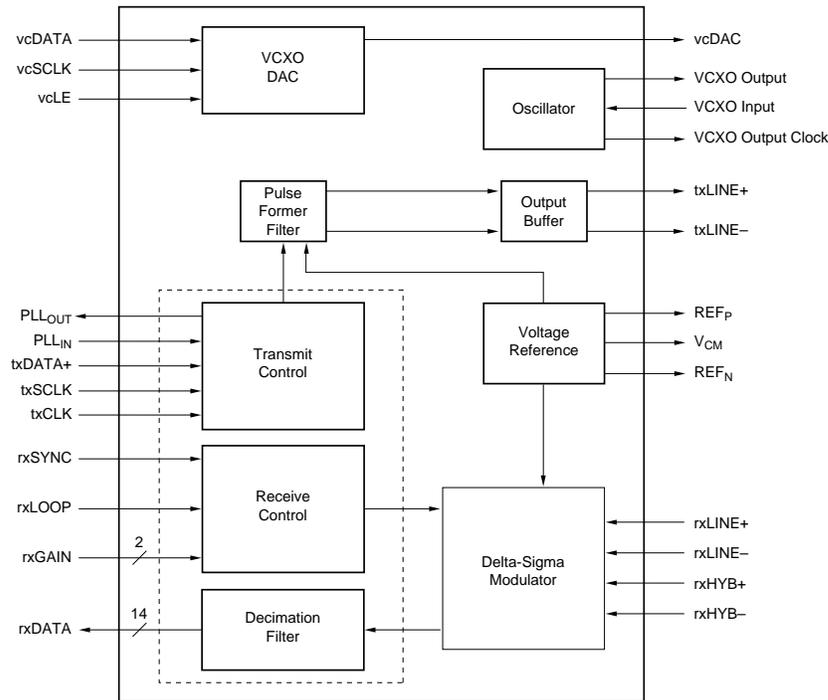
- +5V ONLY (5V or 3.3V Digital)
- SCALEABLE DATA RATE
- 300mW POWER DISSIPATION
- 56-PIN SSOP

## DESCRIPTION

Burr-Brown's Analog Front End greatly reduces the size and cost of an HDSL (High bit rate Digital Subscriber Line) system by providing all of the active analog circuitry needed to connect an HDSL digital signal processor to an external compromise hybrid and a HDSL line transformer. The transmit and receive filter responses automatically change with clock frequency—allowing the AFE1115 to operate over a range of data rates from 196kbps to 1.168Mbps.

Functionally, this unit consists of a transmit and a receive section with a VCXO (Voltage Controlled

Crystal Oscillator) control DAC and VCXO circuitry. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line. Data to the VCXO and symbol data are sent to the AFE1115 via two serial interfaces; the receive data is available as a 14-bit parallel word. This IC operates on a single 5V supply. The digital circuitry in the unit can be connected to a supply from 3.3V to 5V. It is housed in a small 56-pin SSOP package.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111  
 Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

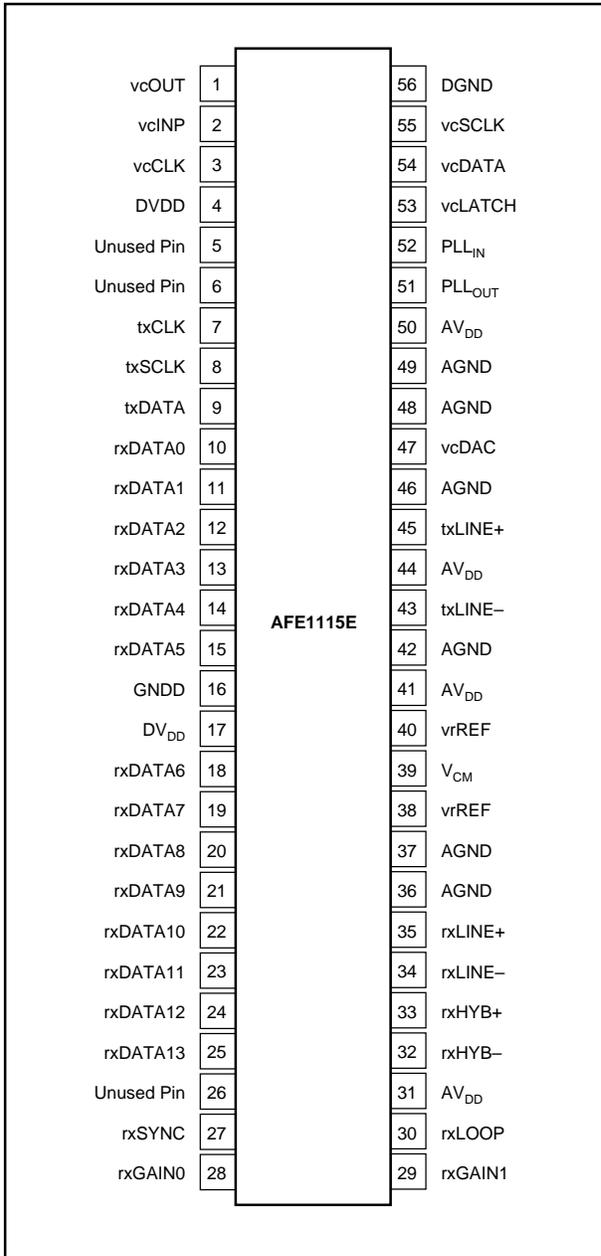
# SPECIFICATIONS

Typical at 25°C, AV<sub>DD</sub> = +5V, DV<sub>DD</sub> = +3.3V, f<sub>ix</sub> = 584kHz (E1 rate), unless otherwise specified.

PARAMETER	COMMENTS	AFE1115E			UNITS
		MIN	TYP	MAX	
<b>RECEIVE CHANNEL</b> Number of Inputs Input Voltage Range Common-Mode Voltage Input Impedance All Inputs Input Capacitance Input Gain Matching Resolution Programmable Gain Settling Time for Gain Change Gain + Offset Error Output Data Coding Output Data Rate, rxSYNC <sup>(3)</sup>	Differential Balanced Differential <sup>(1)</sup>  Line Input vs Hybrid Input  Three Gains: -3dB, 3dB, and 9dB  Tested at Each Gain Range Two's Complement	2     14 -3   98	  ±3.0 +2.5  See Typical Performance Curves 10 ±2  6 5	       +9   584	V V  pF % Bits dB Symbol Periods %FSR <sup>(2)</sup> kHz
<b>TRANSMIT CHANNEL</b> Transmit Clock Rate, f <sub>ix</sub> T1 Transmit -3dB Point T1 Rate Power <sup>(4, 5)</sup> E1 Transmit -3dB Point E1 Transmit Power <sup>(4, 5)</sup> Pulse Output Common-Mode Voltage, V <sub>CM</sub> Output Resistance <sup>(6)</sup>	Symbol Rate Bellcore TA-NWT-3017 Compliant See Test Method Section ETSI RTR/TM-03036 Compliant See Test Method Section  DC to 1MHz	98  13  13    98	  196  292  See Typical Performance Curves AV <sub>DD</sub> /2 1	584  14  14    1	kHz kHz dBm kHz dBm V Ω
<b>TRANSCEIVER PERFORMANCE</b> Uncancelled Echo <sup>(7)</sup>	rxGAIN = -3dB, Loopback Enabled rxGAIN = -3dB, Loopback Disabled rxGAIN = 3dB, Loopback Disabled rxGAIN = 9dB, Loopback Disabled			-67 -67 -71 -73	dB dB dB dB
<b>VCXO PERFORMANCE</b> VCXO Control DAC Resolution VCXO Control DAC Output VCXO Control DAC Output VCXO Performance	Positive Full Scale Output Negative Full Scale Output See VCXO Circuit and Layout Section	8	4.5 0.5		Bits V V
<b>DIGITAL INTERFACE<sup>(6)</sup></b> Logic Levels V <sub>IH</sub> V <sub>IL</sub> V <sub>OH</sub> V <sub>OL</sub>	I <sub>IH</sub>   < 10μA  I <sub>IL</sub>   < 10μA I <sub>OH</sub> = -20μA I <sub>OL</sub> = 20μA	DV <sub>DD</sub> -1 -0.3 DV <sub>DD</sub> -0.5		DV <sub>DD</sub> +0.3 +0.8  +0.4	V V V V
<b>POWER</b> Analog Power Supply Voltage Analog Power Supply Voltage Digital Power Supply Voltage Digital Power Supply Voltage Power Dissipation <sup>(4, 5, 8)</sup> Power Dissipation <sup>(4, 5, 8)</sup> PSRR	Specification Operating Range Specification Operating Range AV <sub>DD</sub> = 5V, DV <sub>DD</sub> = 3.3V, AV <sub>DD</sub> = DV <sub>DD</sub> = 5V	4.75  3.15	5  3.3  300 350 60	5.25  5.25	V V V V mW mW dB
<b>TEMPERATURE RANGE</b> Operating <sup>(6)</sup>		-40		+85	°C

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common-mode voltage on each pin is ±1.5V to achieve a total input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (16.5dBm output from txLINEP and txLINEN). (5) See the Test Method section of this data sheet for more information. (6) Guaranteed by design and characterization. (7) Uncancelled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications sections of this data sheet for more information. (8) Power dissipation includes only the power dissipated within the component and does not include power dissipated in the external loads. See the Discussion of Specifications section for more information.

## PIN CONFIGURATION



## PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	TEMPERATURE RANGE
AFE1115E	56-Pin Plastic SSOP	346	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN DESCRIPTIONS

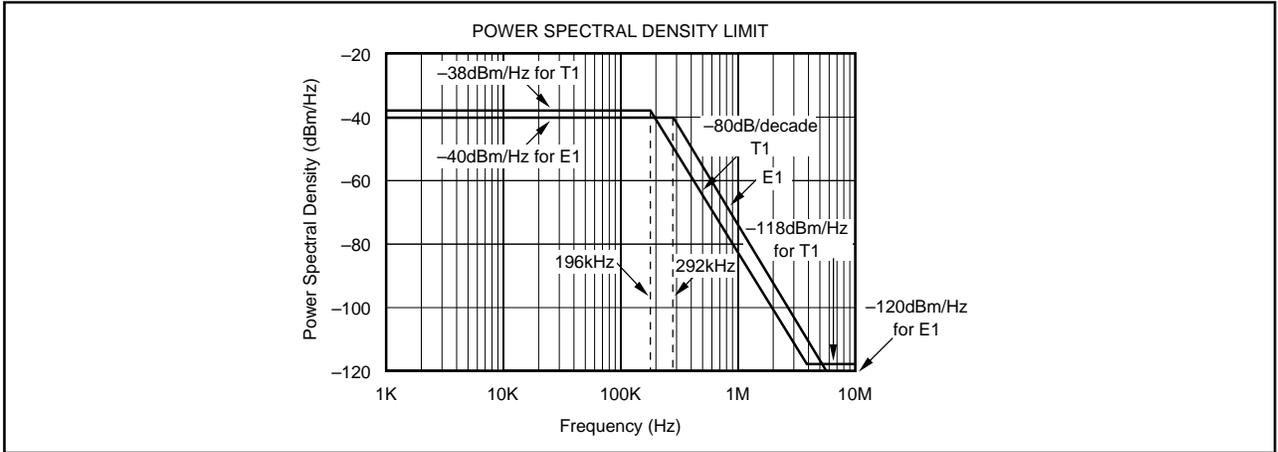
PIN #	TYPE	NAME	DESCRIPTION
1	Output	vcOUT	VCXO Output
2	Input	vcINP	VCXO Input
3	Output	vcCLK	VCXO Output Clock
4	Power	DVDD	Digital Supply (+3.3 to +5V)
5	NC	Unused Pin	
6	NC	Unused Pin	
7	Input	txCLK	Transmit Baud Clock (XMTLE signal) (1168kHz for E1)
8	Input	txSCLK	Transmit Serial Clock
9	Input	txDATA	Transmit Data Input
10	Output	rxDATA0	ADC Output Bit-0
11	Output	rxDATA1	ADC Output Bit-1
12	Output	rxDATA2	ADC Output Bit-2
13	Output	rxDATA3	ADC Output Bit-3
14	Output	rxDATA4	ADC Output Bit-4
15	Output	rxDATA5	ADC Output Bit-5
16	Ground	GNDD	Digital Ground
17	Power	DV <sub>DD</sub>	Digital Supply (+3.3 to +5V)
18	Output	rxDATA6	ADC Output Bit-6
19	Output	rxDATA7	ADC Output Bit-7
20	Output	rxDATA8	ADC Output Bit-8
21	Output	rxDATA9	ADC Output Bit-9
22	Output	rxDATA10	ADC Output Bit-10
23	Output	rxDATA11	ADC Output Bit-11
24	Output	rxDATA12	ADC Output Bit-12
25	Output	rxDATA13	ADC Output Bit-13
26	NC	Unused Pin	(DV <sub>DD</sub> may be connected for pinout compatibility with AFE1105)
27	Input	rxSYNC	ADC Sync Signal (392kHz for T1, 584kHz for E1)
28	Input	rxGAIN0	Receive Gain Control Bit-0
29	Input	rxGAIN1	Receive Gain Control Bit-1
30	Input	rxLOOP	Loopback Control Signal (loopback is enabled by positive signal)
31	Power	AV <sub>DD</sub>	Analog Supply (+5V)
32	Input	rxHYB-	Negative Input from Hybrid Network
33	Input	rxHYB+	Positive Input from Hybrid Network
34	Input	rxLINE-	Negative Line Input
35	Input	rxLINE+	Positive Line Input
36	Ground	AGND	Analog Ground
37	Ground	AGND	Analog Ground
38	Output	vrREFP	Positive Reference Output
39	Output	V <sub>CM</sub>	Common-mode Voltage (buffered)
40	Output	vrREFN	Negative Reference Output
41	Power	AV <sub>DD</sub>	Analog Supply (+5V)
42	Ground	AGND	Analog Ground
43	Output	txLINE-	Negative Line Output
44	Power	AV <sub>DD</sub>	Analog Supply (+5V)
45	Output	txLINE+	Positive Line Output
46	Ground	AGND	Analog Ground
47	Output	vcDAC	VCXO Control
48	Ground	AGND	Analog Ground
49	Ground	AGND	PLL Ground
50	Power	AV <sub>DD</sub>	PLL Supply
51	Output	PLL <sub>OUT</sub>	PLL Filter Output
52	Input	PLL <sub>IN</sub>	PLL Filter Input
53	Input	vcLATCH	VCXO Control Latch Enable
54	Input	vcDATA	VCXO Control Data
55	Input	vcSCLK	VCXO Control Serial Clock
56	Ground	DGND	Digital Ground

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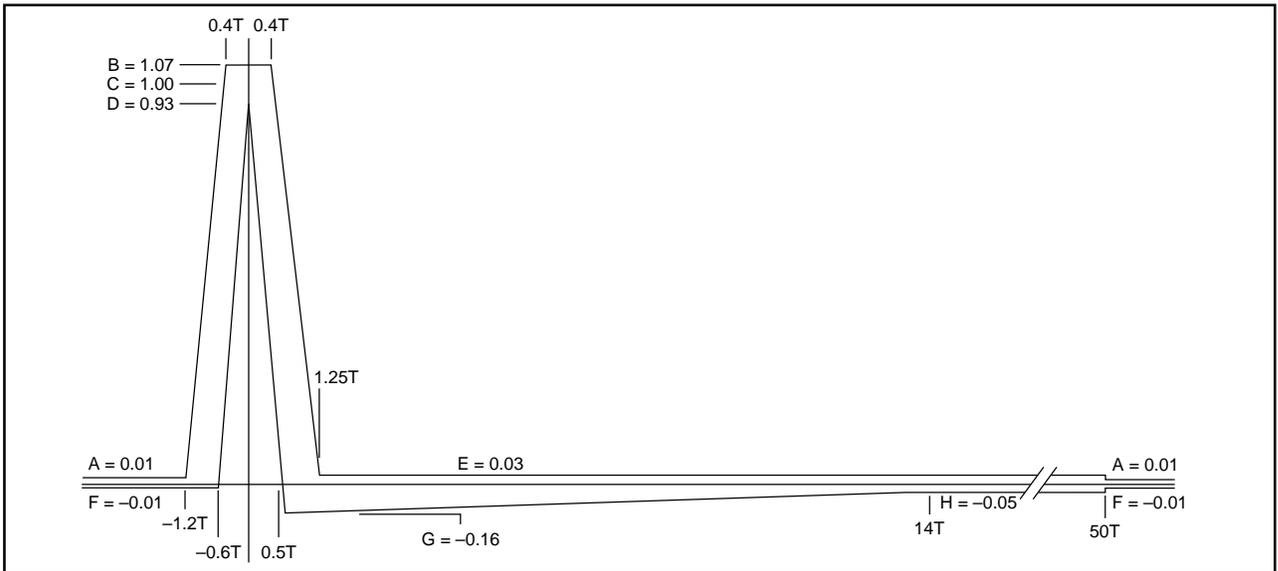
# TYPICAL PERFORMANCE CURVES

## At Output of Pulse Transformer

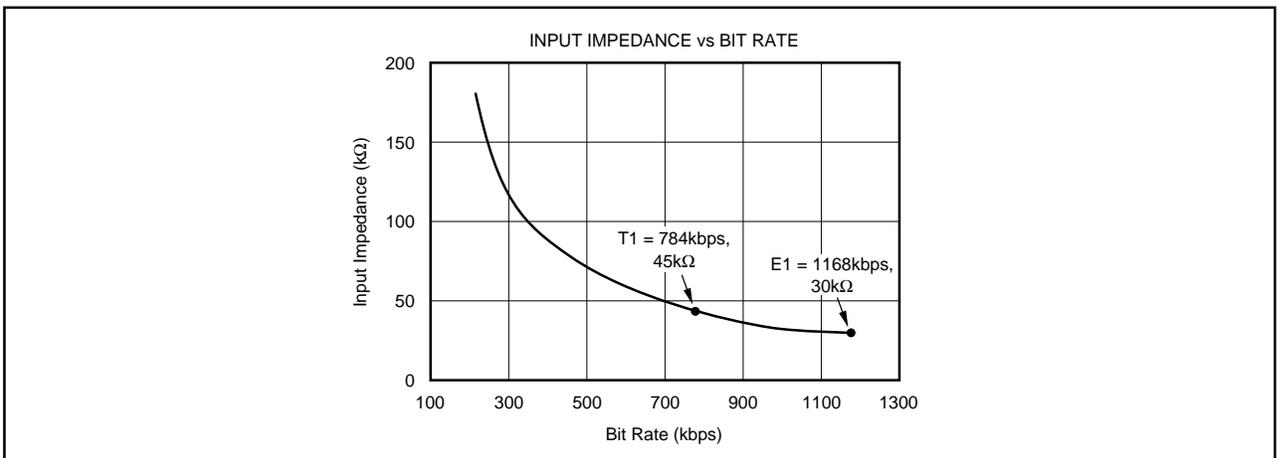
The curves shown below are measured at the line output of the HDSL transformer. Typical at 25°C,  $AV_{DD} = +5V$ ,  $DV_{DD} = +3.3V$ , unless otherwise specified.



CURVE 1. Upper Bound of Power Spectral Density Measured at Output of HDSL Transformer.



CURVE 2. Transmitted Pulse Template and Actual Performance as Measured at Transformer Output.



CURVE 3. Input Impedance of rxLINE and rxHYB.

# THEORY OF OPERATION

The transmit channel consists of a switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data through a serial interface and generates a standard 2B1Q output waveform. The output meets the pulse mask and power spectral density requirements defined in European Telecommunications Standards Institute document RTR/TM-03036 for E1 mode and in sections 6.2.1 and 6.2.2.1 of Bellcore technical advisory TA-NWT-001210 for T1 mode. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion).

The receive channel is designed around a fourth-order delta sigma A/D converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first order analog echo cancellation. A programmable gain amplifier with gains of -3dB to +9dB is also included. The delta sigma modulator operating at a 24X oversampling ratio produces a parallel 14-bit output at symbol rates up to 584kHz. The basic functionality of the AFE1115 is illustrated in Figure 1 shown below.

The receive channel operates by summing the two differential inputs, one from the line (rxLINE) and the other from the compromise hybrid (rxHYB). These two inputs are connected so that the hybrid signal is subtracted from the line signal. This connection is described in the paragraph titled "Echo Cancellation in the AFE". The equivalent gain for each input in the difference amp is one. The resulting signal then passes to a programmable gain amplifier which can be set for gains of -3dB through +9dB. The ADC converts the signal to a 14-bit digital word, rxD13-rxD0.

An independent VCXO control DAC and VCXO circuitry is also included on the chip. This VCXO is designed to be used

in remote units for clock recovery. The VCXO is formed with the on-board circuitry plus external crystal and varactor diodes. The VCXO control DAC receives control data through a serial interface which sets a voltage level at the output of the DAC. The DAC output controls the frequency of the VCXO. To achieve specified analog performance when using the VCXO, the crystal frequency of the VCXO must be 48x the baud rate.

## rxLOOP INPUT

rxLOOP is the loopback control signal. When enabled, the rxLINE+ and rxLINE- inputs are disconnected from the AFE. The rxHYB+ and rxHYB- inputs remain connected. Loopback is enabled by applying a positive signal (Logic 1) to rxLOOP.

## ECHO CANCELLATION IN THE AFE

The rxHYB input is designed to be subtracted from the rxLINE input for first order echo cancellation. To accomplish this, note that the rxLINE input is connected to the same polarity signal at the transformer (positive to positive and negative to negative) while the rxHYB input is connected to opposite polarity through the compromise hybrid (negative to positive and positive to negative) as shown in Figure 2.

## RECEIVE DATA CODING

The data from the receive channel A/D converter is coded in two's complement.

ANALOG INPUT	OUTPUT CODE (rxDATA)
Positive Full Scale	01111111111111
Mid Scale	00000000000000
Negative Full Scale	10000000000000

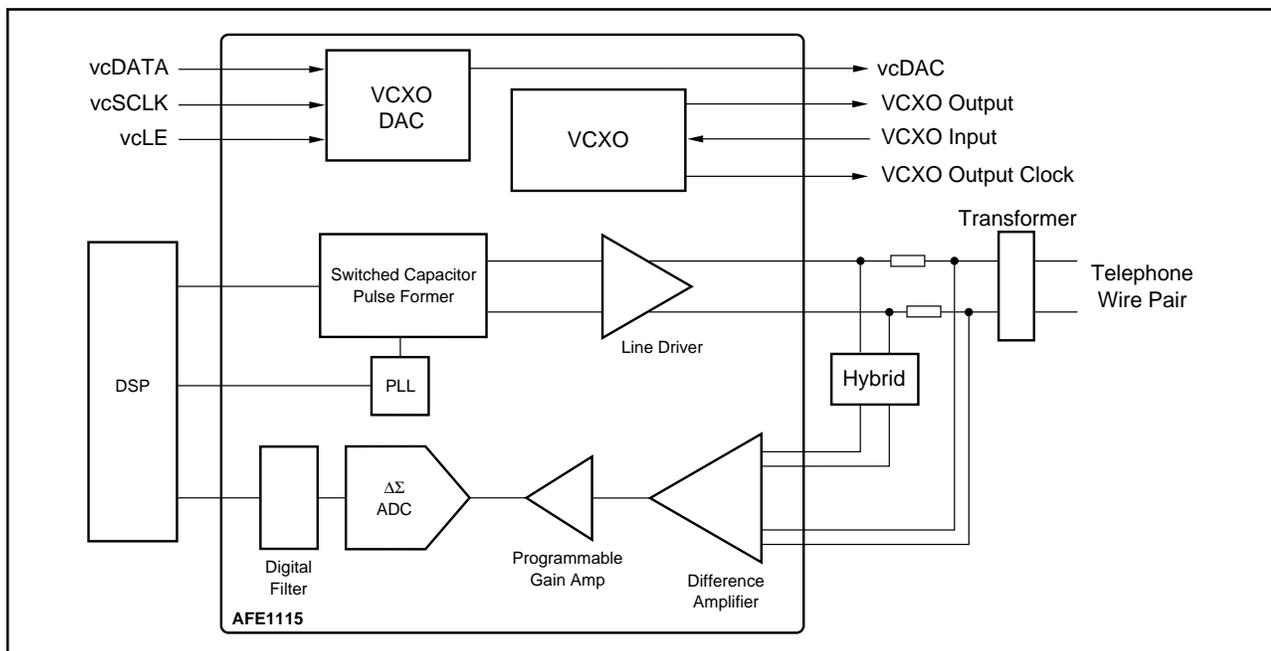


FIGURE 1. Functional Block Diagram of AFE1115 Circuit.

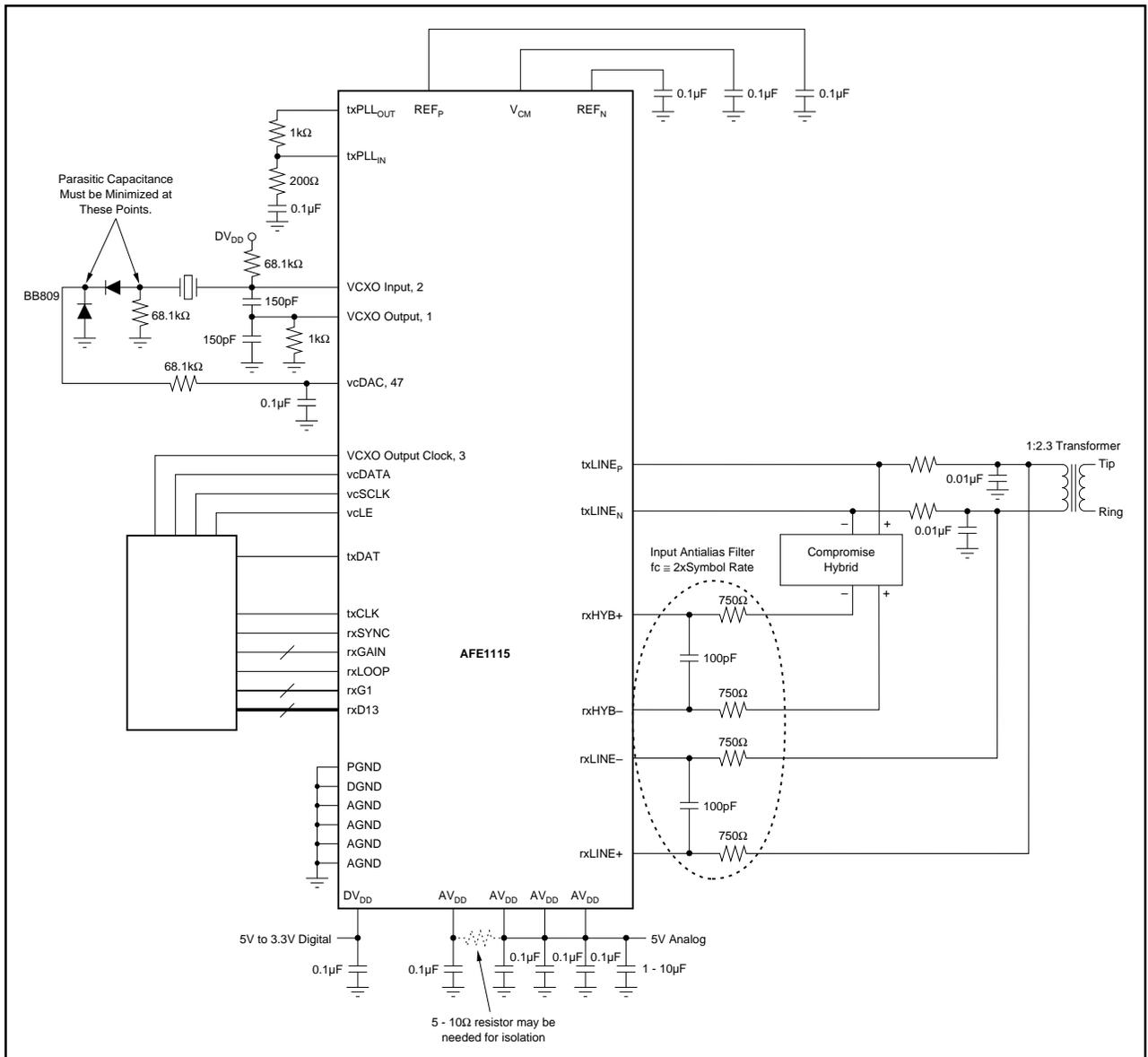


FIGURE 2. Basic Connection Diagram.

### RECEIVE CHANNEL PROGRAMMABLE GAIN AMPLIFIER

The gain of the amplifier at the input of the Receive Channel is set by two gain control pins, rxGAIN1 and rxGAIN0. The resulting gain between -3dB and +9dB is shown below.

rxGAIN1	rxGAIN0	GAIN
0	0	-3dB
0	1	+3dB
1	0	+9dB

### SCALEABLE DATA RATE

The AFE1115 scales operation with the clock frequency. All internal filters and the pulse former change frequency with the clock speed so that the unit can be used at different frequencies just by changing the clock speed.

### rxHYB AND rxLINE INPUT ANTI-ALIASING FILTERS

An external input anti-aliasing filter is needed on the hybrid and line inputs as shown in the Basic Connection Diagram above. The -3dB frequency of the input anti-aliasing filter for the rxLINE and rxHYB differential inputs should be approximately 1MHz for E1 and T1 symbol rates. Suggested values for the filter are 750Ω for each of the two input resistors and 100pF for the capacitor. Together the two 750Ω resistors and the 100pF capacitor result in a 3dB frequency of just over 1MHz. The 750Ω input resistors will result in a minimal voltage divider loss with the input impedance of the AFE1115.

For speed less than E1, the anti-aliasing filters will give best performance with 3dB frequency approximately equal to two times the symbol rate. For instance, a 3dB frequency of 400kHz may be used for a single line symbol rate of 196k symbols per second.

### rxHYB AND rxLINE INPUT COMMON-MODE OPTIONAL VOLTAGE

The AFE1115 will meet specifications with the application circuit shown in the Basic Connection Diagram (Figure 2) above. However, slightly improved performance may be obtained with the Hybrid input (rxHYB) and the Line input (rxLINE) set to a common mode voltage of 1.5V. The negative reference output pin (vrREFN, pin 40) provides a good 1.5V level to use to set the common-mode voltage. The circuit shown in Figure 3 can be used to set the common-mode voltage of the Line input to 1.5V.

A similar circuit can be used to set the Hybrid input to 1.5V. Another option for the Hybrid input is to design the external compromise hybrid so that the signal into the rsHYB inputs is centered at 1.5V. If the compromise hybrid circuit is AC coupled to the rxHYB inputs, an external pull-up resistor to vrREFN may be needed to center the input at 1.5V.

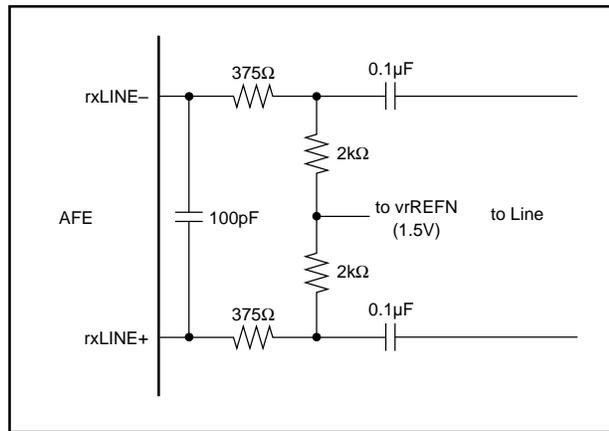


FIGURE 3. Optional rxLINE Input Common-mode Voltage Control.

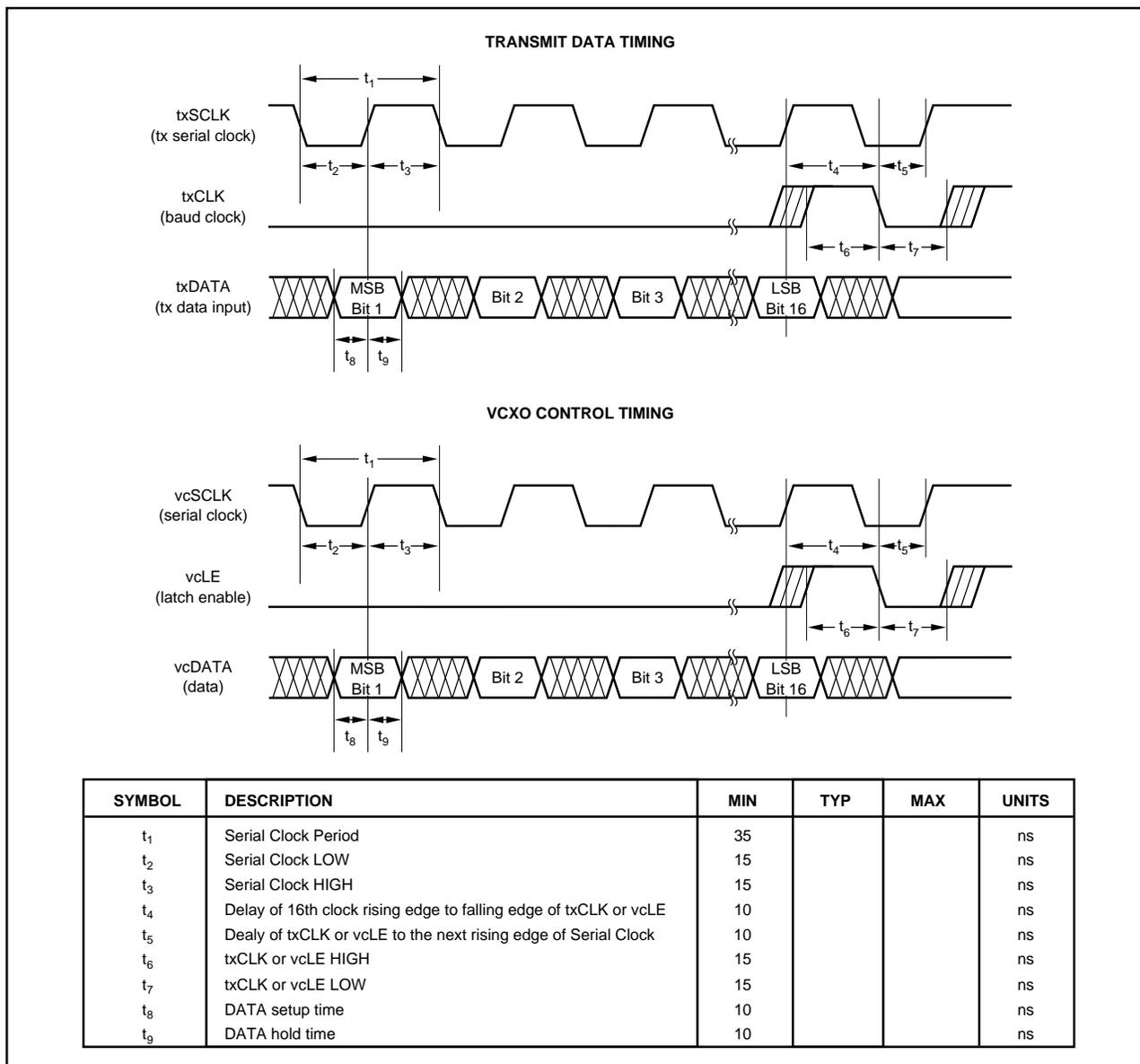


FIGURE 4. Timing Diagram.

## TRANSMIT SYMBOL DATA

During each symbol period transmit symbol data are sent to the AFE1115 in serial format through the txDATA input pin. A 16 bit word is sent to the AFE1115 to determine the symbol that is transmitted by the AFE1115. The symbol data is contained in the first three bits of the data, the remaining 13 bits of the 16 bit word are ignored.

The most significant bit (MSB) is the transmit enable bit. When the MSB is a logic 0, a zero symbol only is transmitted regardless of the state of the other two bits. When the MSB is a logic 1, bits 2 and 3 determine the symbol transmitted as shown in the table below.

MSB - BIT 1	BIT 2	BIT 3	2B1Q SYMBOL
0	X	X	0
1	1	1	+3
1	1	0	+1
1	0	1	-1
1	0	0	-3

TABLE I. Transmit Symbol Data (txDATA). X = Don't Care.

## VCXO CONTROL D/A CONVERTER DATA

During each symbol period VCXO control D/A converter data is sent to the AFE1115 in serial format through the vcDATA input pin. A 16 bit word is sent to the AFE1115 to determine the output of the VCXO control D/A converter. The VCXO control D/A converter is connected to the VCXO circuit to control the VCXO frequency. The D/A converter input is contained in the first eight bits of the data, the remaining eight bits of the 16 bit word are ignored.

INPUT CODE (vcDATA) MSB	ANALOG OUTPUT
01111111XXXXXXXX	Negative Full Scale (+0.5V)
00000000XXXXXXXX	Mid Scale (+2.5V)
10000000XXXXXXXX	Positive Full Scale (+4.5V)

TABLE II. VCXO Control DAC Output. X = Don't Care.

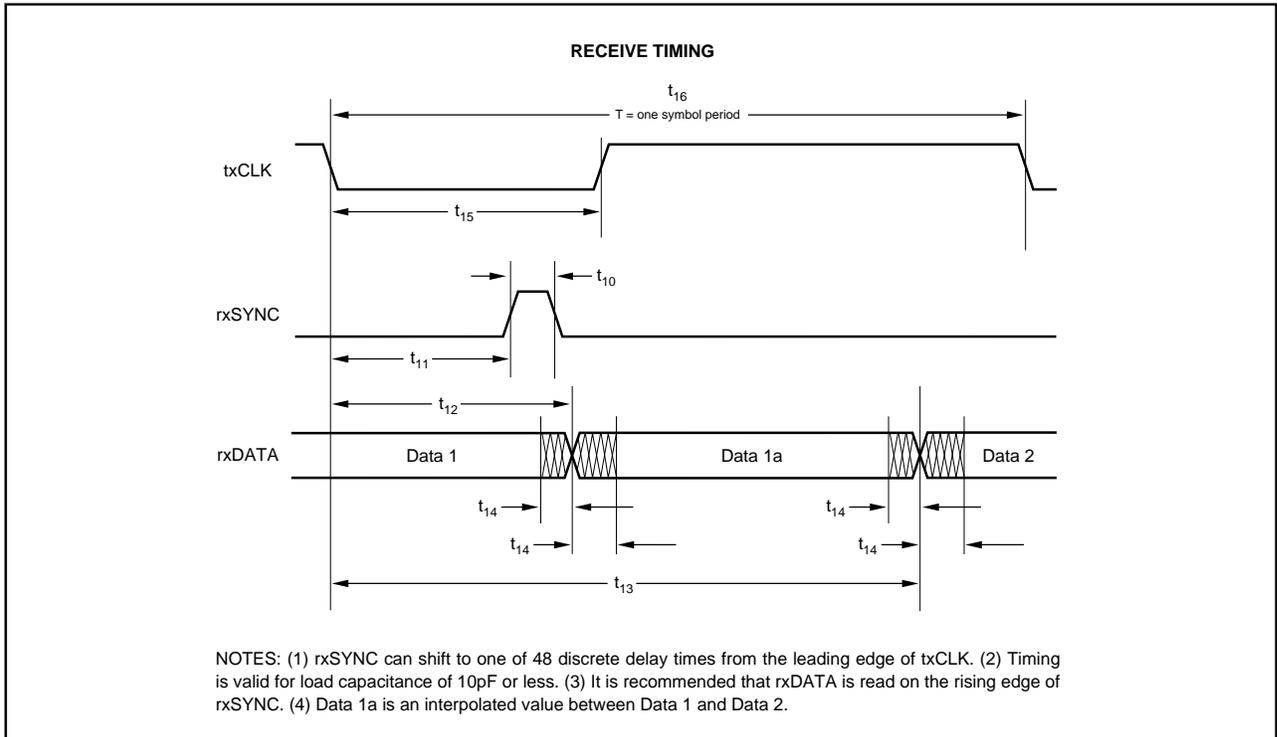


FIGURE 5. Receive Timing Diagram.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	VALUE
$t_{10}$	rxSYNC Pulse Width	$T/24$			
$t_{11}$	Delay of rxSYNC from rising edge of txCLK, $n = 0$ to 47	$nT/48 - T/96$		$nT/48 + T/96$	
$t_{12}$	Nominal Time at Which rxDATA Changes from Data 1 to Data 1a		$(n + 1.5) T/48$		
$t_{13}$	Nominal Time at Which rxDATA Changes from Data 1a to Data 2		$(n + 25.5) T/48$		
$t_{14}$	Uncertainty of $t_{12}$ and $t_{13}$			20	ns
$t_{15}$	txCLK Pulse Width	$T/16$		$15T/16$	
$t_{16}$	Symbol Period, T	1.7		10.2	$\mu$ s

TABLE III. Receive Timing ( $n =$  Delay Increments from txCLK).

## RECEIVE TIMING

The rxSYNC signal controls portions of the A/D converter's decimation filter and the data output timing of the A/D converter. It is generated at the symbol rate by the user and must be synchronized with txCLK. The leading edge of rxSYNC can occur at the leading edge of txCLK or it can be shifted by the user in increments of 1/48 of a symbol period to one of 47 discrete delay times after the leading edge of txCLK.

The bandwidth of the A/D converter decimation filter is equal to one half of the symbol rate. The A/D converter data output rate is 2X the symbol rate. The specifications of the AFE1115 assume that one A/D converter output is used per symbol period and the other output is ignored. The Receive Timing Diagram above suggests using the rxSYNC pulse to read the first data output in a symbol period. Either data output may be used. Both data outputs may be used for more flexible post-processing.

## DISCUSSION OF SPECIFICATIONS

### UNCANCELLED ECHO

The key measure of transceiver performance is uncancelled echo. This measurement is made as shown in the diagram of Figure 6 and the measurement is made as follows. The AFE is connected to an output circuit including a typical 1:2.3 line transformer. The line is simulated by a 135Ω resistor.

Symbol sequences are generated by the tester and applied both to the AFE and to the input of an adaptive filter. The output of the adaptive filter is subtracted from the AFE output to form the uncancelled echo signal. Once the filter taps have converged, the RMS value of the uncancelled echo is calculated. Since there is no far-end signal source or additive line noise, the uncancelled echo contains only noise and linearity errors generated in the transmitter and receiver.

The data sheet value for uncancelled echo is the ratio of the RMS uncancelled echo (referred to the receiver input through the receiver gain) to the nominal transmitted signal (13.5dBm into 135Ω, or 1.74Vrms). This echo value is measured under a variety of conditions: with loopback enabled (line input disabled); with loopback disabled under all receiver gain ranges; and with the line shorted ( $S_1$  closed in Figure 6).

### POWER DISSIPATION

Approximately 75% of the power dissipation in the AFE1115 is in the analog circuitry, and this component does not change with clock frequency. However, the power dissipation in the digital circuitry does decrease with lower clock frequency. In addition, the power dissipation in the digital section is decreased with operation from a smaller supply voltage, such as 3.3V. (The analog supply, must remain in the range 4.75V to 5.25V.)

The power dissipation listed in the specifications section applies under these normal operating conditions: 5V Analog Power Supply; 3.3V Digital Power Supply; E1 baud rate;

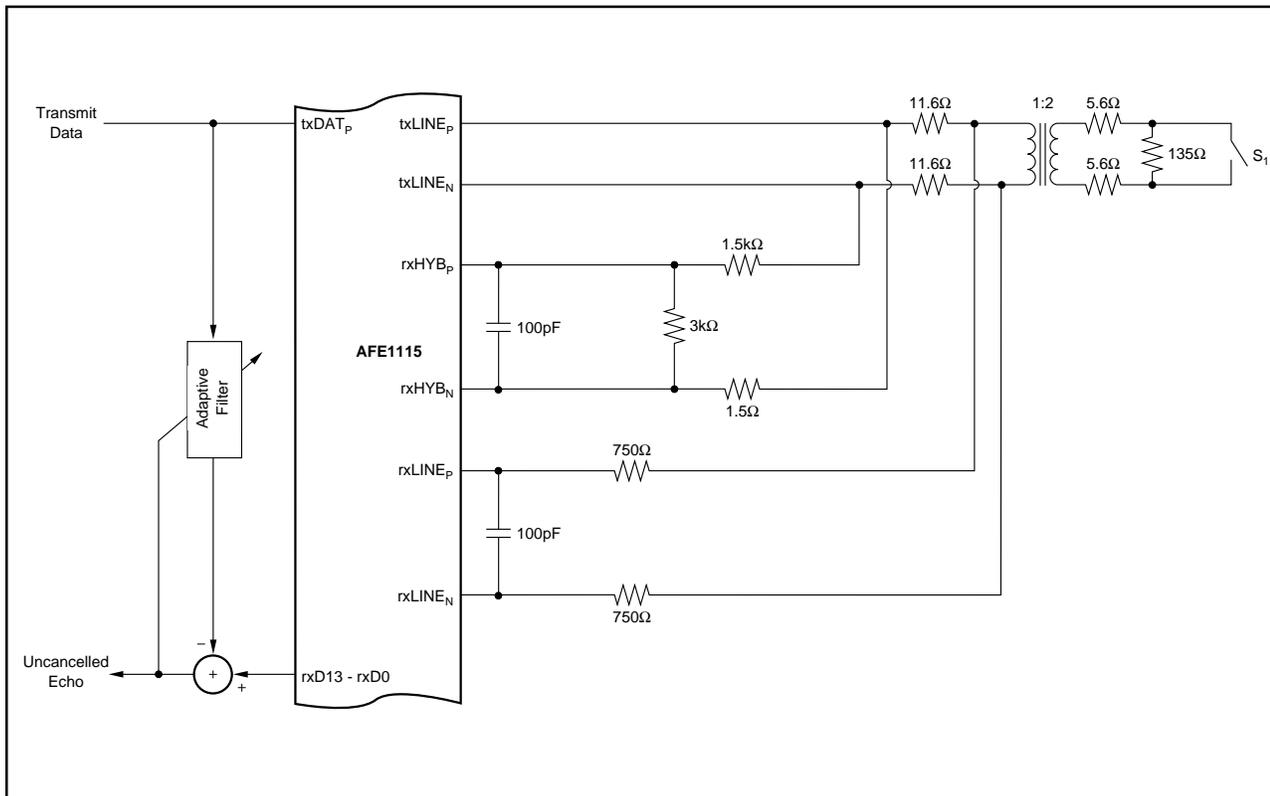


FIGURE 6. Uncancelled Echo Test Diagram.

13.5dBm delivered to the line; and a pseudo-random equiprobable sequence of HDSL pulses. The power dissipation specifications includes all power dissipated in the AFE1115, it does not include power dissipated in the external load. The external power is 16.5dBm, 13.5dBm to the line and 13.5dBm to the impedance matching resistors. The external load power of 16.5dBm is 45mW. The typical power dissipation in the AFE1115 under various conditions is shown in

BIT RATE PER AFE1115 (Symbols/sec)	DVDD (V)	TYPICAL POWER DISSIPATION IN THE AFE1115 (mW)
1168 (E1)	3.3	300
1168 (E1)	5	350
784 (T1)	3.3	290
784 (T1)	5	330
292 (1/4 E1)	3.3	280
292 (1/4 E1)	5	300

TABLE IV. Typical Power Dissipation.

Table IV.

## LAYOUT

The analog front end of an HDSL system has a number of conflicting requirements. It must accept and deliver digital outputs at fairly high rates of speed, generate a VCXO clock, phase-lock to a high-speed digital clock, and convert the line input to a high-precision (14-bit) digital output. Thus, there are really four sections of the AFE1115: the digital section, the phase-locked loop, the VCXO and the analog section.

### DIGITAL LAYOUT

The power supply for the digital section of the AFE1115 can range from 3.3V to 5V. This supply should be decoupled to digital ground with a ceramic 0.1μF capacitor placed as close as possible to digital ground (DGND, pin 16) and digital power (DV<sub>DD</sub>, pin 17). Ideally, both a digital power supply plane and a digital ground plane should run to and underneath the digital pins of the AFE1115 (pins 7 through 30). However, DV<sub>DD</sub> may be supplied by a wide printed circuit board trace. A digital ground plane underneath all digital pins is strongly recommended. The VCXO circuit needs special attention for layout. There is a portion of the external VCXO circuitry which needs to be as far away as possible from a ground or power plane or other traces. See the discussion below in the section titled VCXO Circuit and Layout.

### ANALOG LAYOUT

The phase-locked loop is powered from AV<sub>DD</sub> (pin 50) and its ground is referenced to AGND (pin 49). Note that AV<sub>DD</sub> must be in the 4.75V to 5.25V range. This portion of the AFE1115 should be decoupled with both 10μF Tantalum capacitor and a 0.1μF ceramic capacitor. The ceramic capacitor should be placed as close to the AFE1115 as possible.

The placement of the Tantalum capacitor is not as critical, but should be close to the pin. In each case, the capacitor should be connected between AV<sub>DD</sub> and AGND (pins 49 and 50). The capacitors should be placed in quiet analog areas rather than noisy digital areas.

In most systems, it will be natural to derive AV<sub>DD</sub> for the phase-locked loop (PLL) from the AV<sub>DD</sub> supply. A 5Ω to 10Ω resistor should be used to connect PLL AV<sub>DD</sub> (pin 49) to the analog supply. This resistor in combination with the 10μF capacitor form a lowpass filter—keeping glitches on the analog supply from affecting the phase locked loop. Ideally, the phase-locked loop power supply would originate from the analog supply (via the 5Ω to 10Ω resistor) near the power connector for the printed circuit board. Likewise, the PLL ground should connect to a large PCB trace or small ground plane which returns to the power supply connector underneath the PLL AV<sub>DD</sub> supply path. The PLL “ground plane” should also extend underneath PLL<sub>IN</sub> and PLL<sub>OUT</sub> (pins 51 and 52).

The remaining portion of the AFE1115 should be considered analog. The four non-PLL AGND pins (pins 36, 37, 42, and 46) should be connected directly to a common analog ground plane and all non-PLL AV<sub>DD</sub> pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to the power supply.

Ideally, all ground planes and traces and all power planes and traces should return to the power supply connector before being connected together (if necessary). Each ground and power pair should be routed over each other, should not overlap any portion of another pair, and the pairs should be separated by a distance of at least 0.25 inch (6mm). One exception is that the digital and analog ground planes should be connected together underneath the AFE1115 by a small trace.

## VCXO CIRCUIT AND LAYOUT

The VCXO circuitry is shown in Figure 7. The basic VCXO circuit consists of on-chip control DAC, amplifiers, Schmidt triggers, and clock buffer along with an external crystal and varactor diodes. The control DAC output (vcDAC) varies the capacitance of the varactor diodes (D1 and D2), which controls the frequency at which the crystal circuit oscillates. The buffered clock output is available at pin 3, VCXO Clock Output.

**Important Note:** To achieve specified analog performance when using VCXO, the crystal frequency of the VCXO must be 48x the baud rate. In addition, the txCLK and the rxSYNC control signals must be derived from the VCXO clock so that the edges of the control signal are synchronized with the 48x crystal frequency. If these recommendations are followed, the key internal analog decisions are made at the time of minimum noise. As an example, for an E1 rate of 1168kbps, the symbol rate is 584k symbols per second. In this case the VCXO crystal frequency should be 48 x 584k = 28.032MHz. Likewise, for T1, the crystal frequency should be 18.816MHz.

The performance of the VCXO is critically dependent on the external components and printed circuit board layout that is used. The varactor diodes and the crystal are particularly important components.

The printed circuit board layout containing the two varactor diodes, D1 and D2, in the VCXO external circuitry is critical to the performance of the VCXO. In particular, the two connection points of the varactor diodes shown in the Figure 7 must have very low parasitic capacitance to ground to achieve the best tuning range possible. To achieve lowest parasitic capacitance to ground, there must be no ground plane or other PCB traces near these two points. Ground planes and other traces should be kept 1 cm away from these two points where possible.

Figure 8 shows an example of a printed circuit board layout of the sensitive VCXO circuitry for the circuit shown in Figure 7. There should be no ground planes, power planes or other traces in the white area indicated around the two sensitive points. The balance of the circuit board should be covered by ground planes where possible. With the circuit shown in Figure 7, these typical specifications were achieved.

Pull Range at 20MHz	±125ppm
Frequency Range of Crystal that can be used	10MHz to 28MHz
Crystal Frequency	48x baud rate

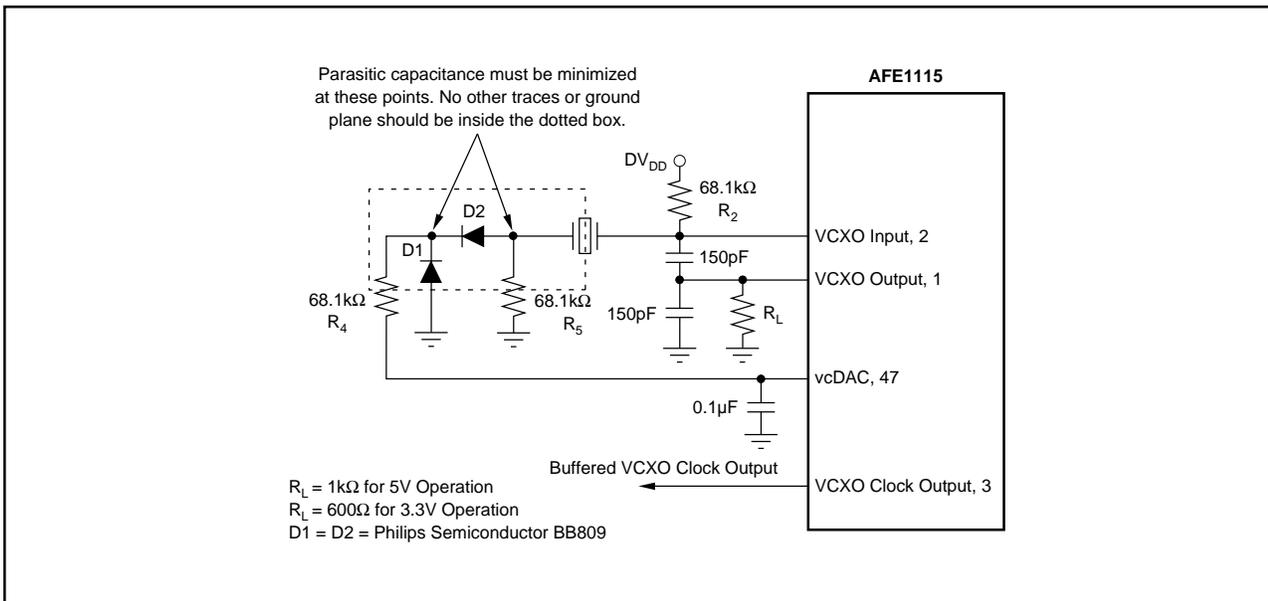


FIGURE 7. VCXO Circuitry.

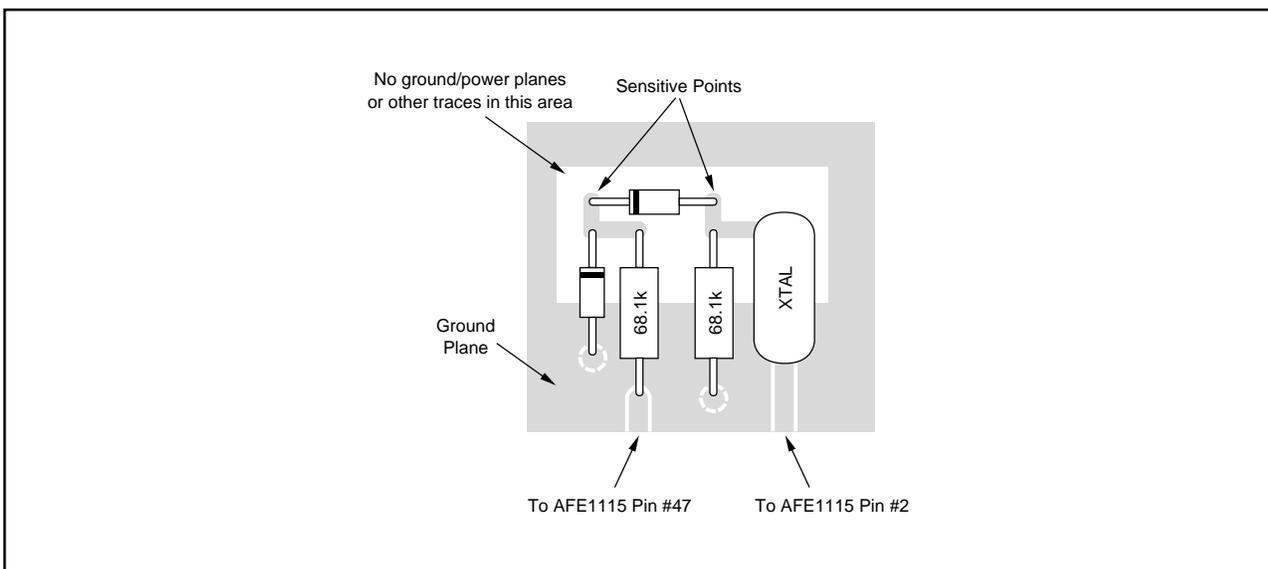


FIGURE 8. VCXO Circuit Layout, Approximately Two Times Actual Size.