BURR-BROWN®

ADS7842

12-Bit, 4-Channel Parallel Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SINGLE SUPPLY: 2.7V to 5V
- 4-CHANNEL INPUT MULTIPLEXER
- UP TO 200kHz SAMPLING RATE
- FULL 12-BIT PARALLEL INTERFACE
- ±1 LSB INL AND DNL
- GUARANTEED NO MISSING CODES
- 72dB SINAD
- LOW POWER: 2mW
- 28-LEAD SSOP PACKAGE

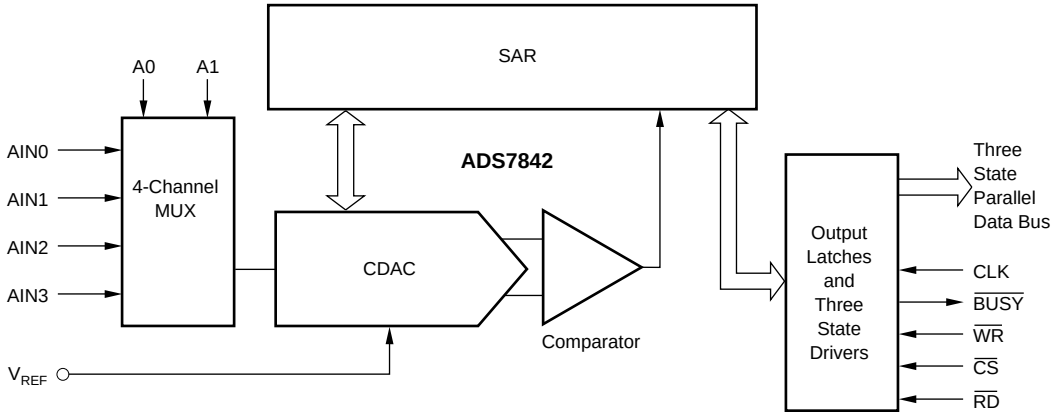
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTS
- LABORATORY EQUIPMENT

DESCRIPTION

The ADS7842 is a complete, 4-channel, 12-bit analog-to-digitial converter (ADC). It contains a 12-bit, capacitor-based, SAR A/D with a sample-and-hold amplifier, interface for microprocessor use and parallel, three-state output drivers. The ADS7842 is specified at a 200kHz sampling rate while dissipating only 2mW of power. The reference voltage can be varied from 100mV to V_{CC} with a corresponding LSB resolution from 24µV to 1.22mV. The ADS7842 is guaranteed down to 2.7V operation.

Low power, high speed and an on-board multiplexer make the ADS7842 ideal for battery-operated systems such as portable, multi-channel dataloggers and measurement equipment. The ADS7842 is available in a 28-lead SSOP package and is guaranteed over the –40°C to +85°C temperature range.



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SPECIFICATIONS: +5V

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7842E			ADS7842EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Full-Scale Input Span		0		V_{REF}	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		12			12			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				200			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 5Vp-p at 10kHz		–78	–72		–80	–76	dB
Signal-to-(Noise + Distortion)	V_{IN} = 5Vp-p at 10kHz	68	71		70	72		dB
Spurious Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz	72	79		76	81		dB
Channel-to-Channel Isolation	V_{IN} = 5Vp-p at 50kHz		120			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			40	100		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	3.0		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
External Clock		0.2		8	*		*	MHz
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			550	900		*	*	µA
	f_{SAMPLE} = 12.5kHz		300			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				4.5			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7842E.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +5.0V, one LSB is 1.22mV. (2) First five harmonics of the test frequency. (3) Power-down mode at end of conversion when $\overline{WR}$, $\overline{CS}$, and $\overline{BUSY}$ conditions have all been met. Refer to Table I of this data sheet.

SPECIFICATION: +2.7V

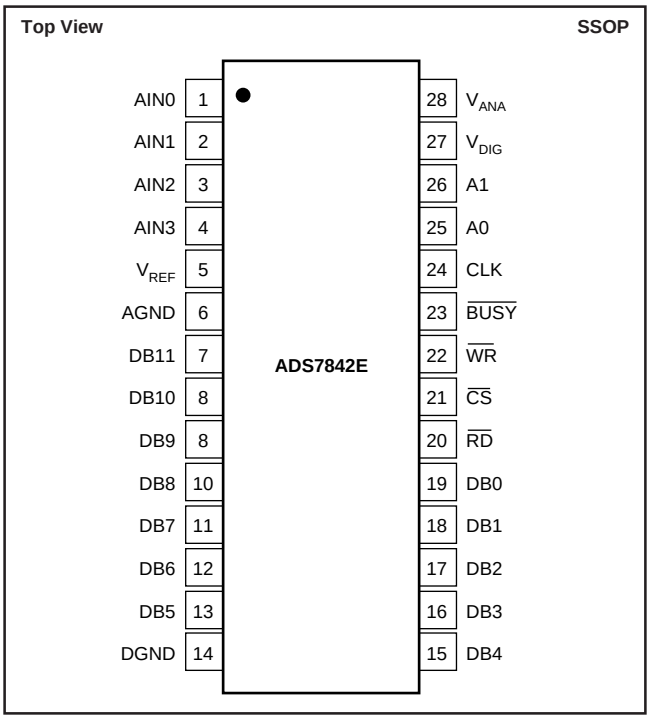
At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7842E			ADS7842EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Full-Scale Input Span		0		V_{REF}	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			12			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±5			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				125			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 2.5Vp-p at 10kHz		–77	–70		–79	–74	dB
Signal-to-(Noise + Distortion)	V_{IN} = 2.5Vp-p at 10kHz	68	71		70	72		dB
Spurious Free Dynamic Range	V_{IN} = 2.5Vp-p at 10kHz	72	78		76	80		dB
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			13	40		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	$+V_{CC}$ • 0.7		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
External Clock		0.2		8	*		*	MHz
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			280	650		*	*	µA
	f_{SAMPLE} = 12.5kHz		220			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				1.8			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7842E.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 610mV. (2) First five harmonics of the test frequency. (3) Power-down mode at end of conversion when $\overline{WR}$, $\overline{CS}$, and $\overline{BUSY}$ conditions have all been met. Refer to Table I of this data sheet.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to +6V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	AIN0	Analog Input Channel 0
2	AIN1	Analog Input Channel 1
3	AIN2	Analog Input Channel 2
4	AIN3	Analog Input Channel 3
5	V_{REF}	Voltage Reference Input. See Specifications Tables for ranges.
6	AGND	Analog Ground
7	DB11	Data Bit 11 (MSB)
8	DB10	Data Bit 10
9	DB9	Data Bit 9
10	DB8	Data Bit 8
11	DB7	Data Bit 7
12	DB6	Data Bit 6
13	DB5	Data Bit 5
14	DGND	Digital Ground
15	DB4	Data Bit 4
16	DB3	Data Bit 3
17	DB2	Data Bit 2
18	DB1	Data Bit 1
19	DB0	Data Bit 0 (LSB)
20	$\overline{RD}$	Read Input. Active LOW. Reads the data outputs in combination with $\overline{CS}$.
21	$\overline{CS}$	Chip Select Input. Active LOW. The combination of $\overline{CS}$ taken LOW and $\overline{WR}$ taken LOW initiates a new conversion and places the outputs in the tri-state mode.
22	$\overline{WR}$	Write Input. Active LOW. Starts a new conversion and selects an analog channel via address inputs A0 and A1, in combination with $\overline{CS}$.
23	$\overline{BUSY}$	$\overline{BUSY}$ goes LOW and stays LOW during a conversion. $\overline{BUSY}$ rises when a conversion is complete and enables the parallel outputs.
24	CLK	External Clock Input. The clock speed determines the conversion rate by the equation $f_{CLK} = 16 \cdot f_{SAMPLE}$.
25, 26	A0, A1	Address Inputs. Selects one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of either $\overline{RD}$ or $\overline{WR}$.
		A0 / A1 / Channel Selected: 0 0 AIN0; 0 1 AIN1; 1 0 AIN2; 1 1 AIN3
27	V_{DIG}	Digital Supply Input. Nominally +5V.
28	V_{ANA}	Analog Supply Input. Nominally +5V.

PACKAGE/ORDERING INFORMATION

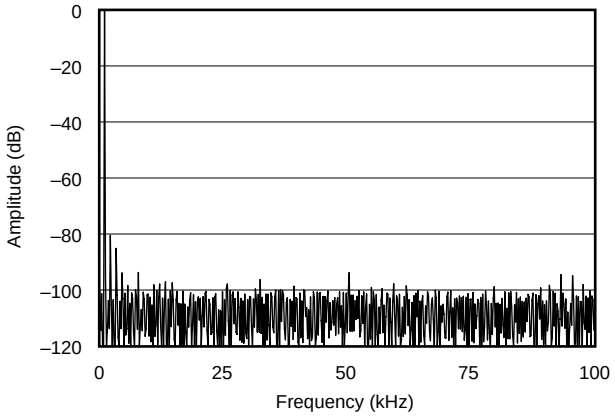
PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	SINAD (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[1]	ORDERING NUMBER[2]	TRANSPORT MEDIA
ADS7842E	±2	68	–40°C to +85°C	28-Lead SSOP	324	ADS7842E	Rails
"	"	"	"	"	"	ADS7842E/1K	Tape and Reel
ADS7842EB	±1	70	–40°C to +85°C	28-Lead SSOP	324	ADS7842EB	Rails
"	"	"	"	"	"	ADS7842EB/1K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 1000 pieces of "ADS7842E/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

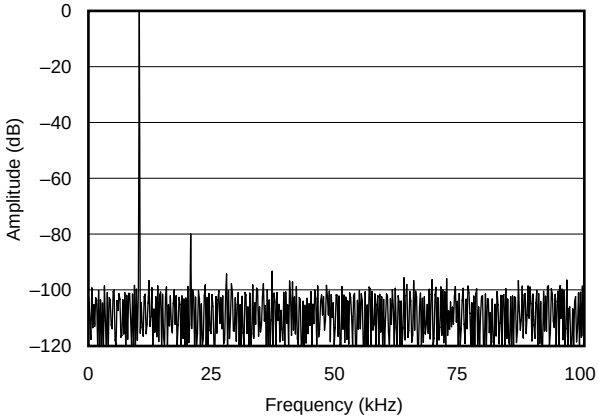
TYPICAL PERFORMANCE CURVES: +5V

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

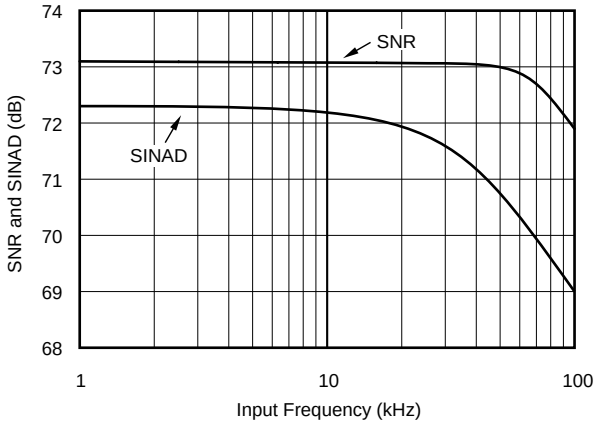
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,123Hz, –0.2dB)



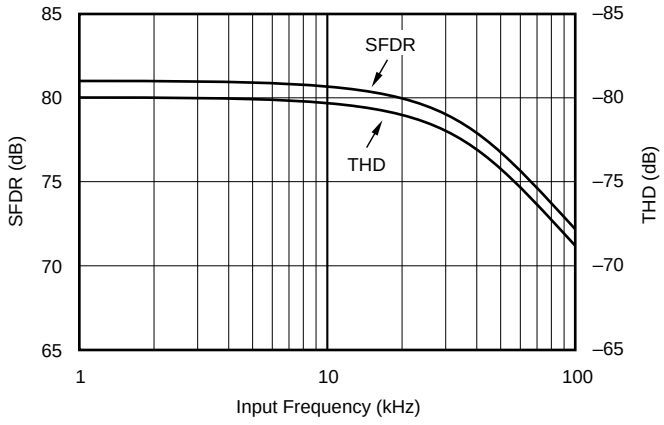
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.3kHz, –0.2dB)



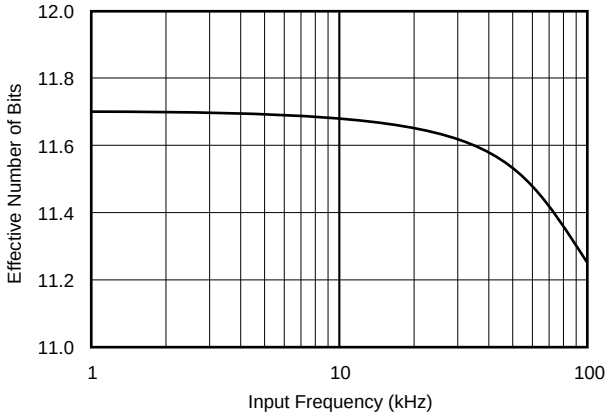
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



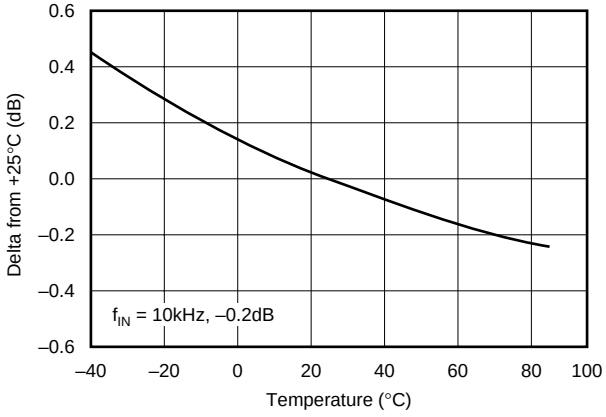
SPURIOUS FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



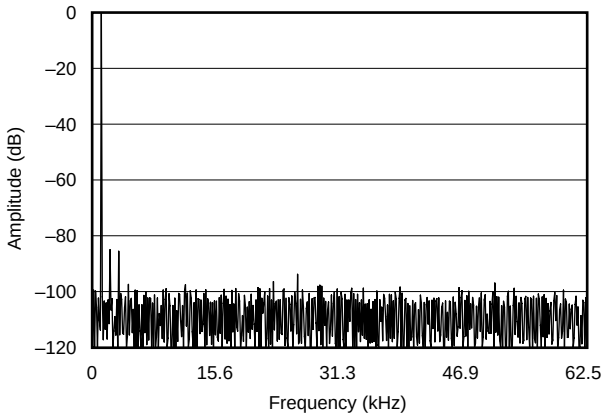
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



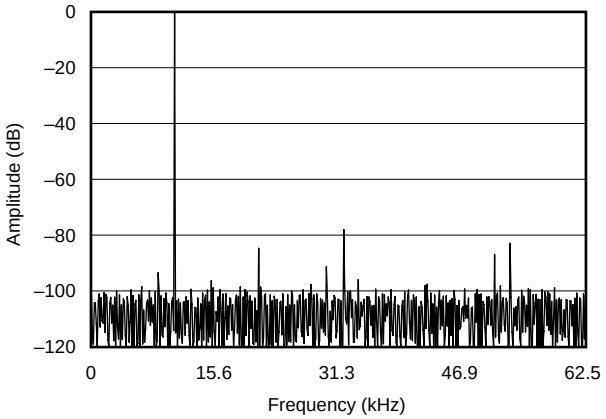
TYPICAL PERFORMANCE CURVES: +2.7V

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

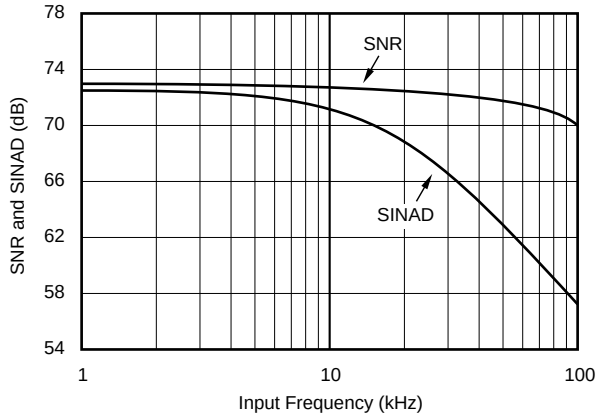
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,129Hz, –0.2dB)



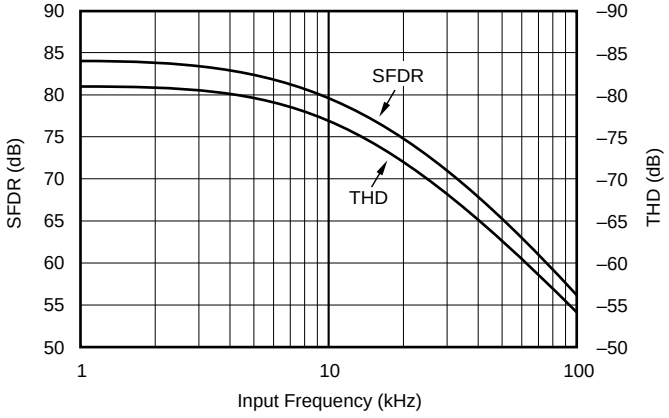
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.6kHz, –0.2dB)



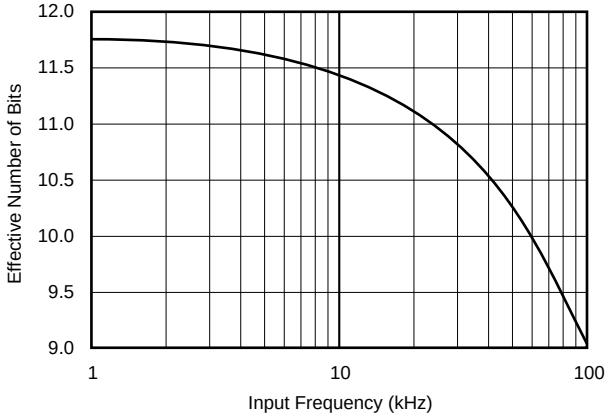
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



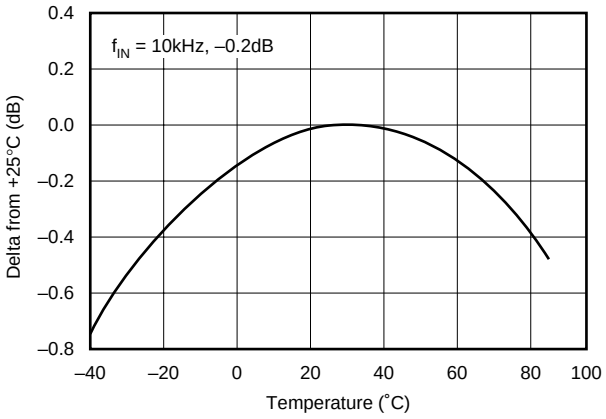
SPURIOUS FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



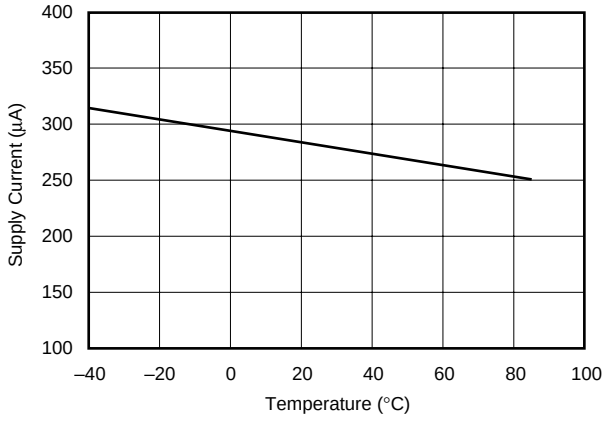
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



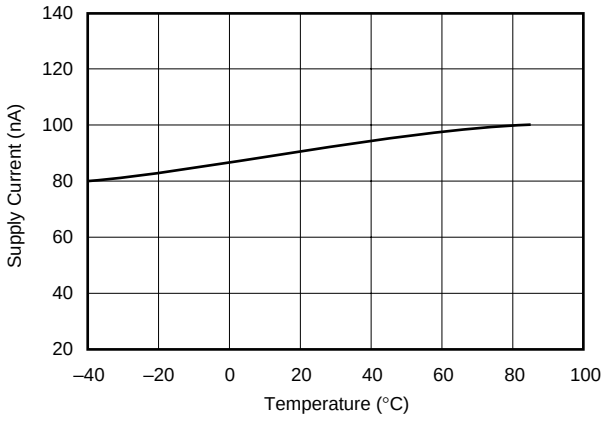
TYPICAL PERFORMANCE CURVES: +2.7V (CONT)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

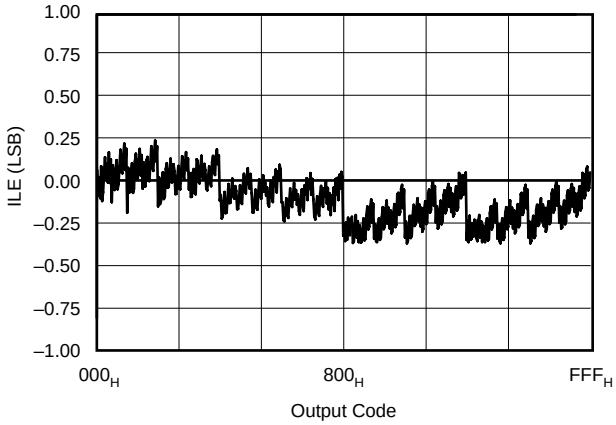
SUPPLY CURRENT vs TEMPERATURE



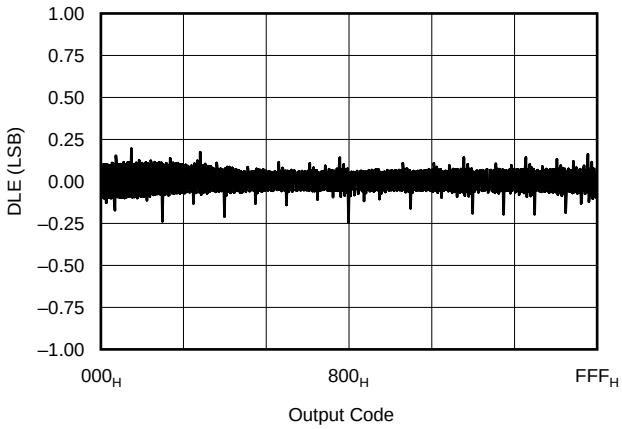
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



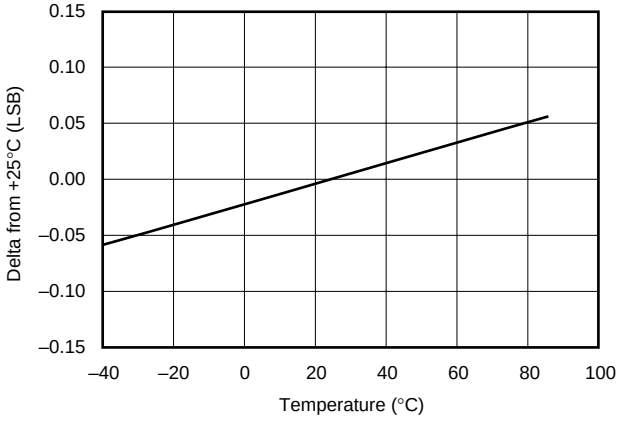
INTEGRAL LINEARITY ERROR vs CODE



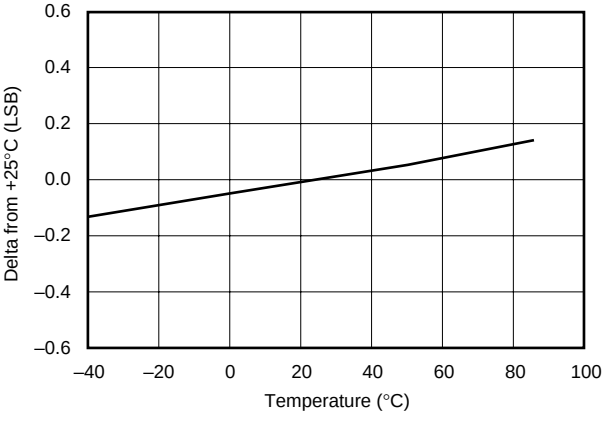
DIFFERENTIAL LINEARITY ERROR vs CODE



CHANGE IN GAIN vs TEMPERATURE



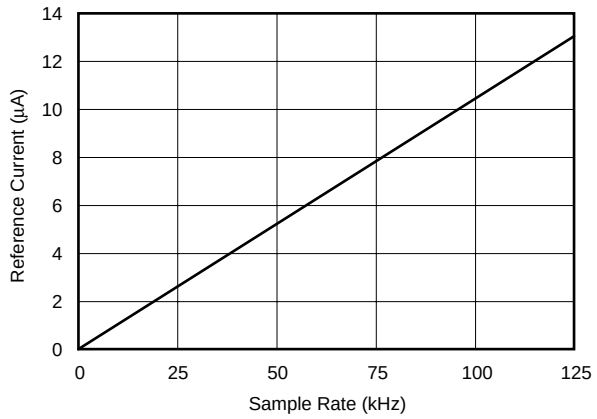
CHANGE IN OFFSET vs TEMPERATURE



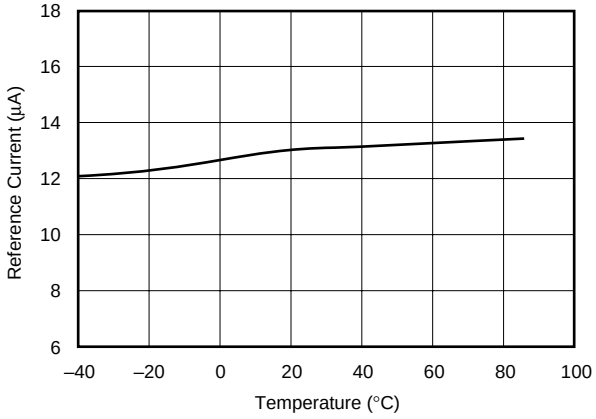
TYPICAL PERFORMANCE CURVES: +2.7V (CONT)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

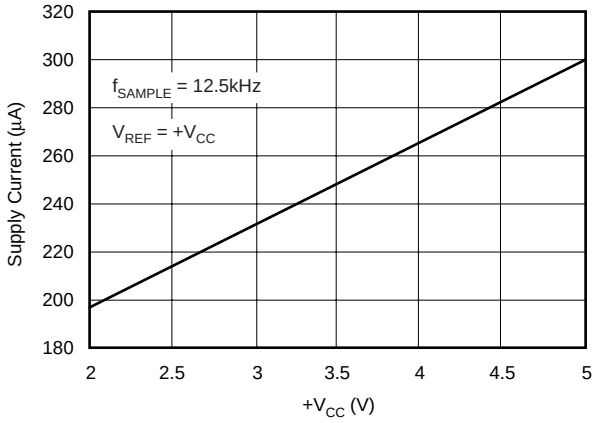
REFERENCE CURRENT vs SAMPLE RATE



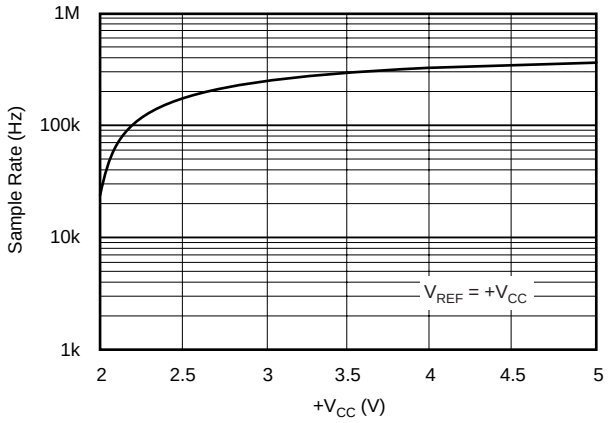
REFERENCE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs $+V_{CC}$



MAXIMUM SAMPLE RATE vs $+V_{CC}$



THEORY OF OPERATION

The ADS7842 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µs CMOS process.

The basic operation of the ADS7842 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 100mV and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7842.

ANALOG INPUTS

The ADS7842 features four, single-ended inuts. The input current into each analog input depends on input voltage and sampling rate. Essentially, the current into the device must charge the internal hold capacitor during the sample period. After this capacitance has fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 12-bit settling level within the same period, which can be as little as 350ns in some operating modes. While the converter is in the hold mode, or after the sampling capacitor has been fully charged, the input impedance of the analog input is greater than 1GΩ.

EXTERNAL CLOCK

The ADS7842 requires an external clock to run the conversion process. This clock can vary between 200kHz (12.5kHz throughput) and 3.2MHz (200kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 50ns and the clock period is at least 125ns. The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7842.

BASIC OPERATION

Figure 1 shows the simple circuit required to operate the ADS7842 with Channel 0 selected. A conversion can be initiated by bringing the $\overline{WR}$ pin (pin 22) LOW for a minimum of 25ns. $\overline{BUSY}$ (pin 23) will output a LOW during the conversion process and rises only after the conversion is complete. The 12 bits of output data will be valid on pin 7-13 and 15-19 following the rising edge of $\overline{BUSY}$.

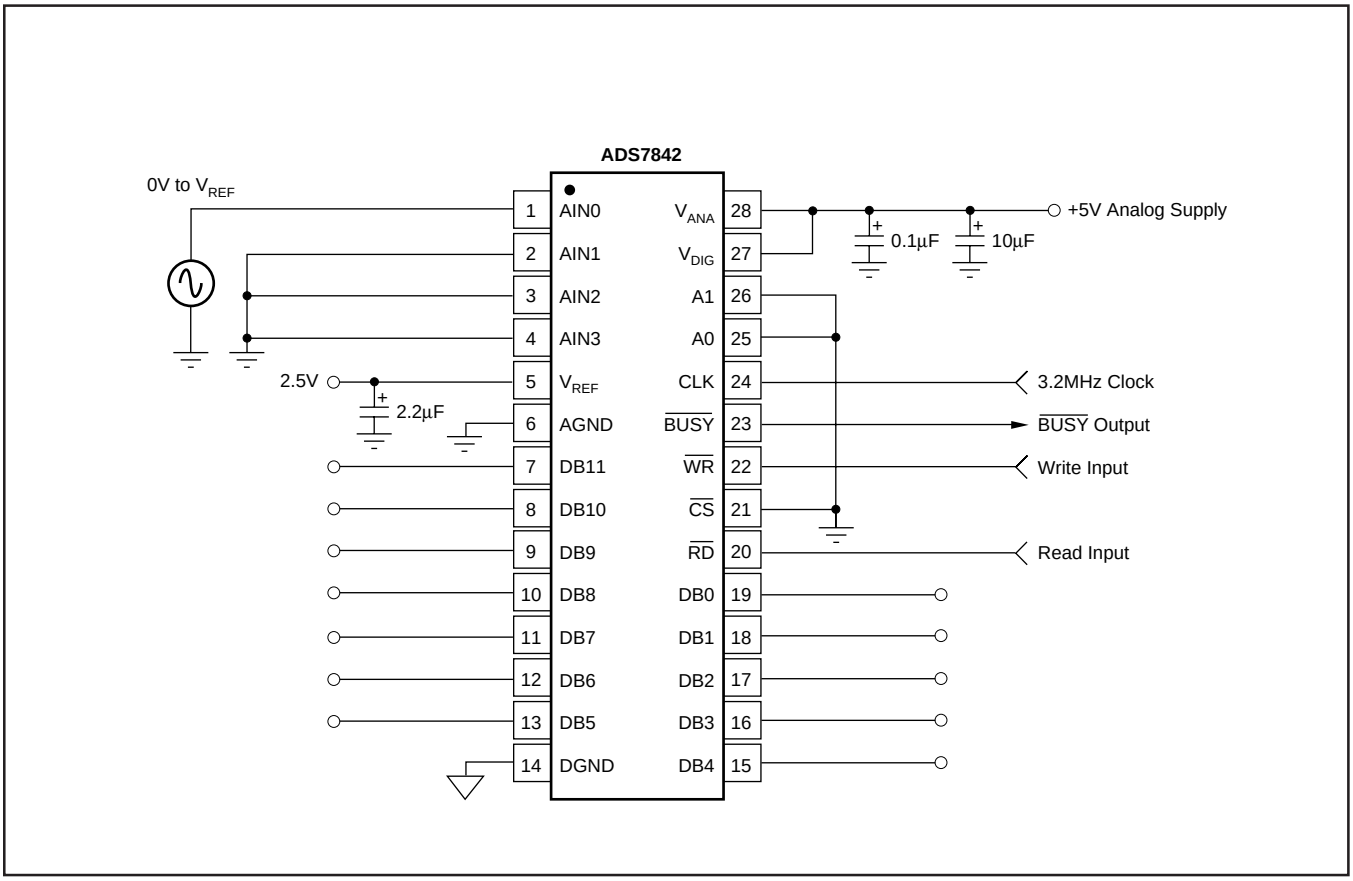


FIGURE 1. Basic Operation of the ADS7842.

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1, and $\overline{CS}$. The ADS7842 will enter the conversion mode on the first rising edge of the external clock following the $\overline{WR}$ pin going LOW. The ADS7842 will start the conversion on the 1st clock cycle. The MSB will be approximated by the Capacitive Digital-to-Analog Converter (CDAC) on the 1st clock cycle, the 2nd MSB on the 2nd cycle, and so on until the LSB has been decided on the 12th clock cycle. The $\overline{BUSY}$ output will go LOW 20ns after the falling edge of the $\overline{WR}$ pin. The $\overline{BUSY}$ output will return HIGH just after the ADS7842 has finished a conversion and the data will be valid on pins 7 - 19. The rising edge of $\overline{BUSY}$ can be used to latch the data. It is recommended that the data be read immediately after each conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance. See Figure 2.

READING DATA

Data from the ADS7842 will appear at pins 7 - 13 and 15 - 19. The MSB will output on pin 7 while the LSB will output on pin 19. The outputs are coded in Straight Binary (with 0V = $000_H$and V_{REF} = FFF_H, see Table IV). Following a conversion, the $\overline{BUSY}$ pin will go HIGH. After $\overline{BUSY}$ goes HIGH, the $\overline{CS}$ and $\overline{RD}$ pins may be brought LOW to enable the 12-bit output bus. $\overline{CS}$ and $\overline{RD}$ must be held LOW for at least 25ns seconds following $\overline{BUSY}$ HIGH. Data will be valid 25ns seconds after the falling edge of both $\overline{CS}$ and $\overline{RD}$. The output data will remain valid for 25ns seconds following the rising edge of both $\overline{CS}$ and $\overline{RD}$. See Figure 4 for the read cycle timing diagram.

POWER-DOWN MODE

The ADS7842 has two different power-down modes: sleep and nap. In the sleep mode, all analog and digital circuitry have been switched off. In the nap mode, the voltage reference remains on while all remaining circuitry is switched off. The simplest way to use the power-down mode is following a conversion. After a conversion has finished and $\overline{BUSY}$ has returned HIGH, $\overline{CS}$ and $\overline{RD}$ must be brought LOW for a minimum of 25ns. When $\overline{CS}$ and $\overline{RD}$ are both returned HIGH, the ADS7842 will enter the power-down mode on the rising edge of the $\overline{RD}$ pin. Depending on the status of the A0 and A1 address pins, the ADS7842 will either enter the nap or sleep mode (refer to Table III and Figure 5 for more details).

The typical supply current of the ADS7842 with a 5V supply and a 500kHz sampling rate is 2.6mA. In the nap mode, the typical supply current is 600µA. In the sleep mode, the current is reduced to 10µA typically.

In order to return the ADS7852 to normal operation following either power-down mode, the $\overline{CS}$ and $\overline{RD}$ pins must be toggled from HIGH to LOW a second time. On the second rising edge of $\overline{RD}$, the ADS7842 will exit the power-down mode and enter the sampling mode. See Figure 6.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time			3.5	µs
t_{ACQ}	Acquisition Time			1.5	µs
t_{CKP}	Clock Period	300			ns
t_{CKL}	Clock LOW	150			ns
t_{CKH}	Clock HIGH	150			ns
t_1	$\overline{CS}$ to WR Setup Time	150			ns
t_2	Address to $\overline{CS}$ Hold Time	0			ns
t_3	$\overline{CS}$ LOW	25			ns
t_4	CLK to $\overline{WR}$ Setup Time	25			ns
t_5	$\overline{CS}$ to $\overline{BUSY}$ LOW			20	ns
t_6	CLK to $\overline{WR}$ LOW	5			ns
t_7	CLK to $\overline{WR}$ HIGH	25			ns
t_8	$\overline{WR}$ to CLK LOW	25			ns
t_9	Address Hold Time	5			ns
t_{10}	Address Setup Time	5			ns
t_{11}	$\overline{BUSY}$ to $\overline{RD}$ Delay	0			ns
t_{12}	CLK LOW to $\overline{BUSY}$ HIGH	10			ns
t_{13}	BUS Access	25			ns
t_{14}	BUS Relinquish	25			ns
t_{15}	Address to $\overline{RD}$ HIGH	2			ns
t_{16}	Address Hold Time	2			ns
t_{17}	$\overline{RD}$ HIGH to CLK LOW	50			ns

TABLE I. Timing Specifications ($+V_{CC}$ = +2.7V to 3.6V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time			3.5	µs
t_{ACQ}	Acquisition Time			1.5	µs
t_{CKP}	Clock Period	300			ns
t_{CKL}	Clock LOW	150			ns
t_{CKH}	Clock HIGH	150			ns
t_1	$\overline{CS}$ to WR Setup Time	150			ns
t_2	Address to $\overline{CS}$ Hold Time	0			ns
t_3	$\overline{CS}$ LOW	25			ns
t_4	CLK to $\overline{WR}$ Setup Time	25			ns
t_5	$\overline{CS}$ to $\overline{BUSY}$ LOW			20	ns
t_6	CLK to $\overline{WR}$ LOW	5			ns
t_7	CLK to $\overline{WR}$ HIGH	25			ns
t_8	$\overline{WR}$ to CLK LOW	25			ns
t_9	Address Hold Time	5			ns
t_{10}	Address Setup Time	5			ns
t_{11}	$\overline{BUSY}$ to $\overline{RD}$ Delay	0			ns
t_{12}	CLK LOW to $\overline{BUSY}$ HIGH	10			ns
t_{13}	BUS Access	25			ns
t_{14}	BUS Relinquish	25			ns
t_{15}	Address to $\overline{RD}$ HIGH	2			ns
t_{16}	Address Hold Time	2			ns
t_{17}	$\overline{RD}$ HIGH to CLK LOW	50			ns

TABLE II. Timing Specifications ($+V_{CC}$ = +4.75V to +5.25V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	$\overline{BUSY}$	A0	A1	COMMENTS
0	↓	X	1	1	X	Sleep Mode
0	↓	X	X	0	X	Nap Mode
↓ means rising edge triggered. X = Don't care.						

TABLE III. Truth Table for Sleep and Nap Modes.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Least Significant Bit (LSB)	1.2207mV		
Full Scale	4.99878V	1111 1111 1111	FFF
Midscale	2.5V	1000 0000 0000	800
Midscale –1LSB	2.49878V	0111 1111 1111	7FF
Zero Full Scale	0V	0000 0000 0000	000

Table IV. Ideal Input Voltages and Output Codes.

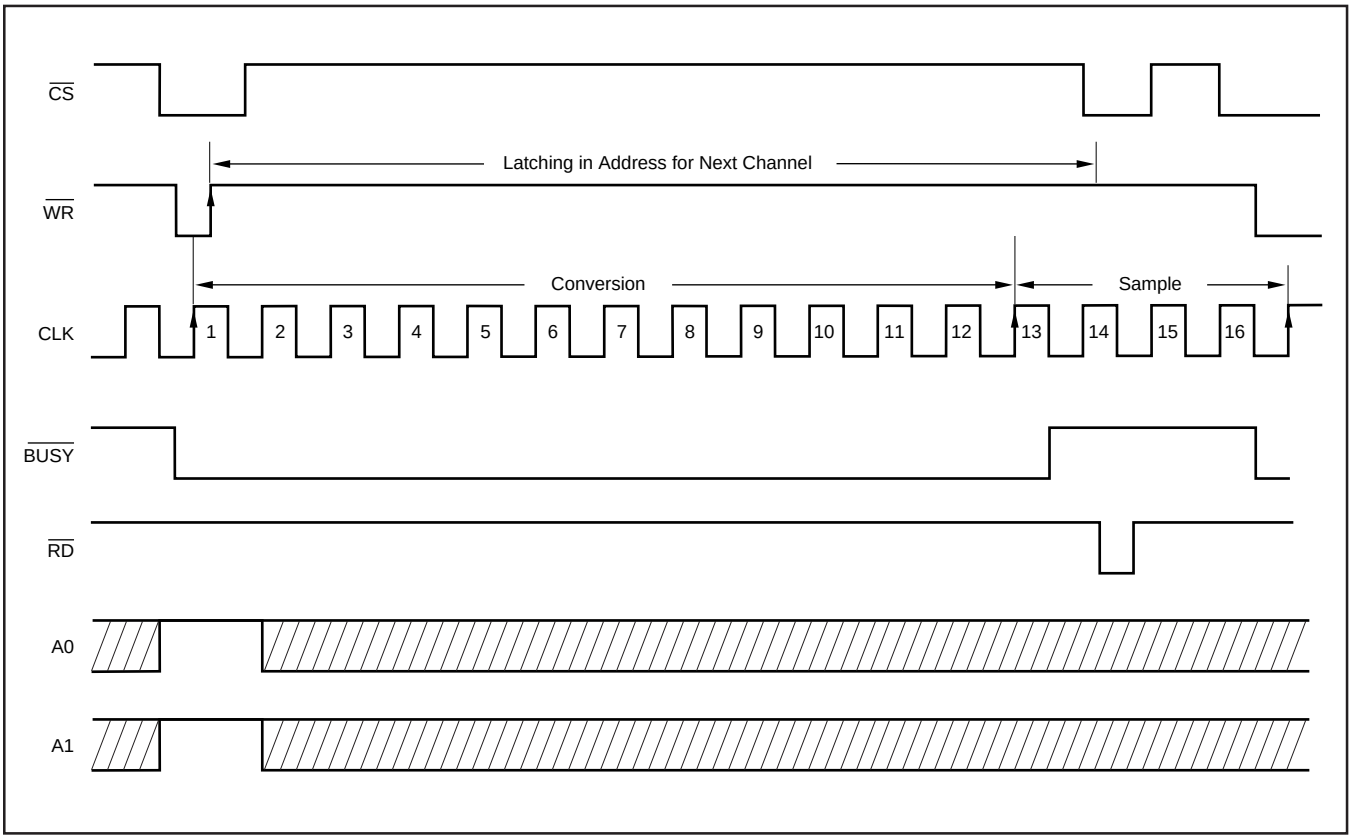
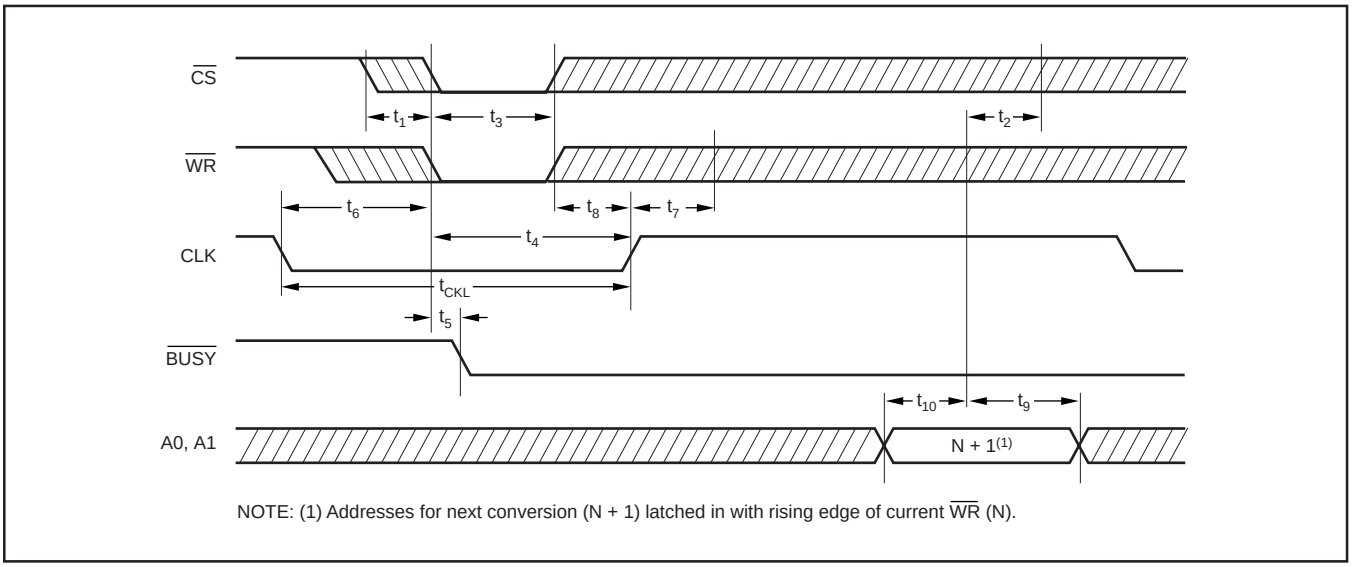


FIGURE 2. Normal Operation, 16 Clocks per Conversion.



NOTE: (1) Addresses for next conversion (N + 1) latched in with rising edge of current $\overline{WR}$ (N).

FIGURE 3. Initiating a Conversion.

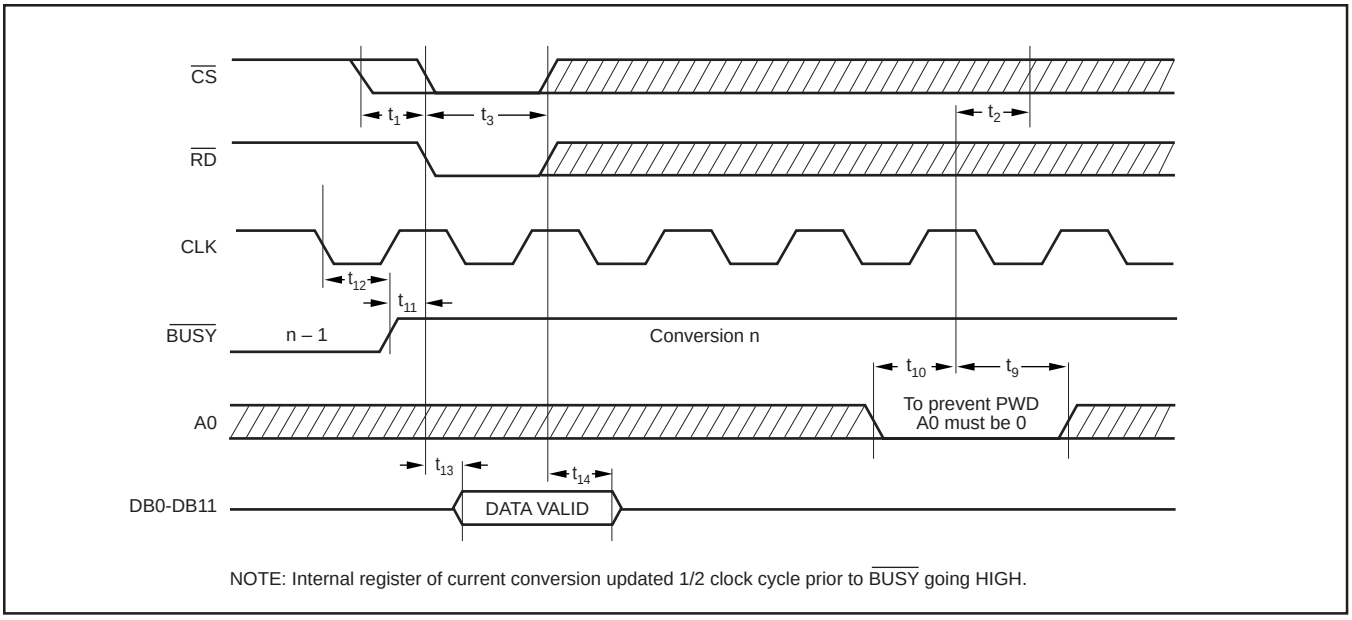


FIGURE 4. Read Timing Following a Conversion.

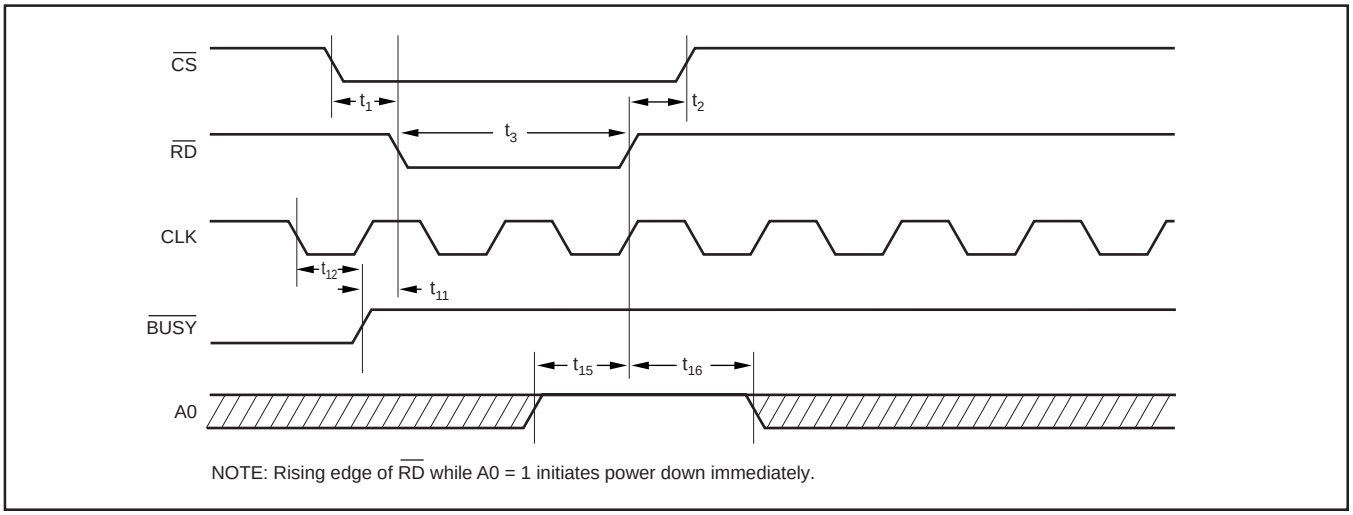


FIGURE 5. Entering Power-Down Using $\overline{RD}$ and A0.

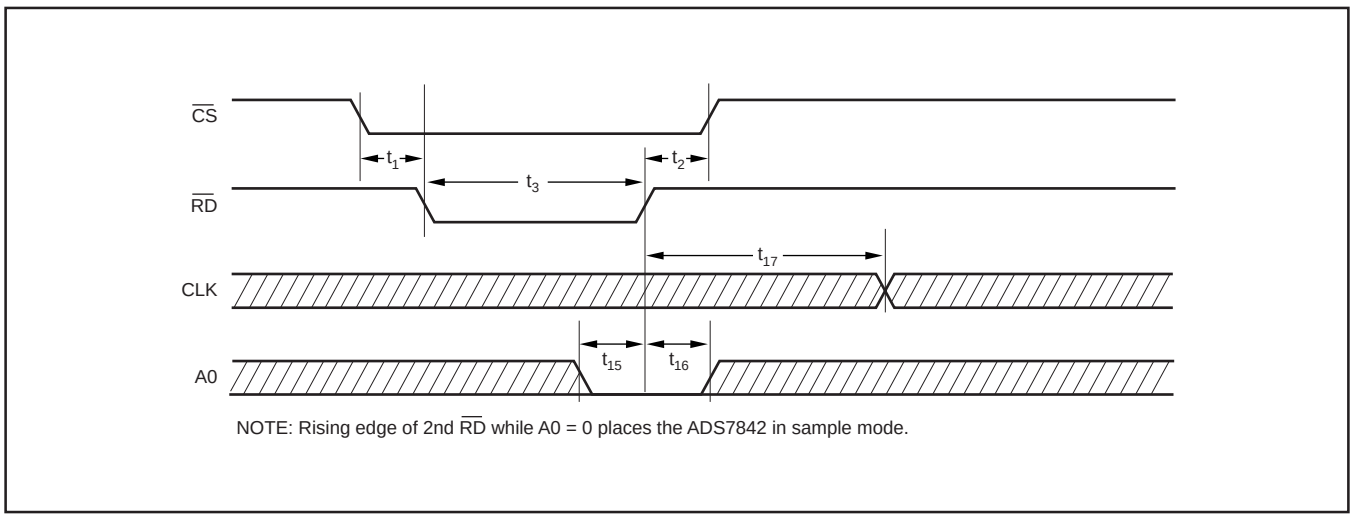


FIGURE 6. Initiating Wake-Up Using $\overline{RD}$ and A0.