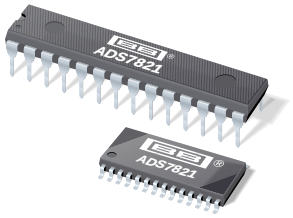
BURR - BROWN®



ADS7821

16-Bit 10μs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

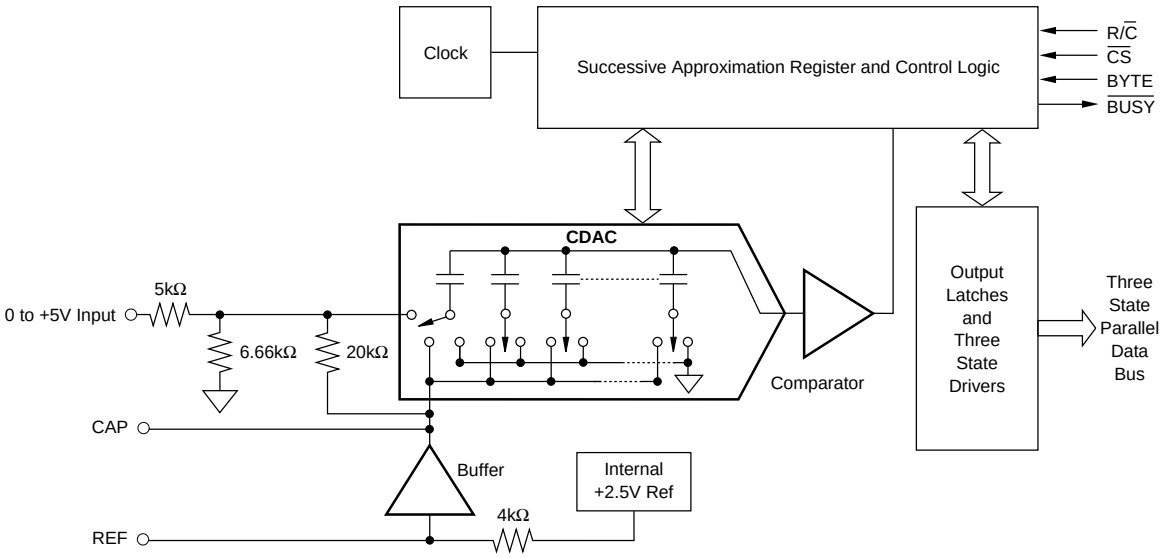
- 100kHz min SAMPLING RATE
- 0 to +5V INPUT RANGE
- 86dB min SINAD WITH 20kHz INPUT
- DNL: 16-bits "No Missing Codes"
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7820
- USES INTERNAL OR EXTERNAL REFERENCE
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 28-PIN 0.3" PLASTIC DIP AND SOIC

DESCRIPTION

The ADS7821 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7821 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a 0 to +5V input range, with power dissipation under 100mW.

The 28-pin ADS7821 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the –25°C to +85°C range.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, $V_{DIG} = V_{ANA} = V_D$ = +5V, using external reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7821P, U			ADS7821PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			✶	Bits
ANALOG INPUT								
Voltage Range			0 to +5			✶		V
Impedance			10			✶		kΩ
Capacitance			35			✶		pF
THROUGHPUT SPEED								
Conversion Cycle	Acquire and Convert			10			✶	µs
Throughput Rate		100			✶			kHz
DC ACCURACY								
Integral Linearity Error				±4			±3	LSB[1]
No Missing Codes		15			16			Bits
Transition Noise[2]			0.9			✶		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±2			✶		ppm/°C
Full Scale Error[3,4]	Internal Reference			±0.5			±0.25	%
Full Scale Error Drift	Internal Reference		±7			±5		ppm/°C
Offset Error				±8			±4	mV
Offset Error Drift			±2			✶		ppm/°C
Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$)	+4.75V < V_D < +5.25V			±12			±8	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 20kHz	90			94			dB[5]
Total Harmonic Distortion	f_{IN} = 20kHz			–90			–94	dB
Signal-to-(Noise+Distortion)	f_{IN} = 20kHz	83			86			dB
	f_{IN} = –60dB Input		28			30		dB
Signal-to-Noise	f_{IN} = 20kHz	83			86			dB
Full-Power Bandwidth[6]			250			✶		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			✶		ns
Transient Response	FS Step			2			✶	µs
Overvoltage Recovery[7]			150			✶		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	✶	✶	✶	V
Internal Reference Source Current (Must use external buffer)			1			✶		µA
Internal Reference Drift			8			✶		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	✶	✶	✶	V
External Reference Current Drain	Ext. 2.5000V Ref			100			✶	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	✶		✶	V
V_{IH}		+2.0		V_D +0.3V	✶		✶	V
I_{IL}				±10			✶	µA
I_{IH}				±10			✶	µA
DIGITAL OUTPUTS								
Data Format				Parallel 16 bits				
Data Coding				Straight Binary				
V_{OL}	I_{SINK} = 1.6mA			+0.4			✶	V
V_{OH}	I_{SOURCE} = 500µA	+4			✶			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			✶	µA
Output Capacitance	High-Z State			15			✶	pF
DIGITAL TIMING								
Bus Access Time				83			✶	ns
Bus Relinquish Time				83			✶	ns

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = V_D = +5V, using external reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7821P, U			ADS7821PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	✶	✶	✶	V
V_{ANA}		+4.75	+5	+5.25	✶	✶	✶	V
I_{DIG}			0.3			✶		mA
I_{ANA}			16			✶		mA
Power Dissipation	f_S = 100kHz			100			✶	mW
TEMPERATURE RANGE								
Specified Performance		–25		+85	✶		✶	°C
Derated Performance		–55		+125	✶		✶	°C
Storage		–65		+150	✶		✶	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			✶		°C/W
SOIC			75			✶		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, 0 to +5V input ADS721, one LSB is 76µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer as shown in Figure 6a. (4) Full scale error is the worst case of Full Scale untrimmed deviation from ideal last code transition divided by the transition voltage and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN} ..... –0.7V to V_{ANA} +0.3V
REF ..... AGND2 –0.3V to +V_{ANA} +0.3V
CAP ..... Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2 ..... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} ..... +0.3V
V_{DIG} 7V
Digital Inputs ..... –0.3V to +V_{DIG} +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7821P	Plastic DIP	246
ADS7821PB	Plastic DIP	246
ADS7821U	SOIC	217
ADS7821UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7821P	±4	83	–25°C to +85°C	Plastic DIP
ADS7821PB	±3	86	–25°C to +85°C	Plastic DIP
ADS7821U	±4	83	–25°C to +85°C	SOIC
ADS7821UB	±3	86	–25°C to +85°C	SOIC

ELECTROSTATIC DISCHARGE SENSITIVITY

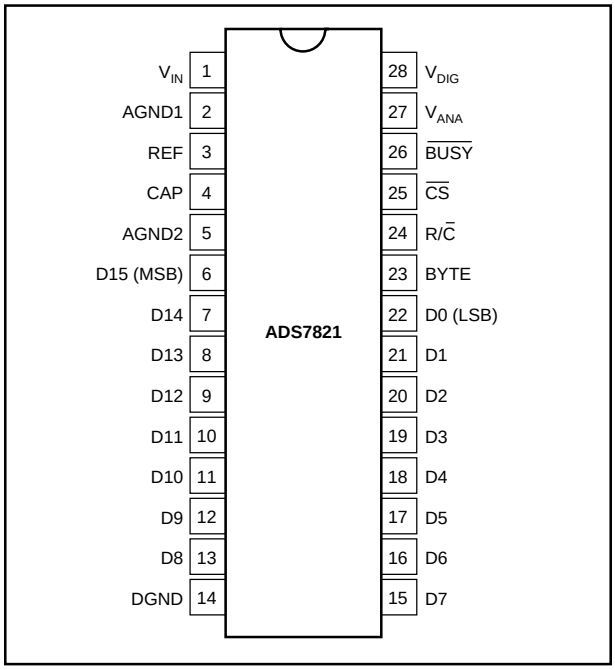
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2		Analog Ground.
6	D15 (MSB)	O	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Swaps Pins 6 through 13 with Pins 15 through 22 when HIGH. See Figures 2 and 5.
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V_{ANA}		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

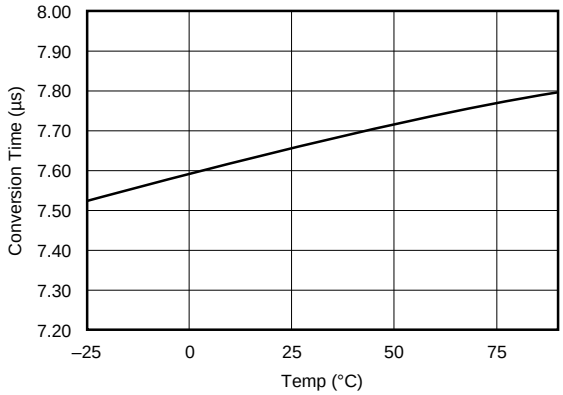
PIN CONFIGURATION



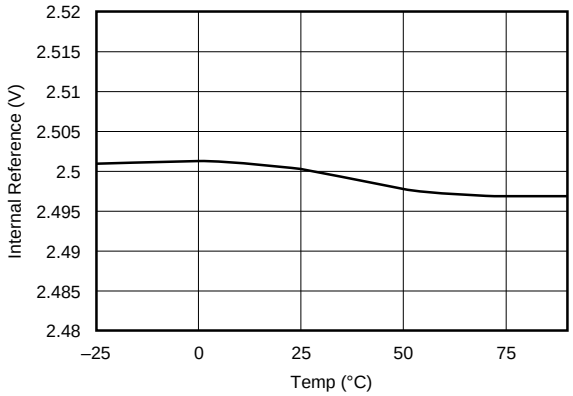
TYPICAL PERFORMANCE CURVES

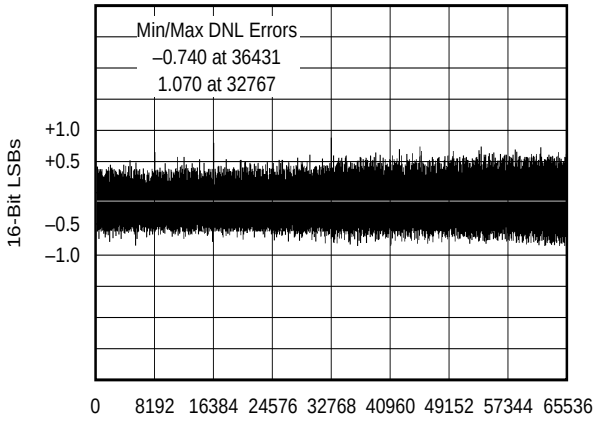
T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using external reference, unless otherwise specified.

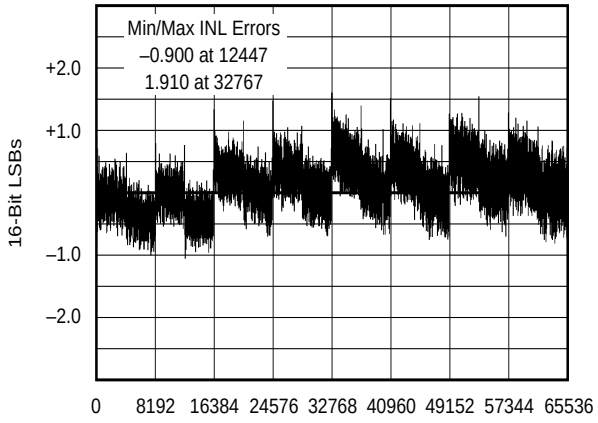
CONVERSION TIME vs TEMPERATURE



INTERNAL REFERENCE VOLTAGE vs TEMPERATURE







BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7821 with a full parallel data output. Taking R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns (5µs max) will initiate a conversion. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Straight Binary with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7821 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 25) and R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7821 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7821 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 3 through 5 for timing diagrams.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. However, the output will become active whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 3 and 4 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for "Read" and "Convert".

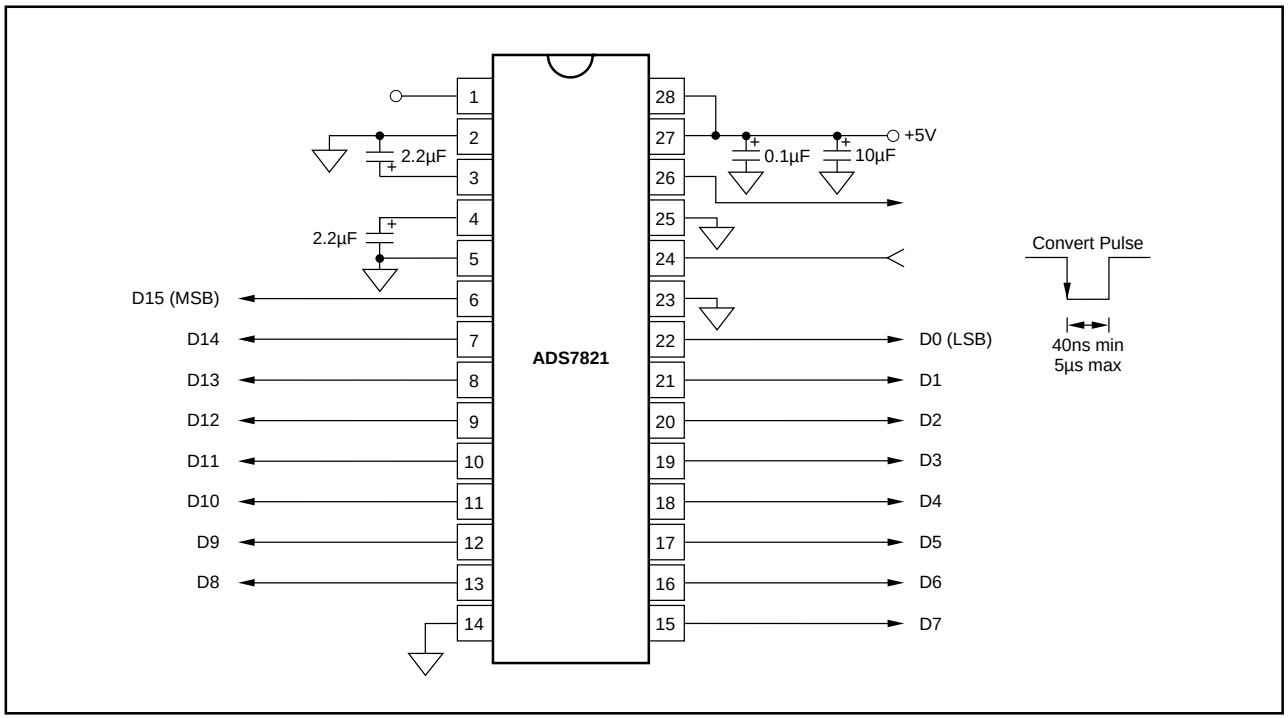


FIGURE 1. Basic Operation.

READING DATA

The ADS7821 outputs full or byte-reading parallel data in Straight Binary data output format. The parallel output will be active when R/$\overline{C}$ (pin 24) is HIGH and $\overline{CS}$ (pin 25) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 16-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full Scale Range	0 to +5V		
Least Significant Bit (LSB)	76µV		
Full Scale	4.999924V	1111 1111 1111 1111	FFFF
Midscale	2.5V	1000 0000 0000 0000	8000
One LSB below Midscale	2.499924V	0111 1111 1111 1111	7FFF
Zero Scale	0V	0000 0000 0000 0000	0000

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D15-D0 (pin 6-13 and 15-22). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table IV and Figures 3 through 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 5µs after the start of conversion 'n'. Do not attempt to read data from 5µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 through 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tying $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 3.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		5000	ns
t_2	Data Valid Delay after Start of Conversion			8	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		7.6	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after Start of Conversion		5		µs
$t_7 + t_6$	Throughput Time		9	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE IV. Conversion Timing.

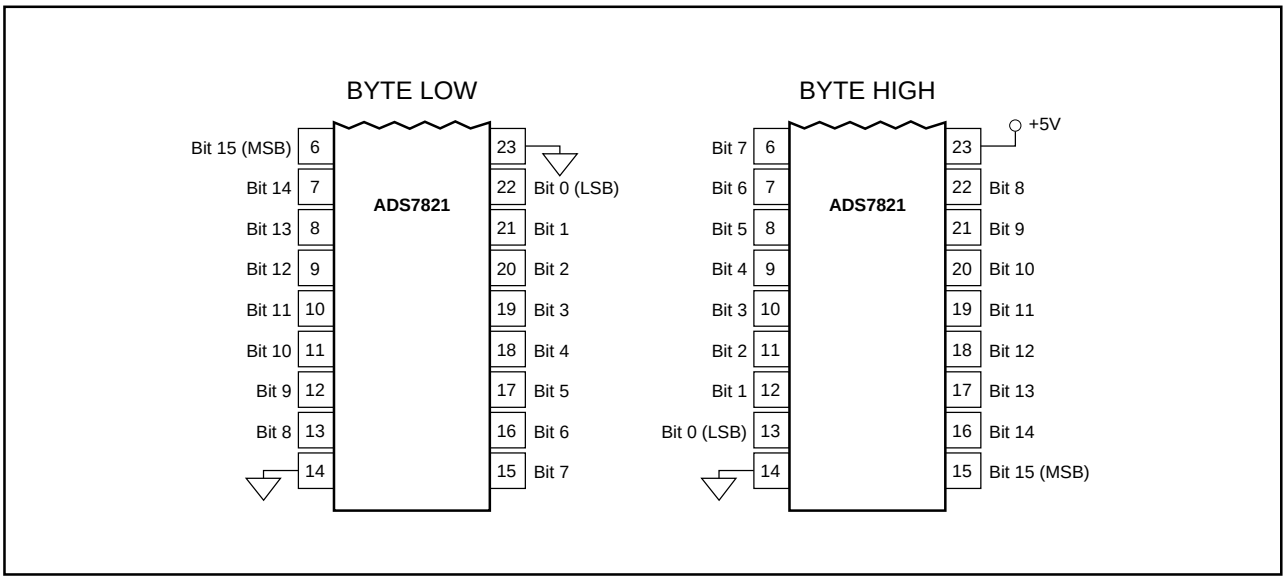


FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

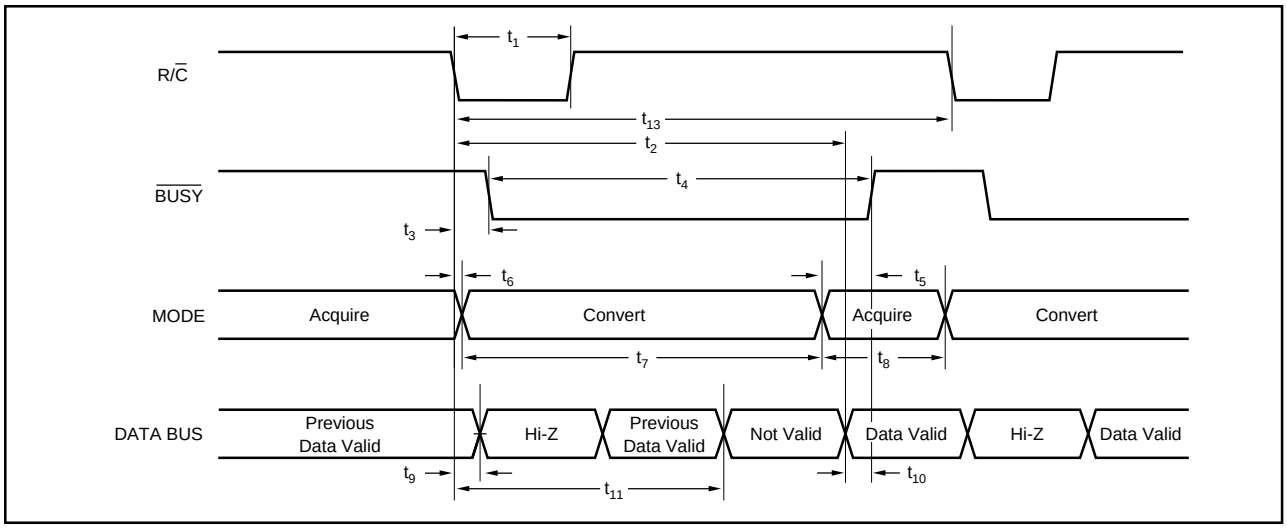


FIGURE 3. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied LOW.)

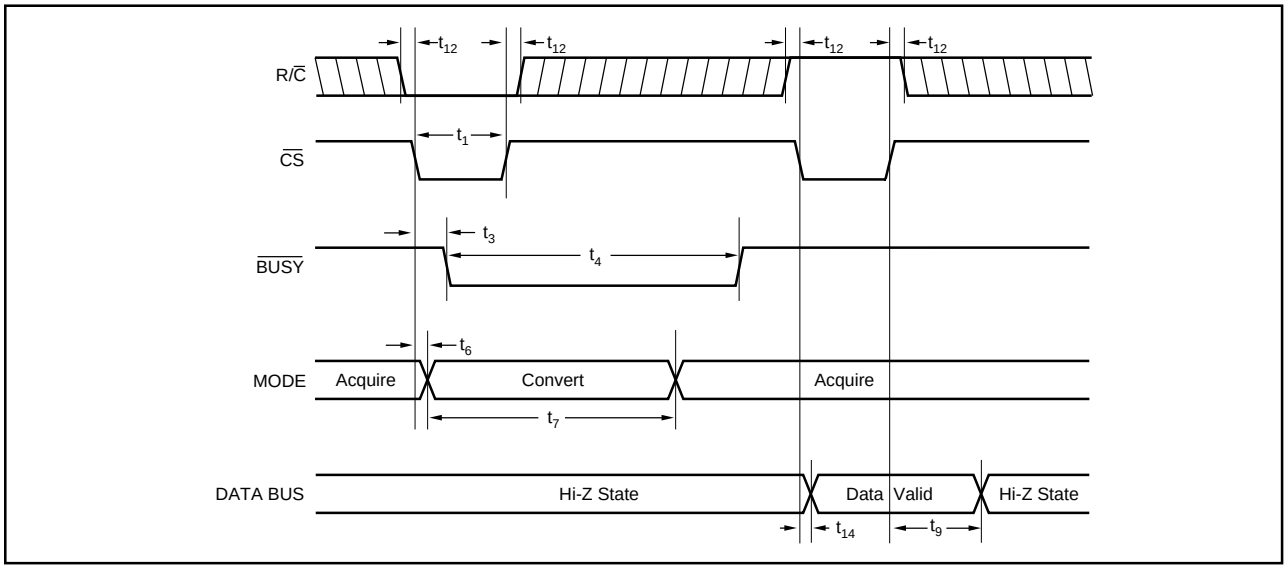


FIGURE 4. Using $\overline{CS}$ to Control Conversion and Read Timing.

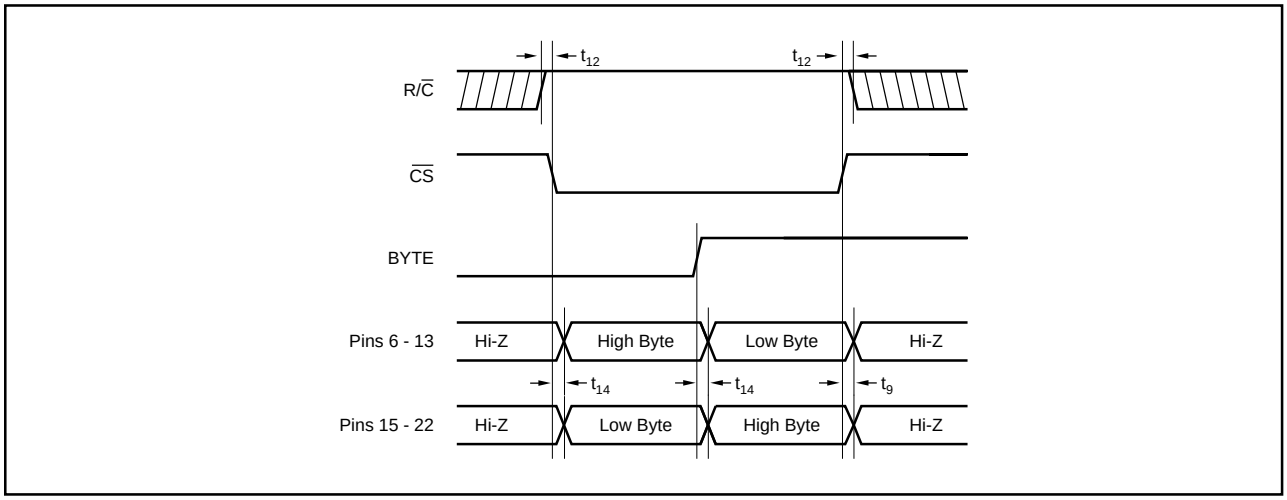


FIGURE 5. Using $\overline{CS}$ and BYTE to Control Data Bus.

INPUT RANGE

The ADS7821 offers a standard 0V to 5V input range. Figure 6 shows the required circuit connections for the ADS7821 with and without the gain adjustment hardware. Adjustments for offset and gain are described in the calibration section of this data sheet.

CALIBRATION

The ADS7821 can be trimmed in hardware or software. There is no external offset adjustment. If offset adjustment is required, an op amp featuring an offset trim pin should be used to drive the ADS7821. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

GAIN ADJUSTMENT

To calibrate the gain of the ADS7821, a 576kΩ resistor can be tied between the REF pin and a 50kΩ potentiometer as shown in Figure 6a. The calibration range is ±15mV for the gain.

REFERENCE

The ADS7821 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 3, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to directly drive external loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a static load. Static loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7821. Use of an external buffer is recommended for loads requiring more than 2mA. Do not attempt to directly drive any dynamic load with the output voltage on CAP. This will cause performance degradation of the converter.

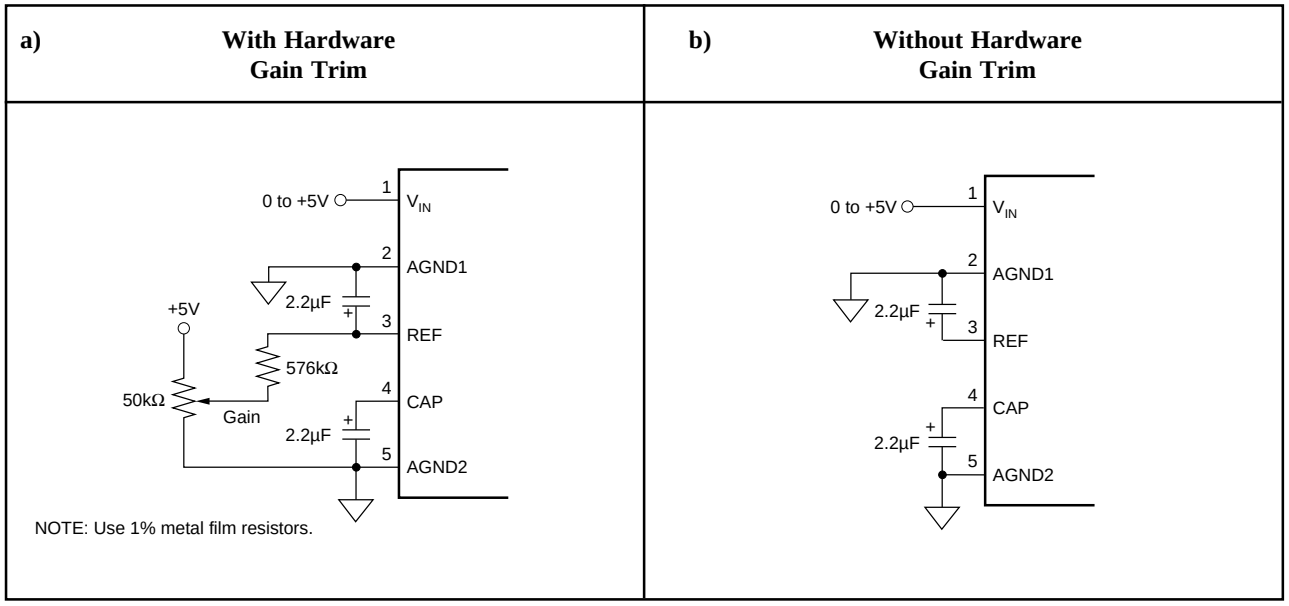


FIGURE 6. Circuit Diagram With and Without External Gain Trim.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7821 uses 98% of its power for the analog circuitry. The ADS7821 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7821. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7821, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. Any op amp sufficient for the signal in an application should be sufficient to drive the ADS7821.

INTERMEDIATE LATCHES

The ADS7821 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus. Tri-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7821 has an internal LSB size of 38μV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.