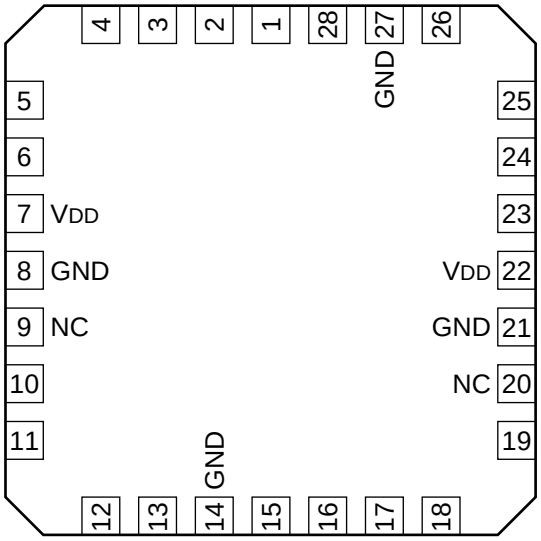
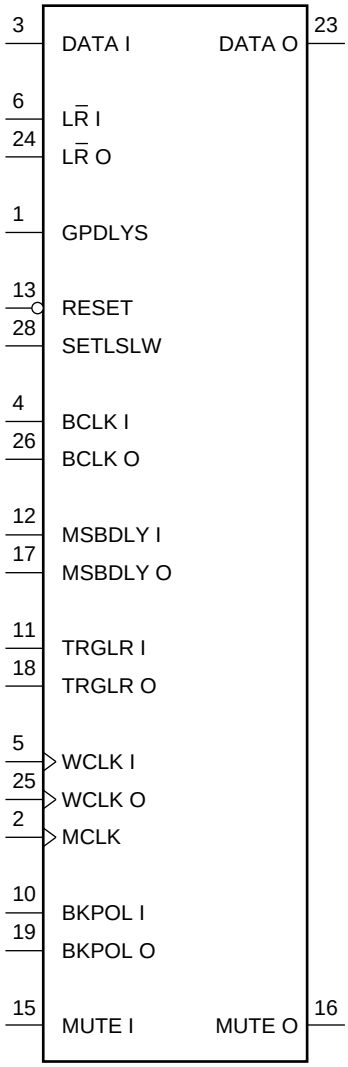
C-MOS STEREO ASYNCHRONOUS SAMPLE RATE CONVERTER

—TOP VIEW—





PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	GPDLYS	11	I	TRGLR I	21	—	GND
2	I	MCLK	12	I	MSBDLY I	22	—	VDD
3	I	DATA I	13	I	$\overline{\text{RESET}}$	23	O	DATA O
4	I	BCLK I	14	—	GND	24	I	LR̄ O
5	I	WCLK I	15	I	MUTE I	25	I	WCLK O
6	I	LR̄ I	16	O	MUTE O	26	I	BCLK O
7	—	VDD	17	I	MSBDLY O	27	—	GND
8	—	GND	18	I	TRGLR O	28	I	SETLSLW
9	—	NC	19	I	BKPOL O			
10	I	BKPOL I	20	—	NC			

INPUT

BCLK I	; BIT CLOCK INPUT FOR INPUT DATA
BCLK O	; BIT CLOCK INPUT FOR OUTPUT DATA
BKPOL I, BKPOL O	; BIT CLOCK POLARITY
DATA I	; SERIAL INPUT, MSB FIRST
GPDLYS	; GROUP DELAY-SHORT
$L\overline{R}$ I	; LEFT/$\overline{\text{RIGHT}}$ CLOCK INPUT FOR INPUT DATA
$L\overline{R}$ O	; LEFT/$\overline{\text{RIGHT}}$ CLOCK INPUT FOR OUTPUT DATA
MCLK	; MASTER CLOCK INPUT
MSBDLY I, MSBDLY O	; MSB DELAY
MUTE I	; MUTE INPUT
$\overline{\text{RESET}}$	; ACTIVE LOW RESET
SETLSLW	; SETTLE SLOW TO CHANGES IN SAMPLE RATES
TRGLR I, TRGLR O	; TRIGGER ON $L\overline{R}$
WCLK I	; WORD CLOCK INPUT FOR INPUT DATA
WCLK O	; WORD CLOCK INPUT FOR OUTPUT DATA

OUTPUT

DATA O	; SERIAL OUTPUT, MSB FIRST
MUTE O	; MUTE OUTPUT