

# DATA SHEET

**83C752/87C752**

CMOS single-chip 8-bit microcontrollers

Product specification

1996 Aug 16

IC20 Data Handbook

# CMOS single-chip 8-bit microcontrollers

## 83C752/87C752

CMOS single-chip 8-bit microcontroller with A/D, PWM

### DESCRIPTION

The Philips 83C752/87C752 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC752 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

The 8XC752 contains a  $2k \times 8$  ROM (83C752) EPROM (87C752), a  $64 \times 8$  RAM, 21 I/O lines, a 16-bit auto-reload counter/timer, a fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I<sup>2</sup>C) serial bus interface, an on-chip oscillator, a five channel multiplexed 8-bit A/D converter, and an 8-bit PWM output.

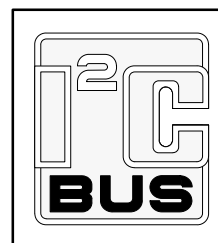
The onboard inter-integrated circuit (I<sup>2</sup>C) bus interface allows the 83C752 to operate as a master or slave device on the I<sup>2</sup>C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I<sup>2</sup>C peripherals.

The EPROM version of this device, the 87C752, is also available in both quartz-lid erasable and plastic one-time programmable (OTP) packages. Once the array has been programmed, it is functionally equivalent to the masked ROM 83C752. Thus, unless explicitly stated otherwise, all references made to the 83C752 apply equally to the 87C752.

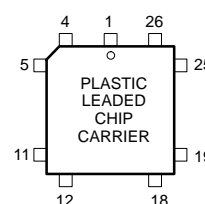
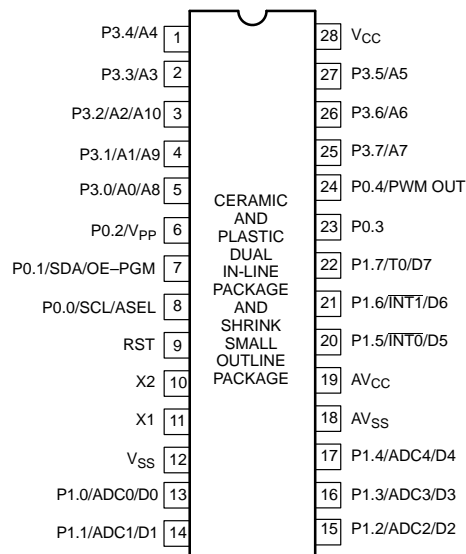
The 83C752 supports two power reduction modes of operation referred to as the idle mode and the power-down mode.

### FEATURES

- Available in erasable quartz lid or One-Time Programmable plastic packages
- 80C51 based architecture
- Inter-integrated Circuit (I<sup>2</sup>C) serial bus interface
- Small package sizes
  - 28-pin DIP
  - 28-pin PLCC
  - 28-pin SSOP
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- $2k \times 8$  ROM (83C752) EPROM (87C752)
- $64 \times 8$  RAM
- 16-bit auto reloadable counter/timer
- 5-channel 8-bit A/D converter
- 8-bit PWM output/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications



### PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	P3.4/A4	15	P1.2/ADC2/D2
2	P3.3/A3	16	P1.3/ADC3/D3
3	P3.2/A2/A10	17	P1.4/ADC4/D4
4	P3.1/A1/A9	18	AV <sub>SS</sub>
5	P3.0/A0/A8	19	AV <sub>CC</sub>
6	P0.2/V <sub>PP</sub>	20	P1.5/INT0/D5
7	P0.1/SDA/OE-PGM	21	P1.6/INT1/D6
8	P0.0/SCL/ASEL	22	P1.7/T0/D7
9	RST	23	P0.3
10	X2	24	P0.4/PWM OUT
11	X1	25	P3.7/A7
12	V <sub>SS</sub>	26	P3.6/A6
13	P1.0/ADC0/D0	27	P3.5/A5
14	P1.1/ADC1/D1	28	V <sub>CC</sub>

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## PART NUMBER SELECTION

ROM	EPROM		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
	S87C752-1F28	UV	0 to +70, 28-pin Ceramic Dual In-line Package	3.5 to 12MHz	0589B
	S87C752-2F28	UV	-40 to +85, 28-pin Ceramic Dual In-line Package	3.5 to 12MHz	0589B
	S87C752-4F28	UV	0 to +70, 28-pin Ceramic Dual In-line Package	3.5 to 16MHz	0589B
	S87C752-5F28	UV	-40 to +85, 28-pin Ceramic Dual In-line Package	3.5 to 16MHz	0589B
S83C752-1DB	S87C752-1DB	OTP	0 to +70, 28-pin Plastic Shrink Small Outline Package	3.5 to 12MHz	SOT341-1
S83C752-1N28	S87C752-1N28	OTP	0 to +70, 28-pin Plastic Dual In-line Package	3.5 to 12MHz	SOT117-2
S83C752-2N28	S87C752-2N28	OTP	-40 to +85, 28-pin Plastic Dual In-line Package	3.5 to 12MHz	SOT117-2
S83C752-4DB	S87C752-4DB	OTP	0 to +70, 28-pin Plastic Shrink Small Outline Package	3.5 to 16MHz	SOT341-1
S83C752-4N28	S87C752-4N28	OTP	0 to +70, 28-pin Plastic Dual In-line Package	3.5 to 16MHz	SOT117-2
S83C752-5N28	S87C752-5N28	OTP	-40 to +85, 28-pin Plastic Dual In-line Package	3.5 to 16MHz	SOT117-2
S83C752-1A28	S87C752-1A28	OTP	0 to +70, 28-pin Plastic Leaded Chip Carrier	3.5 to 12MHz	SOT261-3
S83C752-2A28	S87C752-2A28	OTP	-40 to +85, 28-pin Plastic Leaded Chip Carrier	3.5 to 12MHz	SOT261-3
S83C752-4A28	S87C752-4A28	OTP	0 to +70, 28-pin Plastic Leaded Chip Carrier	3.5 to 16MHz	SOT261-3
S83C752-5A28	S87C752-5A28	OTP	-40 to +85, 28-pin Plastic Leaded Chip Carrier	3.5 to 16MHz	SOT261-3
S83C752-6A28	S87C752-6A28	OTP	-55 to +125, 28-pin Plastic Leaded Chip Carrier	3.5 to 12MHz	SOT261-3
S83C752-6N28	S87C752-6N28	OTP	-55 to +125, 28-pin Plastic Dual In-line Package	3.5 to 12MHz	SOT117-2

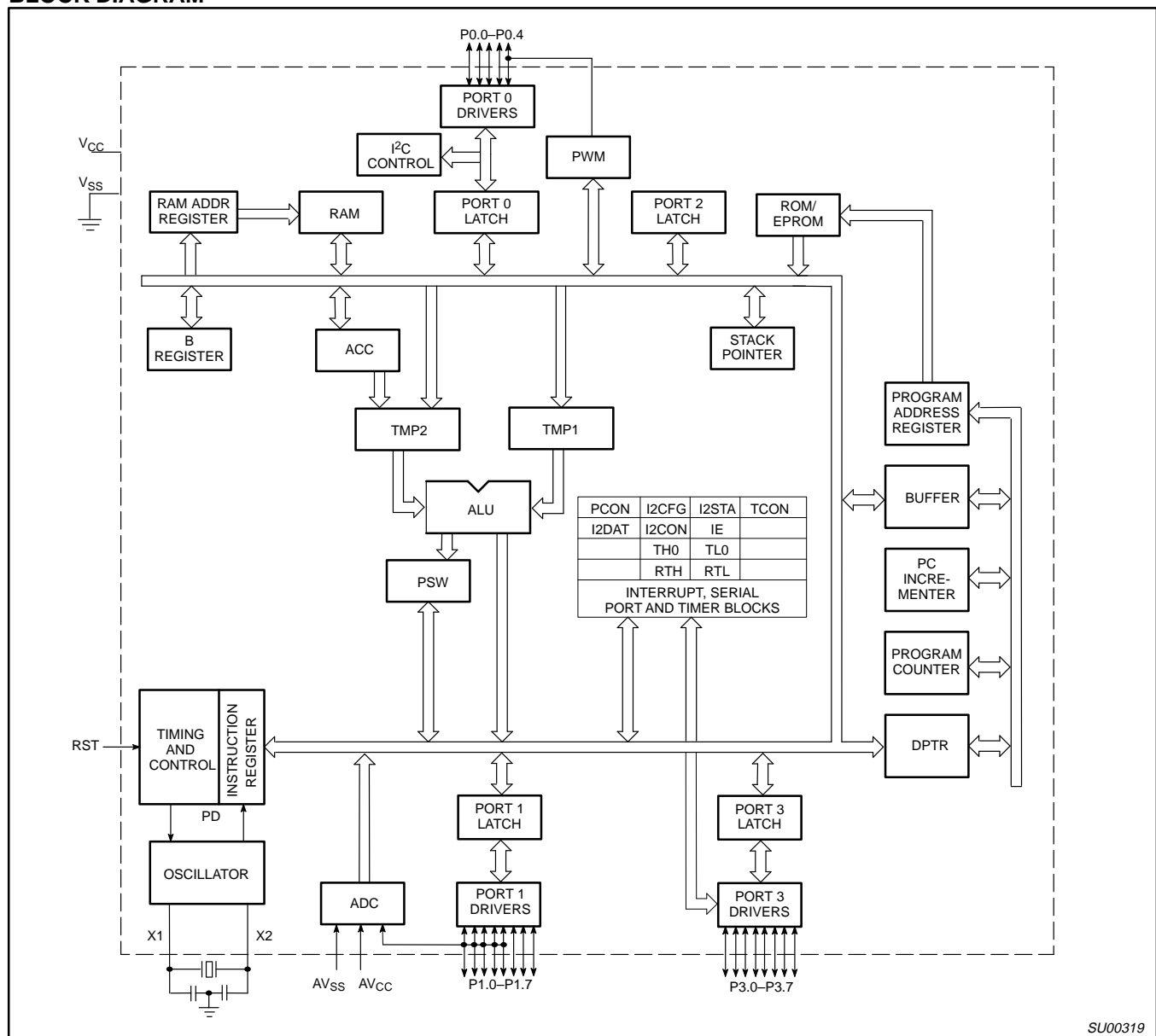
**NOTE:**

1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM.

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### BLOCK DIAGRAM



## CMOS single-chip 8-bit microcontrollers

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## PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V <sub>SS</sub>	12	I	<b>Circuit Ground Potential.</b>
V <sub>CC</sub>	28	I	<b>Supply voltage during normal, idle, and power-down operation.</b>
P0.0–P0.4	8–6 23, 24	I/O	<p><b>Port 0:</b> Port 0 is a 5-bit bidirectional port. Port 0.0–P0.2 are open drain. Port 0.0–P0.2 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. P0.3–P0.4 are bidirectional I/O port pins with internal pull-ups. Port 0 also serves as the serial I<sup>2</sup>C interface. When this feature is activated by software, SCL and SDA are driven low in accordance with the I<sup>2</sup>C protocol. These pins are driven low if the port register bit is written with a 0 or if the I<sup>2</sup>C subsystem presents a 0. The state of the pin can always be read from the port register by the program. Port 0.3 and 0.4 have internal pull-ups that function identically to port 3. Pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs.</p> <p>To comply with the I<sup>2</sup>C specification, P0.0 and P0.1 are open drain bidirectional I/O pins with the electrical characteristics listed in the tables that follow. While these differ from “standard TTL” characteristics, they are close enough for the pins to still be used as general-purpose I/O in non-I<sup>2</sup>C applications.</p>
	6	I	<b>V<sub>PP</sub> (P0.2)</b> – Programming voltage input. (See Note 2.)
	7	I	<b>OE/PGM (P0.1)</b> – Input which specifies verify mode (output enable) or the program mode. OE/PGM = 1 output enabled (verify mode). OE/PGM = 0 program mode.
	8	I	<b>ASEL (P0.0)</b> – Input which indicates which bits of the EPROM address are applied to port 3. ASEL = 0 low address byte available on port 3. ASEL = 1 high address byte available on port 3 (only the three least significant bits are used).
P1.0–P1.7	13–17, 20–22	I/O	<p><b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. P0.3–P0.4 pins are bidirectional I/O port pins with internal pull-ups. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I<sub>IL</sub>). Port 1 also serves the special function features of the SC80C51 family as listed below:</p>
	20	I	<b>INT0 (P1.5):</b> External interrupt.
	21	I	<b>INT1 (P1.6):</b> External interrupt.
	22	I	<b>T0 (P1.7):</b> Timer 0 external input.
	13–17	I	<b>ADC0 (P1.0)–ADC4 (P1.4):</b> Port 1 also functions as the inputs to the five channel multiplexed A/D converter. These pins can be used as outputs only if the A/D function has been disabled. These pins can be used as inputs while the A/D converter is enabled.
			Port 1 serves to output the addressed EPROM contents in the verify mode and accepts as inputs the value to program into the selected address during the program mode.
P3.0–P3.7	5–1, 27–25	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 3 also functions as the address input for the EPROM memory location to be programmed (or verified). The 11-bit address is multiplexed into this port as specified by P0.0/ASEL.
RST	9	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V <sub>SS</sub> permits a power-on RESET using only an external capacitor to V <sub>CC</sub> . After the device is reset, a 10-bit serial sequence, sent LSB first, applied to RESET, places the device in the programming state allowing programming address, data and V <sub>PP</sub> to be applied for programming or verification purposes. The RESET serial sequence must be synchronized with the X1 input.
X1	11	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits. X1 also serves as the clock to strobe in a serial bit stream into RESET to place the device in the programming state.
X2	10	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier.
AV <sub>CC</sub> <sup>1</sup>	19	I	<b>Analog supply voltage and reference input.</b>
AV <sub>SS</sub> <sup>1</sup>	18	I	<b>Analog supply and reference ground.</b>

## NOTE:

1. AV<sub>SS</sub> (reference ground) must be connected to 0V (ground). AV<sub>CC</sub> (reference input) cannot differ from V<sub>CC</sub> by more than ±0.2V, and must be in the range 4.5V to 5.5V.
2. When P0.2 is at or close to 0V, it may affect the internal ROM operation. We recommend that P0.2 be tied to V<sub>CC</sub> via a small pull-up (e.g., 2kΩ).

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**OSCILLATOR CHARACTERISTICS**

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

**IDLE MODE**

The 8XC752 includes the 80C51 power-down and idle mode features. In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals except the A/D and PWM stay active. The functions that continue to run while in the idle mode are Timer 0, the I<sup>2</sup>C interface including Timer 1, and the interrupts. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset. Upon powering-up the circuit, or exiting from idle mode, sufficient time must be allowed for stabilization of the internal analog reference voltages before an A/D conversion is started.

**Special Function Registers**

The special function registers (directly addressable only) contain all of the 8XC751 registers except the program counter and the four register banks. Most of the 21 special function registers are used to control the on-chip peripheral hardware. Other registers include arithmetic registers (ACC, B, PSW), stack pointer (SP) and data pointer registers (DPH, DPL). Nine of the SFRs are bit addressable.

**Data Pointer**

The data pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). In the 80C51 this register allows the access of external data memory using the MOVX instruction. Since the 83C752 does not support MOVX or external memory accesses, this register is generally used as a 16-bit offset pointer of the accumulator in a MOVC instruction. DPTR may also be manipulated as two independent 8-bit registers.

**POWER-DOWN MODE**

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

**Table 1. External Pin Status During Idle and Power-Down Modes**

MODE	Port 0*	Port 1	Port 2
Idle	Data	Data	Data
Power-down	Data	Data	Data

\* Except for PWM output (P0.4).

**DIFFERENCES BETWEEN THE 8XC752 AND THE 80C51****Program Memory**

On the 8XC752, program memory is 2048 bytes long and is not externally expandable, so the 80C51 instructions MOVX, LJMP, and LCALL are not implemented. If these instructions are executed, the appropriate number of instruction cycles will take place along with external fetches; however, no operation will take place. The LJMP may not respond to all program address bits. The only fixed locations in program memory are the addresses at which execution is taken up in response to reset and interrupts, which are as follows:

Event	Address
Reset	000
External $\overline{\text{INT0}}$	003
Counter/timer 0	00B
External $\overline{\text{INT1}}$	013
Timer 1	01B
I <sup>2</sup> C serial	023
ADC	02B
PWM	033

**Memory Organization**

The 8XC752 manipulates operands in three memory address spaces. The first is the program memory space which contains program instructions as well as constants such as look-up tables. The program memory space contains 2k bytes in the 8XC752.

The second memory space is the data memory array which has a logical address space of 128 bytes. However, only the first 64 (0 to 3FH) are implemented in the 8XC752.

The third memory space is the special function register array having a 128-byte address space (80H to FFH). Only selected locations in this memory space are used (see Table 2). Note that the architecture of these memory spaces (internal program memory, internal data memory, and special function registers) is identical to the 80C51, and the 8XC752 varies only in the amount of memory physically implemented.

The 8XC752 does not directly address any external data or program memory spaces. For this reason, the MOVX instructions in the 80C51 instruction set are not implemented in the 83C752, nor are the alternate I/O pin functions  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$ .

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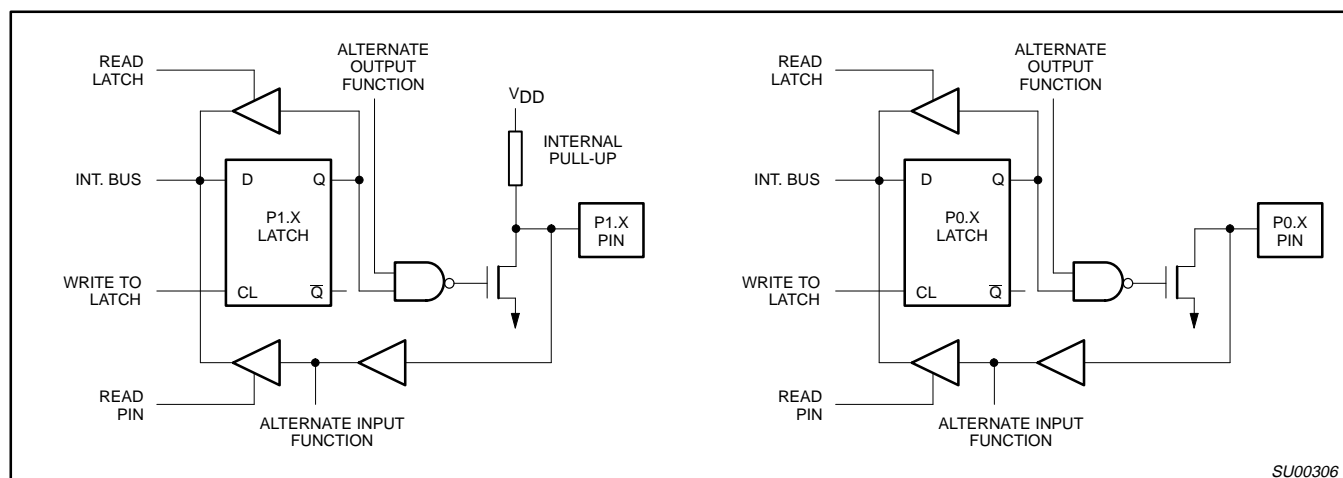


Figure 1. Port Bit Latches and I/O Buffers

**I/O Ports**

The I/O pins provided by the 83C752 consist of port 0, port 1, and port 3.

**Port 0**

Port 0 is a 5-bit bidirectional I/O port and includes alternate functions on some pins of this port. Pins P0.3 and P0.4 are provided with internal pullups while the remaining pins (P0.0, P0.1, and P0.2) have open drain output structures. The alternate functions for port 0 are:

P0.0 SCL – the I<sup>2</sup>C bus clock  
 P0.1 SDA – the I<sup>2</sup>C bus data  
 P0.4 PWM – the PWM output

If the alternate functions, I<sup>2</sup>C and PWM, are not being used, then these pins may be used as I/O ports.

**Port 1**

Port 1 is an 8-bit bidirectional I/O port whose structure is identical to the 80C51, but also includes alternate input functions on all pins. The alternate pin functions for port 1 are:

P1.0-P1.4 - ADC0-ADC4 - A/D converter analog inputs  
 P1.5 INT0 - external interrupt 0 input  
 P1.6 INT1 - external interrupt 1 input  
 P1.7 - T0 - timer 0 external input

If the alternate functions INT0, INT1, or T0 are not being used, these pins may be used as standard I/O ports. It is necessary to connect AV<sub>CC</sub> and AV<sub>SS</sub> to V<sub>CC</sub> and V<sub>SS</sub>, respectively, in order to use these pins as standard I/O pins. When the A/D converter is enabled, the analog channel connected to the A/D may not be used as a digital input; however, the remaining analog inputs may be used as digital inputs. They may not be used as digital outputs. While the A/D is enabled, the analog inputs are floating.

**Port 3**

Port 3 is an 8-bit bidirectional I/O port whose structure is identical to the 80C51. Note that the alternate functions associated with port 3 of the 80C51 have been moved to port 1 of the 83C752 (as applicable). See Figure 1 for port bit configurations.

**Counter/Timer Subsystem**

The 8XC752 has one counter/timer called timer/counter 0. Its operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits with 16 bits of autoloader. The controls for this counter are centralized in a single register called TCON.

A watchdog timer, called Timer 1, is for use with the I<sup>2</sup>C subsystem. In I<sup>2</sup>C applications, this timer is dedicated to time-generation and bus monitoring of the I<sup>2</sup>C. In non-I<sup>2</sup>C applications, it is available for use as a fixed time-base.

**Interrupt Subsystem—Fixed Priority**

The IP register and the 2-level interrupt system of the 80C51 are eliminated. The interrupt structure is a seven-source, one-level interrupt system similar to the 8XC751. Simultaneous interrupt conditions are resolved by a single-level, fixed priority as follows:

Highest priority: Pin INT0  
 Counter/timer flag 0  
 Pin INT1  
 PWM  
 Timer 1  
 Serial I<sup>2</sup>C  
 Lowest priority: ADC

The vector addresses are as follows:

Source	Vector Address
INT0	0003H
TF0	000BH
INT1	0013H
TIMER 1	001BH
SIO	0023H
ADC	002BH
PWM	0033H

**Interrupt Control Registers**

The 80C51 interrupt enable register is modified to take into account the different interrupt sources of the 8XC752.

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## Interrupt Enable Register

MSB				LSB			
EA	EAD	ETI	ES	EPWM	EX1	ET0	EX0

Position	Symbol	Function
IE.7	EA	Global interrupt disable when EA = 0
IE.6	EAD	A/D conversion complete
IE.5	ETI	Timer I
IE.4	ES	I <sup>2</sup> C serial port
IE.3	EPWM	PWM counter overflow
IE.2	EX1	External interrupt 1
IE.1	ET0	Timer 0 overflow
IE.0	EX0	External interrupt 0

## Serial Communications

The 8XC752 contains an I<sup>2</sup>C serial communications port instead of the 80C51 UART. The I<sup>2</sup>C serial port is a single bit hardware interface with all of the hardware necessary to support multimaster and slave operations. Also included are receiver digital filters and timer (timer I) for communication watch-dog purposes. The I<sup>2</sup>C serial port is controlled through four special function registers; I<sup>2</sup>C control, I<sup>2</sup>C data, I<sup>2</sup>C status, and I<sup>2</sup>C configuration.

The I<sup>2</sup>C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main technical features of the bus are:

- Bidirectional data transfer between masters and slaves
- Serial addressing of slaves
- Acknowledgment after each transferred byte
- Multimaster bus
- Arbitration between simultaneously transmitting master without corruption of serial data on bus
- With 82B715, communication distance is extended to beyond 100 feet (30M)

A large family of I<sup>2</sup>C compatible ICs is available. See the I<sup>2</sup>C section for more details on the bus and available ICs.

The 83C752 I<sup>2</sup>C subsystem includes hardware to simplify the software required to drive the I<sup>2</sup>C bus. This circuitry is the same as that on the 83C751. (See the 83C751 section for a detailed discussion of this subsystem).

## Pulse Width Modulation Output (P0.4)

The PWM outputs pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler which generates the clock for the counter. The prescaler register is PWMP. The prescaler and counter are not associated with any other timer. The 8-bit counter counts modulo 255, that is from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of a compare register, PWM. When the counter value matches the contents of this register, the output of the PWM is set high. When the counter reaches zero, the output of the PWM is set low. The pulse width ratio (duty cycle) is defined by the contents of the compare register and is in the range of 0 to 1 programmed in increments of 1/255. The PWM output can be set to be continuously high by loading the compare register with 0 and the output can be set to be continuously low by loading the compare register with 255. The PWM output is enabled by a bit in a special function register, PWENA. When enabled, the pin output is driven with a fully active pull-up. That is, when the output is high, a strong pull-up is continuously applied. When disabled, the pin functions as a normal bidirectional I/O pin, however, the counter remains active.

The PWM function is disabled during RESET and remains disabled after reset is removed until re-enabled by software. The PWM output is high during power down and idle. The counter is disabled during idle. The repetition frequency of the PWM is given by:

$$f_{\text{PWM}} = f_{\text{OSC}} / 2 (1 + \text{PWMP}) 255$$

The low/high ratio of the PWM signal is PWM / (255 – PWM) for PWM not equal to 255. For PWM = 255, the output is always low.

The repetition frequency range is 92Hz to 23.5kHz for an oscillator frequency of 12MHz.

An interrupt will be asserted upon PWM counter overflow if the interrupt is not masked off.

The PWM output is an alternative function of P0.4. In order to use this port as a bidirectional I/O port, the PWM output must be disabled by clearing the enable/disable bit in PWENA. In this case, the PWM subsystem can be used as an interval timer by enabling the PWM interrupt.



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Table 2. 8XC752 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
ACC*	Accumulator	E0H	E7 E6 E5 E4 E3 E2 E1 E0								00H
ADAT#	A/D result	84H									00H
ADCON#	A/D control	A0H	–	–	ENADC	ADCI	ADCS	AADR2	AADR1	AADR0	C0H
B*	B register	F0H	F7 F6 F5 F4 F3 F2 F1 F0								00H
DPTR:	Data pointer (2 bytes)										
DPL	Data pointer low	82H									00H
DPH	Data pointer high	83H									00H
			DF	DE	DD	DC	DB	DA	D9	D8	
I <sup>2</sup> CFG*#	I <sup>2</sup> C configuration	D8H/RD	SLAVEN	MASTRQ	0	TIRUN	–	–	CT1	CT0	0000xx00B
		WR	SLAVEN	MASTRQ	CLRTI	TIRUN	–	–	CT1	CT0	
			9F	9E	9D	9C	9B	9A	99	98	
I <sup>2</sup> CON*#	I <sup>2</sup> C control	98H/RD	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	–	81H
		WR	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP	
I <sup>2</sup> DAT*#	I <sup>2</sup> C data	99H/RD	RDAT	0	0	0	0	0	0	0	80H
		WR	XDAT	X	X	X	X	X	X	X	
			FF	FE	FD	FC	FB	FA	F9	F8	
I <sup>2</sup> STA*#	I <sup>2</sup> C status	F8H	–	IDLE	XDATA	XACTV	MAKSTR	MAKSTP	XSTR	XSTP	x0100000B
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*#	Interrupt enable	A8H	EA	EAD	ETI	ES	EPWM	EX1	ET0	EX0	00H
			–	–	–	84	83	82	81	80	xxx11111B
P0*#	Port 0	80H	–	–	–	PWM0	–	–	SDA	SCL	
			97	96	95	94	93	92	91	90	FFH
P1*#	Port 1	90H	T0	INT1	INT0	ADC4	ADC3	ADC2	ADC1	ADC0	
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
PCON#	Power control	87H	–	–	–	–	–	–	PD	IDL	xxxx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
PWCM#	PWM compare	8EH									xxxxxxxxxB
PWENA#	PWM enable	FEH	–	–	–	–	–	–	–	PWE	FEH
PWMP#	PWM prescaler	8FH									00H
RTL#	Timer low reload	8BH									00H
RTH#	Timer high reload	8DH									00H
SP	Stack pointer	81H									07H
TL#	Timer low	8AH									00H
TH#	Timer high	8CH									00H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*#	Timer control	88H	GATE	C/T	TF	TR	IE0	IT0	IE1	IT1	00H

\* SFRs are bit addressable.

# SFRs are modified from or added to the 80C51 SFRs.

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**Special Function Register Addresses**

Special function registers for the 8XC752 are identical to those of the 80C51, except for the changes listed below:

80C51 special function registers not present in the 8XC752 are TMOD (89), P2 (A0) and IP (B8). The 80C51 registers TH1, TL1, SCON, and SBUF are replaced with the 8XC752 registers RTH, RTL, I2CON, and I2DAT, respectively. Additional special function registers are I2CFG (D8) and I2STA (FB). ADCON (A0), ADAT (84), PWM (8E), PWMP (8F), and PWENA (FE). See Table 3.

**A/D Converter**

The analog input circuitry consists of a 5-input analog multiplexer and an A to D converter with 8-bit resolution. The conversion takes 40 machine cycles, i.e., 40µs at 12MHz oscillator frequency. The A/D converter is controlled using the ADCON control register. Input channels are selected by the analog multiplexer through ADCON register bits 0–2.

The 83C752 contains a five-channel multiplexed 8-bit A/D converter. The conversion requires 40 machine cycles (40µs at 12MHz oscillator frequency).

The A/D converter is controlled by the A/D control register, ADCON. Input channels are selected by the analog multiplexer by bits ADCON.0 through ADCON.2. The ADCON register is not bit addressable.

**ADCON Register**

MSB								LSB
X	X	ENADC	ADCI	ADCS	AADR2	AADR1	AADR0	

ADCI	ADCS	Operation
0	0	ADC not busy, a conversion can be started.
0	1	ADC busy, start of a new conversion is blocked.
1	0	Conversion completed, start of a new conversion is blocked.
1	1	Not possible.

INPUT CHANNEL SELECTION			
ADDR2	ADDR1	ADDR0	INPUT PIN
0	0	0	P1.0
0	0	1	P1.1
0	1	0	P1.2
0	1	1	P1.3
1	0	0	P1.4

Position	Symbol	Function
ADCON.5	ENADC	Enable A/D function when ENADC = 1. Reset forces ENADC = 0.
ADCON.4	ADCI	ADC interrupt flag. This flag is set when an ADC conversion is complete. If IE.6 = 1, an interrupt is requested when ADCI = 1. The ADCI flag is cleared when conversion data is read. This flag is read only.
ADCON.3	ADCS	ADC start. Setting this bit starts an A/D conversion. Once set, ADCS remains high throughout the conversion cycle. On completion of the conversion, it is reset just before the ADCI interrupt flag is cleared. ADCS cannot be reset by software. ADCS should not be used to monitor the A/D converter status. ADCI should be used for this purpose.
ADCON.2	AADR2	Analog input select.
ADCON.1	AADR1	Analog input select.
ADCON.0	AADR0	Analog input select. This binary coded address selects one of the five analog input port pins of P1 to be input to the converter. It can only be changed when ADCI and ADCS are both low. AADR2 is the most significant bit.

The completion of the 8-bit ADC conversion is flagged by ADCI in the ADCON register, and the result is stored in the special function register ADAT.

An ADC conversion in progress is unaffected by an ADC start. The result of a completed conversion remains unaffected provided ADCI remains at a logic 1. While ADCS is a logic 1 or ADCI is a logic 1, a new ADC START will be blocked and consequently lost. An ADC conversion in progress is aborted when the idle or power-down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the idle mode. See Figure 2 for an A/D input equivalent circuit.

The analog input pins ADC0-ADC4 may be used as digital inputs and outputs when the A/D converter is disabled by a 0 in the ENADC bit in ADCON. When the A/D is enabled, the analog input channel that is selected by the ADDR2-ADDR0 bits in ADCON cannot be used as a digital input. Reading the selected A/D channel as a digital input will always return a 1. The unselected A/D inputs may always be used as digital inputs. Unselected analog inputs will be floating and may not be used as digital outputs.

The A/D reference inputs on the 8XC752 are tied together with the analog supply pins AV<sub>CC</sub> and AV<sub>SS</sub>. This means that the reference voltage on the A/D cannot be varied separately from the analog supply pins. AV<sub>SS</sub> must be connected to 0V and AV<sub>CC</sub> must be connected to a supply voltage between 4.5V and 5.5V. A/D measurements may be made in the range of 4.5V to 5.5V. Increasing the voltage on the A/D ground reference above 0V or reducing the voltage on the positive A/D reference below 4.5V is not permitted.

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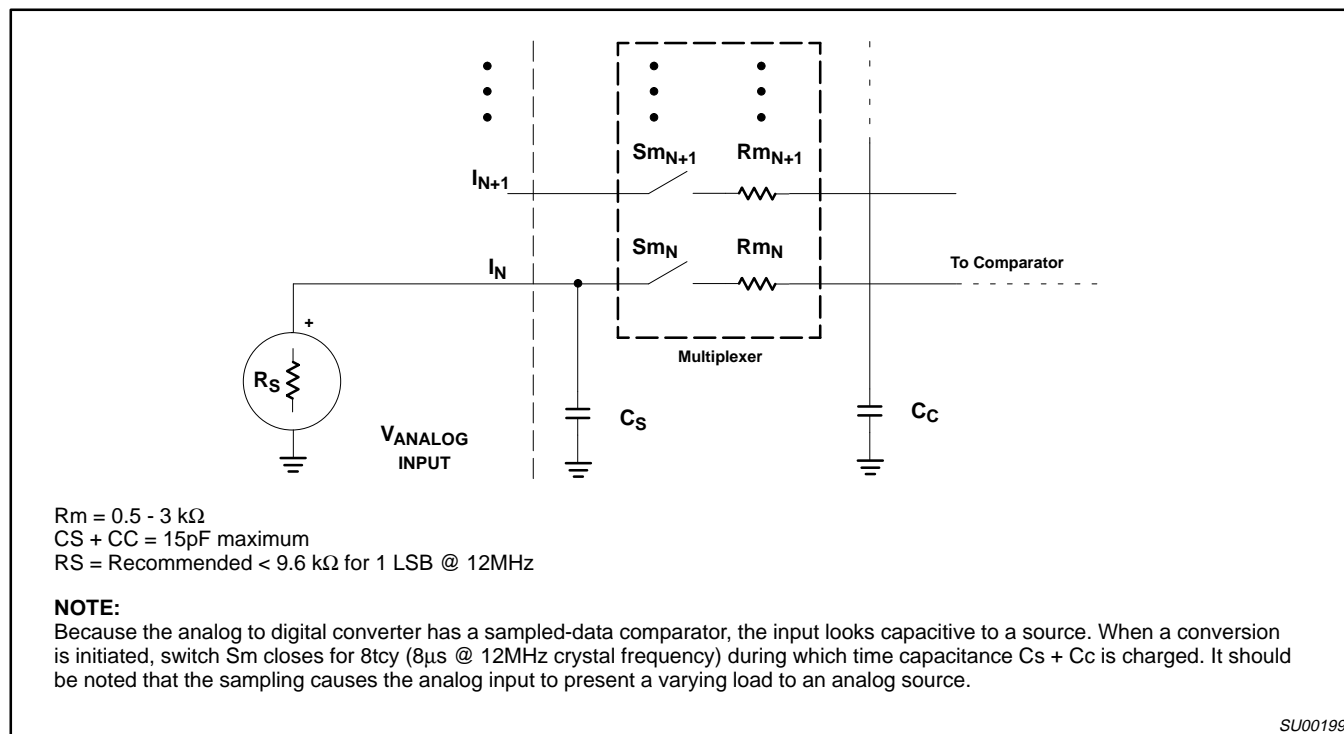


Figure 2. A/D Input: Equivalent Circuit

**A/D CONVERTER PARAMETER DEFINITIONS**

The following definitions are included to clarify some specifications given and do not represent a complete set of A/D parameter definitions.

**Absolute Accuracy Error**

Absolute accuracy error of a given output is the difference between the theoretical analog input voltage to produce a given output and the actual analog input voltage required to produce the same code. Since the same output code is produced by a band of input voltages, the "required input voltage" is defined as the midpoint of the band of input voltage that will produce that code. Absolute accuracy error not specified with a code is the maximum over all codes.

**Nonlinearity**

If a straight line is drawn between the end points of the actual converter characteristics such that zero offset and full scale errors are removed, then non-linearity is the maximum deviation of the code transitions of the actual characteristics from that of the straight line so constructed. This is also referred to as relative accuracy and also integral non-linearity.

**Differential Non-Linearity**

Differential non-linearity is the maximum difference between the actual and ideal code widths of the converter. The code widths are the differences expressed in LSB between the code transition points, as the input voltage is varied through the range for the complete set of codes.

**Gain Error**

Gain error is the deviation between the ideal and actual analog input voltage required to cause the final code transition to a full-scale output code after the offset error has been removed. This may sometimes be referred to as full scale error.

**Offset Error**

Offset error is the difference between the actual input voltage that causes the first code transition and the ideal value to cause the first code transition. This ideal value is 1/2 LSB above  $V_{ref-}$ .

**Channel to Channel Matching**

Channel to channel matching is the maximum difference between the corresponding code transitions of the actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

**Crosstalk**

Crosstalk is the measured level of a signal at the output of the converter resulting from a signal applied to one deselected channel.

**Total Error**

Maximum deviation of any step point from a line connecting the ideal first transition point to the ideal last transition point.

**Relative Accuracy**

Relative accuracy error is the deviation of the ADC's actual code transition points from the ideal code transition points on a straight line which connects the ideal first code transition point and the final code transition point, after nullifying offset error and gain error. It is generally expressed in LSBs or in percent of FSR.

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COUNTER/TIMER

The 8XC752 counter/timer is designated Timer 0 and is separate from Timer 1 of the I<sup>2</sup>C serial port and from the PWM. Its operation is similar to mode 2 of the 80C51 counter/timer, extended to 16 bits. When Timer 0 is used in the external counter mode, the T0 input (P1.7) is sampled every S4P1. The counter/timer function is controlled using the timer control register (TCON).

TCON Register

MSB				LSB			
GATE	C/T	TF	TR	IE0	IT0	IE1	IT1

Position	Symbol	Function
TCON.7	GATE	1 – Timer 0 is enabled only when INT0 pin is high and TR is 1. 0 – Timer 0 is enabled only when TR is 1.
TCON.6	C/T	1 – Counter operation from T0 pin. 0 – Timer operation from internal clock.
TCON.5	TF	1 – Set on overflow of T0. 0 – Cleared when processor vectors to interrupt routine and by reset.
TCON.4	TR	1 – Enable timer 0 0 – Disable timer 0
TCON.3	IE0	1 – Edge detected on INT0
TCON.2	IT0	1 – INT0 is edge triggered. 0 – INT0 is level sensitive.
TCON.1	IE1	1 – Edge detected on INT1
TCON.0	IT1	1 – INT1 is edge triggered. 0 – INT1 is level sensitive.

These flags are functionally identical to the corresponding 80C51 flags except that there is only one of the 80C51 style timers, and the flags are combined into one register.

Note that the positions of the IE0/IT0 and IE1/IT1 bits are transposed from the positions used in the standard 80C51 TCON register.

A communications watchdog timer, Timer 1, is described in the I<sup>2</sup>C section. In I<sup>2</sup>C applications, this timer is dedicated to time generation and bus monitoring for the I<sup>2</sup>C. In non-I<sup>2</sup>C applications, it is available for use as a fixed time base.

The 16-bit timer/counter's operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits. The timer/counter is clocked by either 1/12 the oscillator frequency or by transitions on the T0 pin. The C/T pin in special function register TCON selects between these two modes. When the TCON TR bit is set, the timer/counter is enabled. Register pair TH and TL are incremented by the clock source. When the register pair overflows, the register pair is reloaded with the values in registers RTH and RTL. The value in the reload registers is left unchanged. The TF bit in special function register TCON is set on counter overflow and, if the interrupt is enabled, will generate an interrupt (see Figure 3).

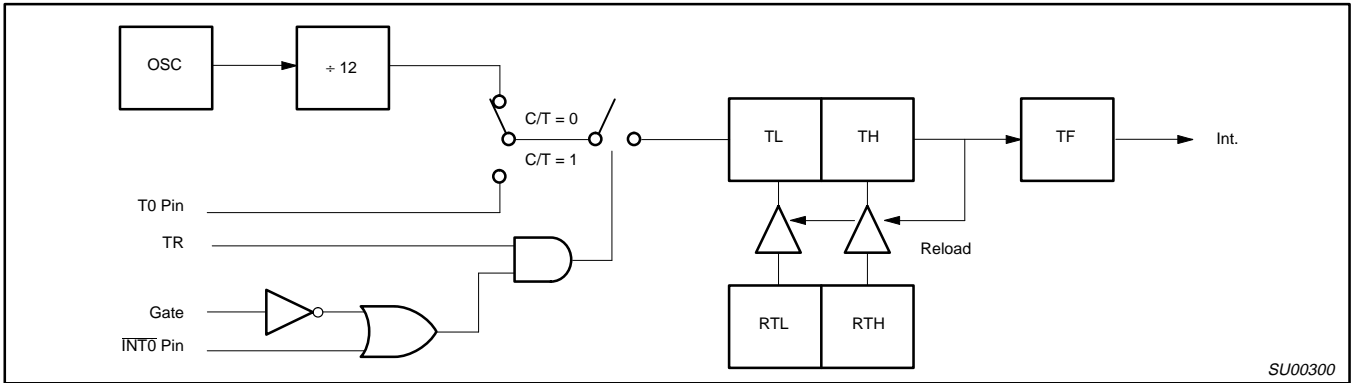


Figure 3. 83C752 Counter/Timer Block Diagram

Table 3. I<sup>2</sup>C Special Function Register Addresses

REGISTER ADDRESS			BIT ADDRESS							
NAME	SYMBOL	ADDRESS	MSB				LSB			
I <sup>2</sup> C control	I2CON	98	9F	9E	9D	9C	9B	9A	99	98
I <sup>2</sup> C data	I2DAT	99	–	–	–	–	–	–	–	–
I <sup>2</sup> C configuration	I2CFG	D8	DF	DE	DD	DC	DB	DA	D9	D8
I <sup>2</sup> C status	I2STA	F8	FF	FE	FD	FC	FB	FA	F9	F8

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**ABSOLUTE MAXIMUM RATINGS**<sup>1, 3, 4</sup>

PARAMETER	RATING	UNIT
Storage temperature range	−65 to +150	°C
Voltage from $V_{CC}$ to $V_{SS}$	−0.5 to +6.5	V
Voltage from any pin to $V_{SS}$ (except $V_{PP}$ )	−0.5 to $V_{CC} + 0.5$	V
Power dissipation	1.0	W
Voltage from $V_{PP}$ pin to $V_{SS}$	−0.5 to + 13.0	V

**DC ELECTRICAL CHARACTERISTICS**

$T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $AV_{CC} = 5\text{V} \pm 5\%$ ,  $AV_{SS} = 0\text{V}$

$V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS <sup>4</sup>			UNIT
			MIN	Typical <sup>1</sup>	MAX	
$I_{CC}$	Supply current (see Figure 6)					
<b>Inputs</b>						
$V_{IL}$	Input low voltage, except SDA, SCL	(0 to $70^{\circ}\text{C}$ ) (−40 to $+85^{\circ}\text{C}$ )	−0.5 −0.5		$0.2V_{CC}-0.1$ $0.2V_{CC}-0.15$	V V
$V_{IH}$	Input high voltage, except X1, RST	(0 to $70^{\circ}\text{C}$ ) (−40 to $+85^{\circ}\text{C}$ )	$0.2V_{CC}+0.9$ ( $0.2V_{CC}+1$ )		$V_{CC}+0.5$ $V_{CC}+0.5$	V V
$V_{IH1}$	Input high voltage, X1, RST	(0 to $70^{\circ}\text{C}$ ) (−40 to $+85^{\circ}\text{C}$ )	$0.7V_{CC}$ $0.7V_{CC}$ to 0.1		$V_{CC}+0.5$ $V_{CC}+0.5$	V V
$V_{IL1}$	SDA, SCL, P0.2 Input low voltage	(0 to $70^{\circ}\text{C}$ ) (−40 to $+85^{\circ}\text{C}$ )	−0.5 −0.5		$0.3V_{CC}$ $0.3V_{CC}-0.1$	V V
$V_{IH2}$	Input high voltage	(0 to $70^{\circ}\text{C}$ ) (−40 to $+85^{\circ}\text{C}$ )	$0.7V_{CC}$ $0.7V_{CC}+0.1$		$V_{CC}+0.5$ $V_{CC}+0.5$	V V
<b>Outputs</b>						
$V_{OL}$	Output low voltage, ports 1, 3, 0.3, and 0.4 (PWM disabled)	$I_{OL} = 1.6\text{mA}^2$			0.45	V
$V_{OL1}$	Output low voltage, port 0.2	$I_{OL} = 3.2\text{mA}^2$			0.45	V
$V_{OH}$	Output high voltage, ports 1, 3, 0.3, and 0.4 (PWM disabled)	$I_{OH} = -60\mu\text{A}$ $I_{OH} = -25\mu\text{A}$ $I_{OH} = -10\mu\text{A}$ $I_{OH} = -400\mu\text{A}$	2.4 $0.75V_{CC}$ $0.9V_{CC}$ 2.4			V V V V
$V_{OH2}$	Output high voltage, P0.4 (PWM enabled)	$I_{OH} = -40\mu\text{A}$	$0.9V_{CC}$			V
$V_{OL2}$	Port 0.0 and 0.1 ( $I^2\text{C}$ ) – Drivers Output low voltage	$I_{OL} = 3\text{mA}$ (over $V_{CC}$ range)			0.4	V
C	Driver, receiver combined: Capacitance				10	pF
$I_{IL}$	Logical 0 input current, ports 1, 3, 0.3, and 0.4 (PWM disabled) <sup>11</sup>	$V_{IN} = 0.45\text{V}$ (0 to $70^{\circ}\text{C}$ ) $V_{IN} = 0.45\text{V}$ (0 to $+85^{\circ}\text{C}$ )			−50 −75	$\mu\text{A}$ $\mu\text{A}$
$I_{TL}$	Logical 1 to 0 transition current, ports 1, 3, 0.3 and 0.4 <sup>11</sup>	$V_{IN} = 2\text{V}$ (0 to $70^{\circ}\text{C}$ ) $V_{IN} = 2\text{V}$ (−40 to $+85^{\circ}\text{C}$ )			−650 −750	$\mu\text{A}$ $\mu\text{A}$
$I_{LI}$	Input leakage current, port 0.0, 0.1 and 0.2	$0.45 < V_{IN} < V_{CC}$			$\pm 10$	$\mu\text{A}$
$R_{RST}$	Reset pull-down resistor		25		175	k $\Omega$
$C_{IO}$	Pin capacitance	Test freq = 1MHz, $T_{amb} = 25^{\circ}\text{C}$			10	pF
$I_{PD}$	Power-down current <sup>5</sup>	$V_{CC} = 2$ to $5.5\text{V}$ $V_{CC} = 2$ to $6.0\text{V}$ (83C752)			50	$\mu\text{A}$
$V_{PP}$	$V_{PP}$ program voltage (87C752 only)	$V_{SS} = 0\text{V}$ $V_{CC} = 5\text{V} \pm 10\%$ $T_{amb} = 21^{\circ}\text{C}$ to $27^{\circ}\text{C}$	12.5		13.0	V
$I_{PP}$	Program current (87C752 only)	$V_{PP} = 13.0\text{V}$			50	mA

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**DC ELECTRICAL CHARACTERISTICS** (Continued)

$T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $AV_{CC} = 5V \pm 5$ ,  $AV_{SS} = 0V^4$

$V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS <sup>4</sup>			UNIT
			MIN	Typical <sup>1</sup>	MAX	
Analog Inputs (A/D guaranteed only with quartz window covered.)						
AV <sub>CC</sub>	Analog supply voltage <sup>10</sup>	AV <sub>CC</sub> = V <sub>CC</sub> ±0.2V	4.5		5.5	V
AI <sub>CC</sub>	Analog operating supply current	AV <sub>CC</sub> = 5.12V			3 <sup>9</sup>	mA
AV <sub>IN</sub>	Analog input voltage <sup>12</sup>		AV <sub>SS</sub> –0.2		AV <sub>CC</sub> +0.2	V
C <sub>IA</sub>	Analog input capacitance				15	pF
t <sub>ADS</sub>	Sampling time				8t <sub>CY</sub>	s
t <sub>ADC</sub>	Conversion time				40t <sub>CY</sub>	s
R	Resolution				8	bits
E <sub>RA</sub>	Relative accuracy				±1	LSB
OS <sub>e</sub>	Zero scale offset				±1	LSB
G <sub>e</sub>	Full scale gain error				0.4	%
M <sub>CTC</sub>	Channel to channel matching				±1	LSB
C <sub>t</sub>	Crosstalk	0–100kHz			–60	dB

**NOTES:**

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
 Maximum  $I_{OL}$  per port pin: 10mA (NOTE: This is 85°C spec.)  
 Maximum  $I_{OL}$  per 8-bit port: 26mA  
 Maximum total  $I_{OL}$  for all outputs: 67mA  
 If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.
- Power-down  $I_{CC}$  is measured with all output pins disconnected; port 0 =  $V_{CC}$ ; X2, X1 n.c.; RST =  $V_{SS}$ .
- $I_{CC}$  is measured with all output pins disconnected; X1 driven with  $t_{CLCH}$ ,  $t_{CHCL} = 5ns$ ,  $V_{IL} = V_{SS} + 0.5V$ ,  $V_{IH} = V_{CC} - 0.5V$ ; X2 n.c.; RST = port 0 =  $V_{CC}$ .  $I_{CC}$  will be slightly higher if a crystal oscillator is used.
- Idle  $I_{CC}$  is measured with all output pins disconnected; X1 driven with  $t_{CLCH}$ ,  $t_{CHCL} = 5ns$ ,  $V_{IL} = V_{SS} + 0.5V$ ,  $V_{IH} = V_{CC} - 0.5V$ ; X2 n.c.; port 0 =  $V_{CC}$ ; RST =  $V_{SS}$ .
- Load capacitance for ports = 80pF.
- The resistor ladder network is not disconnected in the power down or idle modes. Thus, to conserve power, the user may remove  $AV_{CC}$ .
- If the A/D function is not required, or if the A/D function is only needed periodically,  $AV_{CC}$  may be removed without affecting the operation of the digital circuitry. Contents of ADCON and ADAT are not guaranteed to be valid. If  $AV_{CC}$  is removed, the A/D inputs must be lowered to less than 0.5V. Digital inputs on P1.0–P1.4 will not function normally.
- These parameters do not apply to P1.0–P1.4 if the A/D function is enabled.
- The input voltage slew rate should be  $<10V/ms$ . The maximum slew rate depends on the clock frequency of the microcontroller. Designers should use low pass filters before the A/D inputs as a precaution to noise edges causing false readings.

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AC ELECTRICAL CHARACTERISTICS

T<sub>amb</sub> = 0°C to +70°C or –40°C to +85°C, V<sub>CC</sub> = 5V ±10%, V<sub>SS</sub> = 0V<sup>4, 8</sup>

SYMBOL	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
		MIN	MAX	MIN	MAX	
1/t <sub>CLCL</sub>	Oscillator frequency:			3.5 3.5	12 16	MHz MHz
External Clock (Figure 4)						
t <sub>CHCX</sub>	High time	20		20		ns
t <sub>CLCX</sub>	Low time	20		20		ns
t <sub>CLCH</sub>	Rise time		20		20	ns
t <sub>CHCL</sub>	Fall time		20		20	ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal.

The designations are:

- C – Clock
- D – Input data
- H – Logic level high
- L – Logic level low
- Q – Output data
- T – Time
- V – Valid
- X – No longer a valid logic level
- Z – Float

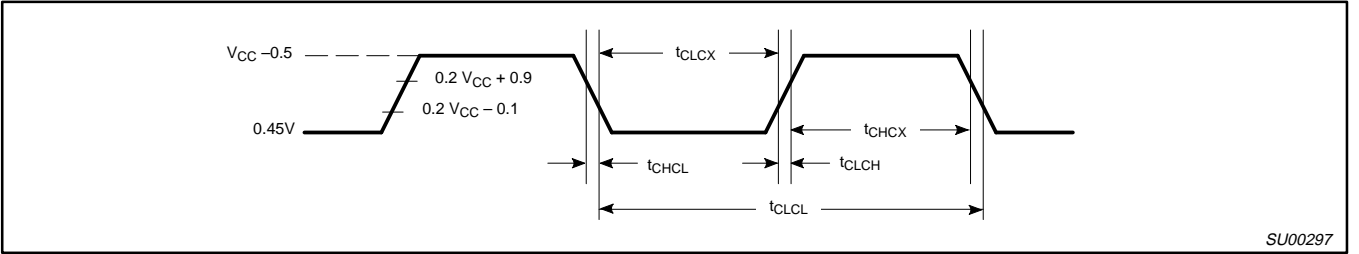


Figure 4. External Clock Drive

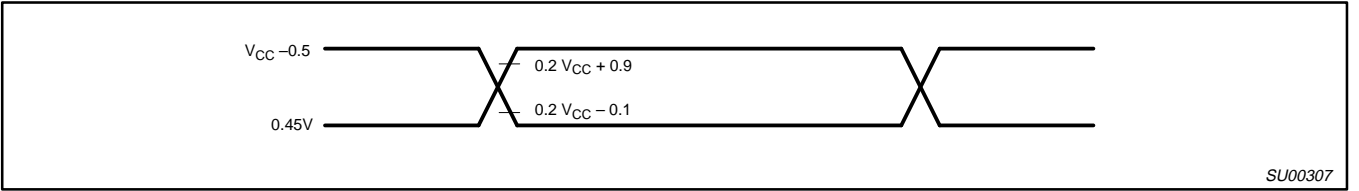
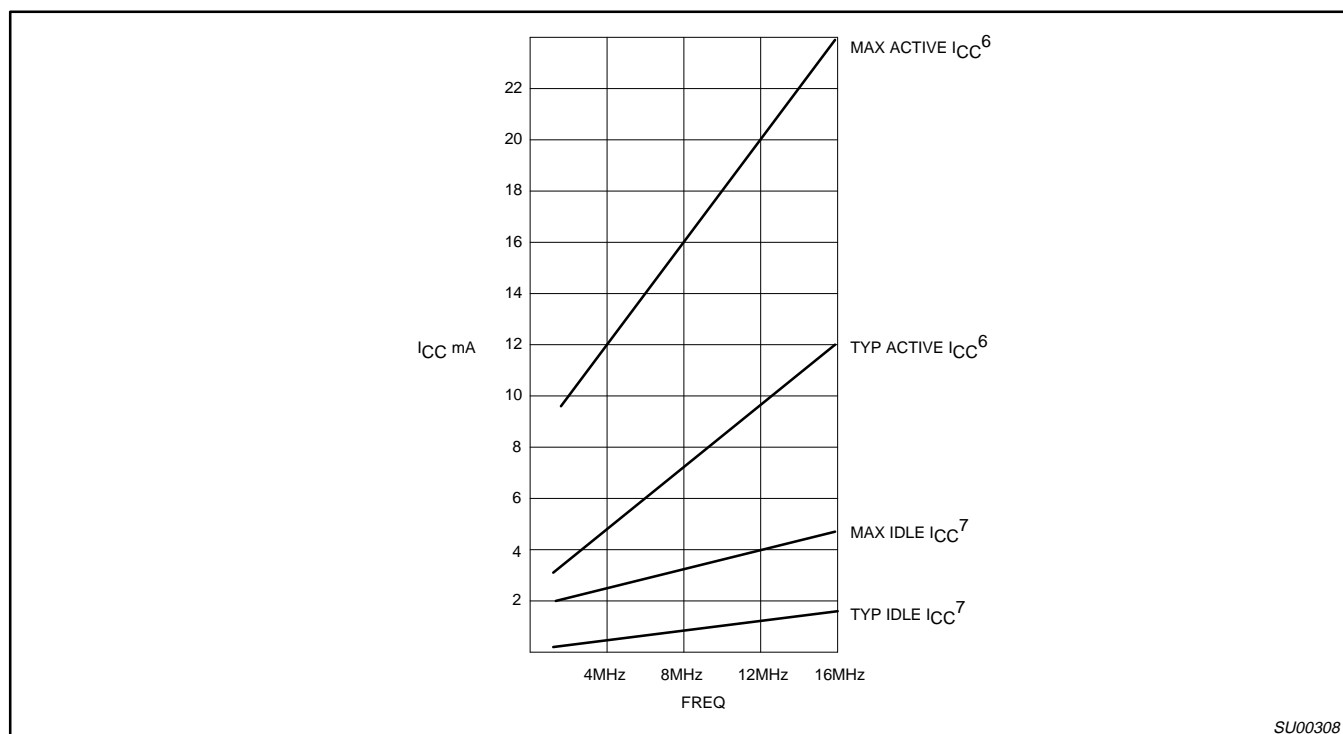


Figure 5. AC Testing Input/Output

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**Figure 6.  $I_{CC}$  vs. FREQ**  
 Maximum  $I_{CC}$  values taken at  $V_{CC} = 5.5V$  and worst case temperature.  
 Typical  $I_{CC}$  values taken at  $V_{CC} = 5.0V$  and  $25^{\circ}C$ .  
 Notes 6 and 7 refer to AC Electrical Characteristics.

## PROGRAMMING CONSIDERATIONS

### EPROM Characteristics

The 87C752 is programmed by using a modified Quick-Pulse Programming algorithm similar to that used for devices such as the 87C451 and 87C51. It differs from these devices in that a serial data stream is used to place the 87C752 in the programming mode.

Figure 7 shows a block diagram of the programming configuration for the 87C752. Port pin P0.2 is used as the programming voltage supply input ( $V_{PP}$  signal). Port pin P0.1 is used as the program (PGM/) signal. This pin is used for the 25 programming pulses.

Port 3 is used as the address input for the byte to be programmed and accepts both the high and low components of the eleven bit address. Multiplexing of these address components is performed using the ASEL input. The user should drive the ASEL input high and then drive port 3 with the high order bits of the address. ASEL should remain high for at least 13 clock cycles. ASEL may then be driven low which latches the high order bits of the address internally. The high address should remain on port 3 for at least two clock cycles after ASEL is driven low. Port 3 may then be driven with the low byte of the address. The low address will be internally stable 13 clock cycles later. The address will remain stable provided that the low byte placed on port 3 is held stable and ASEL is kept low. **Note:** ASEL needs to be pulsed high only to change the high byte of the address.

Port 1 is used as a bidirectional data bus during programming and verify operations. During programming mode, it accepts the byte to be programmed. During verify mode, it provides the contents of the

EPROM location specified by the address which has been supplied to Port 3.

The XTAL1 pin is the oscillator input and receives the master system clock. This clock should be between 1.2 and 6MHz.

The RESET pin is used to accept the serial data stream that places the 87C752 into various programming modes. This pattern consists of a 10-bit code with the LSB sent first. Each bit is synchronized to the clock input, X1.

### Programming Operation

Figures 8 and 9 show the timing diagrams for the program/verify cycle. RESET should initially be held high for at least two machine cycles. P0.1 (PGM/) and P0.2 ( $V_{PP}$ ) will be at  $V_{OH}$  as a result of the RESET operation. At this point, these pins function as normal quasi-bidirectional I/O ports and the programming equipment may pull these lines low. However, prior to sending the 10-bit code on the RESET pin, the programming equipment should drive these pins high ( $V_{IH}$ ). The RESET pin may now be used as the serial data input for the data stream which places the 87C752 in the programming mode. Data bits are sampled during the clock high time and thus should only change during the time that the clock is low. Following transmission of the last data bit, the RESET pin should be held low.

Next the address information for the location to be programmed is placed on port 3 and ASEL is used to perform the address multiplexing, as previously described. At this time, port 1 functions as an output.



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A high voltage  $V_{PP}$  level is then applied to the  $V_{PP}$  input (P0.2). (This sets Port 1 as an input port). The data to be programmed into the EPROM array is then placed on Port 1. This is followed by a series of programming pulses applied to the PGM/ pin (P0.1). These pulses are created by driving P0.1 low and then high. This pulse is repeated until a total of 25 programming pulses have occurred. At the conclusion of the last pulse, the PGM/ signal should remain high.

The  $V_{PP}$  signal may now be driven to the  $V_{OH}$  level, placing the 87C752 in the verify mode. (Port 1 is now used as an output port). After four machine cycles (48 clock periods), the contents of the addressed location in the EPROM array will appear on Port 1.

The next programming cycle may now be initiated by placing the address information at the inputs of the multiplexed buffers, driving the  $V_{PP}$  pin to the  $V_{PP}$  voltage level, providing the byte to be programmed to Port1 and issuing the 26 programming pulses on the PGM/ pin, bringing  $V_{PP}$  back down to the  $V_C$  level and verifying the byte.

### Programming Modes

The 87C752 has four programming features incorporated within its EPROM array. These include the USER EPROM for storage of the application's code, a 16-byte encryption key array and two security bits. Programming and verification of these four elements are selected by a combination of the serial data stream applied to the RESET pin and the voltage levels applied to port pins P0.1 and P0.2. The various combinations are shown in Table 4.

### Encryption Key Table

The 87C752 includes a 16-byte EPROM array that is programmable by the end user. The contents of this array can then be used to encrypt the program memory contents during a program memory verify operation. When a program memory verify operation is performed, the contents of the program memory location is XNOR'ed with one of the bytes in the 16-byte encryption table. The resulting data pattern is then provided to port 1 as the verify data. The encryption mechanism can be disable, in essence, by leaving the bytes in the encryption table in their erased state (FFH) since the XNOR product of a bit with a logical one will result in the original bit. The encryption bytes are mapped with the code memory in 16-byte groups. the first byte in code memory will be encrypted with the first byte in the encryption table; the second byte in code memory will be encrypted with the second byte in the encryption table and so forth up to and including the 16th byte. The encryption repeats in 16-byte groups; the 17th byte in the code memory will be encrypted with the first byte in the encryption table, and so forth.

### Security Bits

Two security bits, security bit 1 and security bit 2, are provided to limit access to the USER EPROM and encryption key arrays. Security bit 1 is the program inhibit bit, and once programmed

performs the following functions:

1. Additional programming of the USER EPROM is inhibited.
2. Additional programming of the encryption key is inhibited.
3. Verification of the encryption key is inhibited.
4. Verification of the USER EPROM and the security bit levels may still be performed.

(If the encryption key array is being used, this security bit should be programmed by the user to prevent unauthorized parties from reprogramming the encryption key to all logical zero bits. Such programming would provide data during a verify cycle that is the logical complement of the USER EPROM contents).

Security bit 2, the verify inhibit bit, prevents verification of both the USER EPROM array and the encryption key arrays. The security bit levels may still be verified.

### Programming and Verifying Security Bits

Security bits are programmed employing the same techniques used to program the USER EPROM and KEY arrays using serial data streams and logic levels on port pins indicated in Table 4. When programming either security bit, it is not necessary to provide address or data information to the 87C752 on ports 1 and 3.

Verification occurs in a similar manner using the RESET serial stream shown in Table 4. Port 3 is not required to be driven and the results of the verify operation will appear on ports 1.6 and 1.7.

Ports 1.7 contains the security bit 1 data and is a logical one if programmed and a logical zero if erased. Likewise, P1.6 contains the security bit 2 data and is a logical one if programmed and a logical zero if erased.

### Erase Characteristics

Erase of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Flourless part number 2345-5 or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm<sup>2</sup> rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erase leaves the array in an all 1s state.

**Table 4. Implementing Program/Verify Modes**

OPERATION	SERIAL CODE	P0.1 (PGM/)	P0.2 ( $V_{PP}$ )
Program user EPROM	296H	—*	$V_{PP}$
Verify user EPROM	296H	$V_{IH}$	$V_{IH}$
Program key EPROM	292H	—*	$V_{PP}$
Verify key EPROM	292H	$V_{IH}$	$V_{IH}$
Program security bit 1	29AH	—*	$V_{PP}$
Program security bit 2	298H	—*	$V_{PP}$
Verify security bits	29AH	$V_{IH}$	$V_{IH}$

**NOTE:**

\* Pulsed from  $V_{IH}$  to  $V_{IL}$  and returned to  $V_{IH}$ .

## CMOS single-chip 8-bit microcontrollers

## 83C752/87C752

**EPROM PROGRAMMING AND VERIFICATION**

$T_{amb} = 21^{\circ}\text{C}$  to  $+27^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	MIN	MAX	UNIT
$1/t_{CLCL}$	Oscillator/clock frequency	1.2	6	MHz
$t_{AVGL}^1$	Address setup to P0.1 (PROG-) low	$10\mu\text{s} + 24t_{CLCL}$		
$t_{GHAX}$	Address hold after P0.1 (PROG-) high	$48t_{CLCL}$		
$t_{DVGL}$	Data setup to P0.1 (PROG-) low	$38t_{CLCL}$		
$t_{DVGL}$	Data setup to P0.1 (PROG-) low	$38t_{CLCL}$		
$t_{GHDX}$	Data hold after P0.1 (PROG-) high	$36t_{CLCL}$		
$t_{SHGL}$	$V_{PP}$ setup to P0.1 (PROG-) low	10		$\mu\text{s}$
$t_{GHSL}$	$V_{PP}$ hold after P0.1 (PROG-)	10		$\mu\text{s}$
$t_{GLGH}$	P0.1 (PROG-) width	90	110	$\mu\text{s}$
$t_{AVQV}^2$	$V_{PP}$ low ( $V_{CC}$ ) to data valid		$48t_{CLCL}$	
$t_{GHGL}$	P0.1 (PROG-) high to P0.1 (PROG-) low	10		$\mu\text{s}$
$t_{SYNL}$	P0.0 (sync pulse) low	$4t_{CLCL}$		
$t_{SYNH}$	P0.0 (sync pulse) high	$8t_{CLCL}$		
$t_{MASEL}$	ASEL high time	$13t_{CLCL}$		
$t_{MAHLD}$	Address hold time	$2t_{CLCL}$		
$t_{HASET}$	Address setup to ASEL	$13t_{CLCL}$		
$t_{ADSTA}$	Low address to address stable	$13t_{CLCL}$		

**NOTES:**

1. Address should be valid at least  $24t_{CLCL}$  before the rising edge of P0.2 ( $V_{PP}$ ).
2. For a pure verify mode, i.e., no program mode in between,  $t_{AVQV}$  is  $14t_{CLCL}$  maximum.

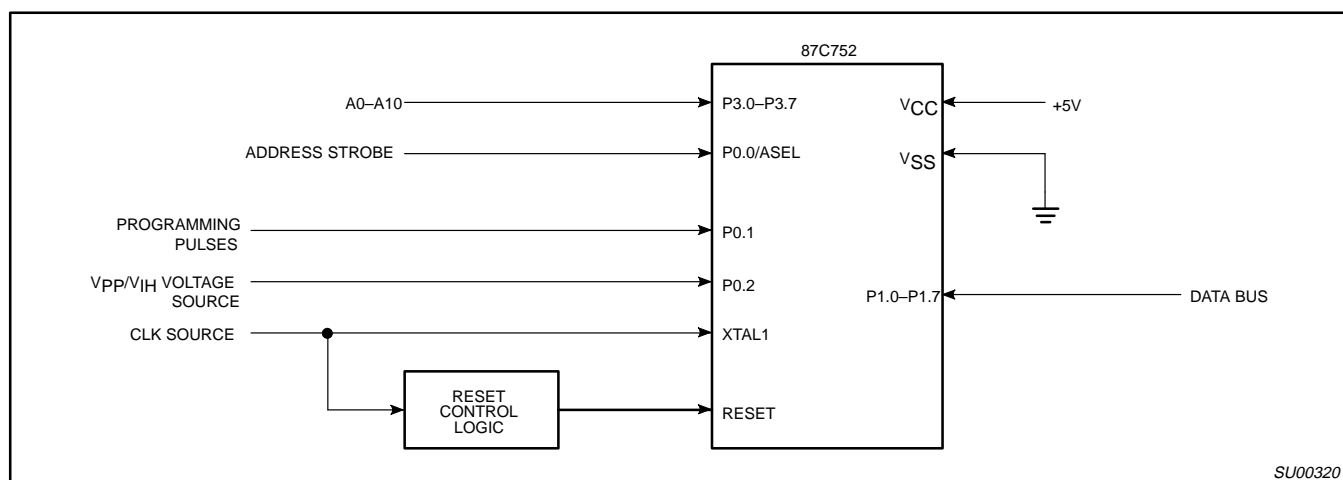


Figure 7. Programming Configuration

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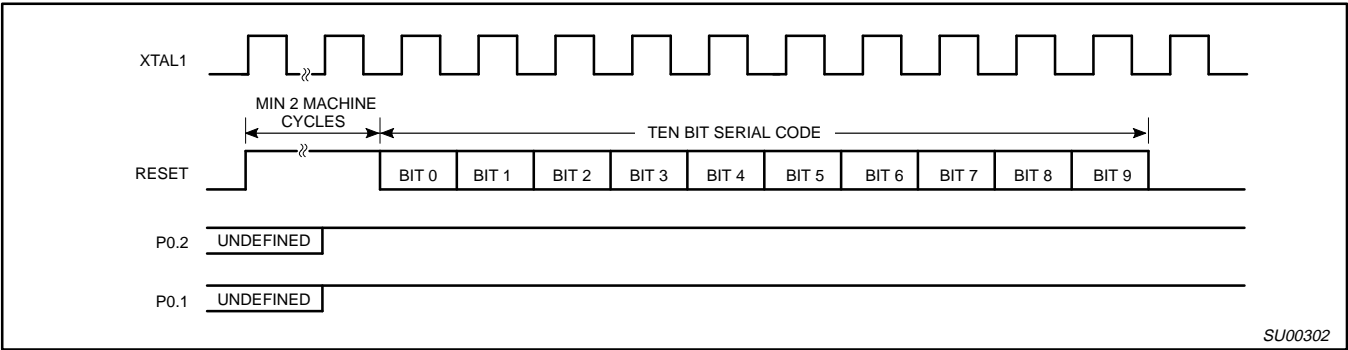


Figure 8. Entry into Program/Verify Modes

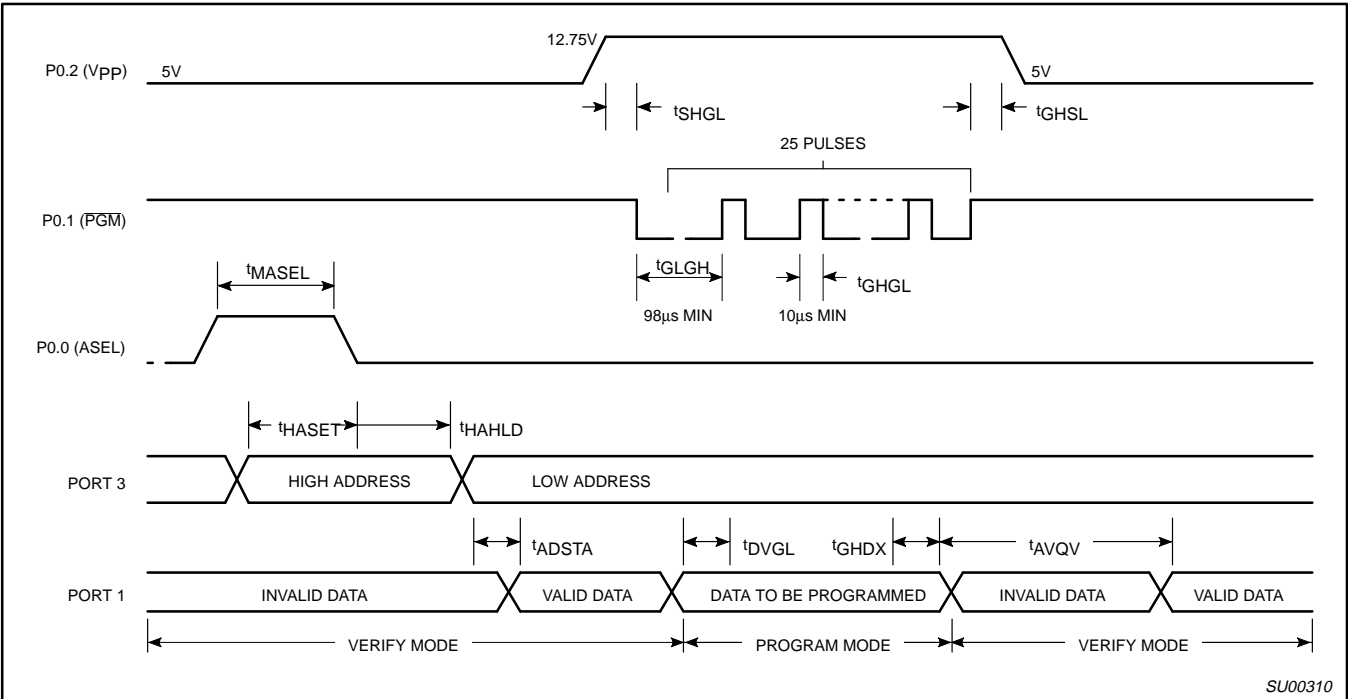


Figure 9. Program/Verify Cycle



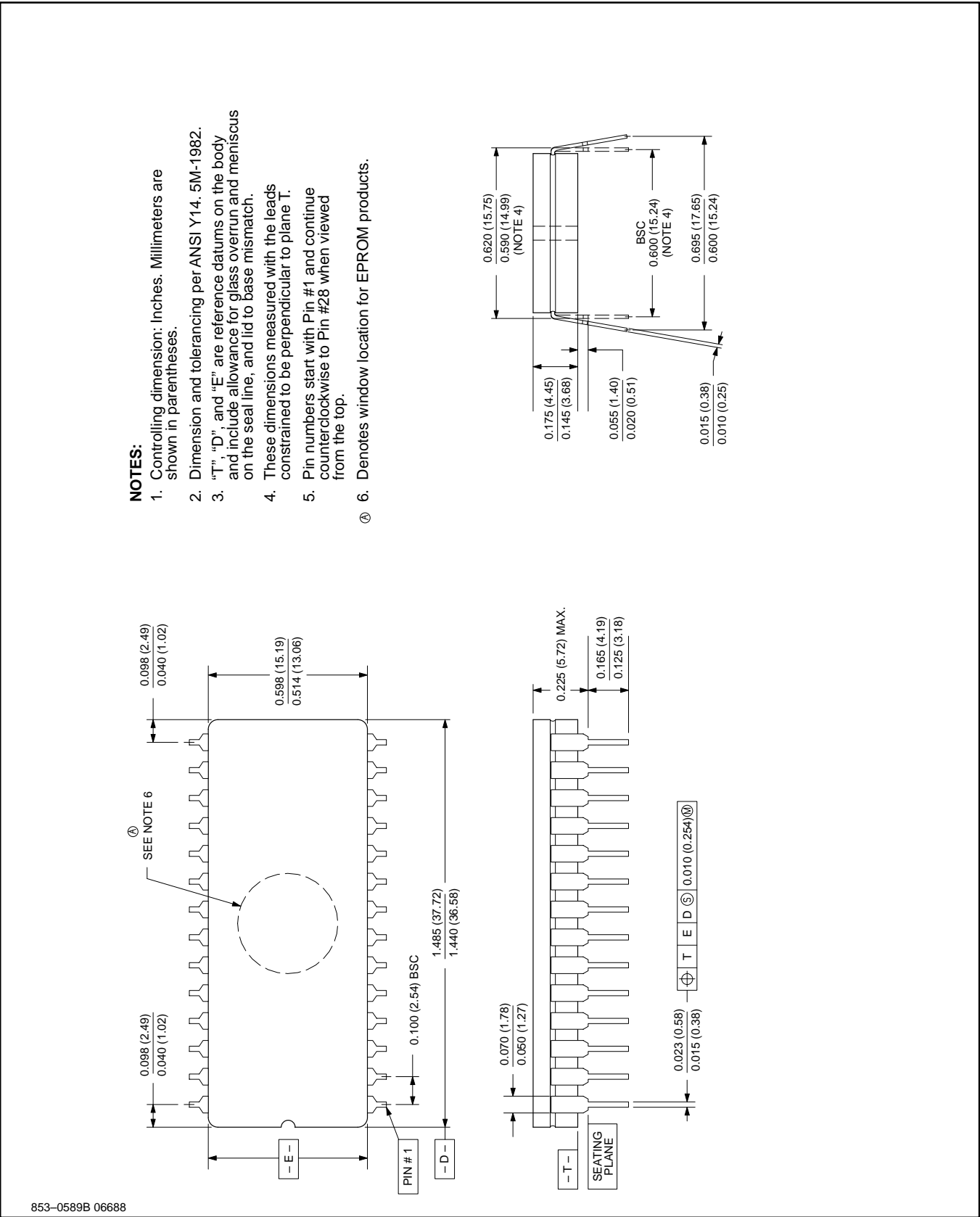
Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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0589B

28-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)

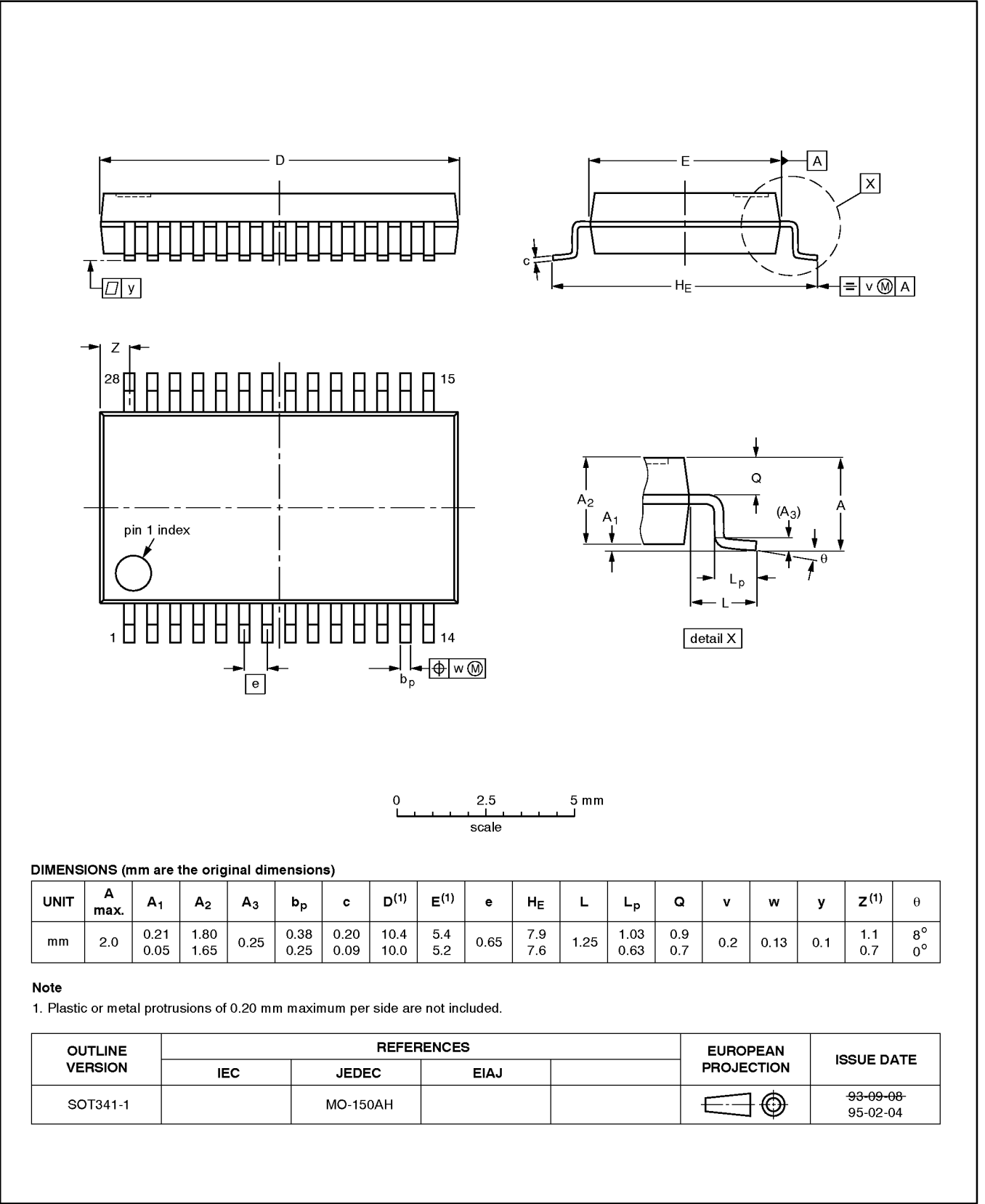


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SSOP28: plastic shrink small outline package; 28 leads; body width 5.3mm

SOT341-1

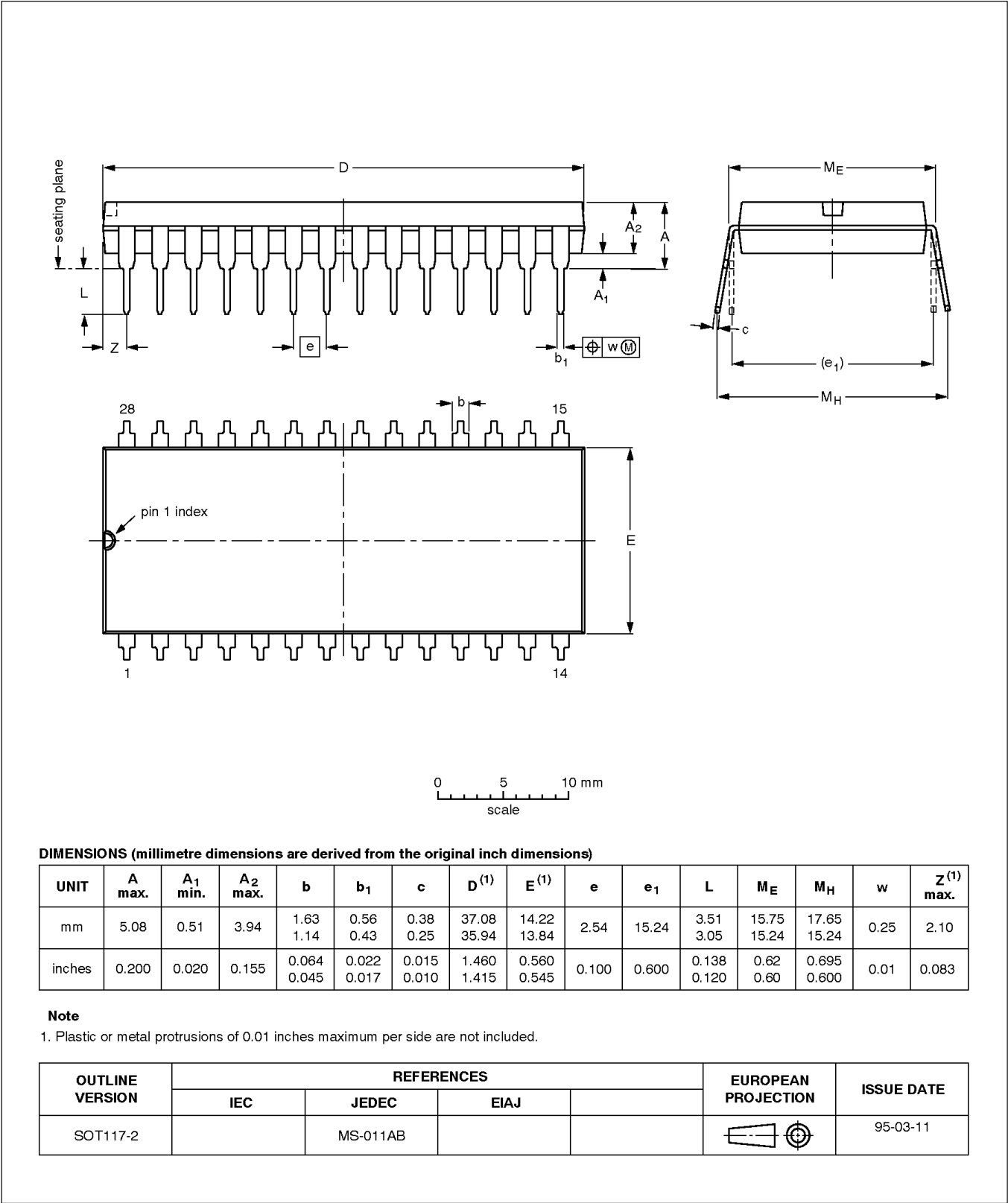


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DIP28: plastic dual in-line package; 28 leads (600 mil); long body

SOT117-2

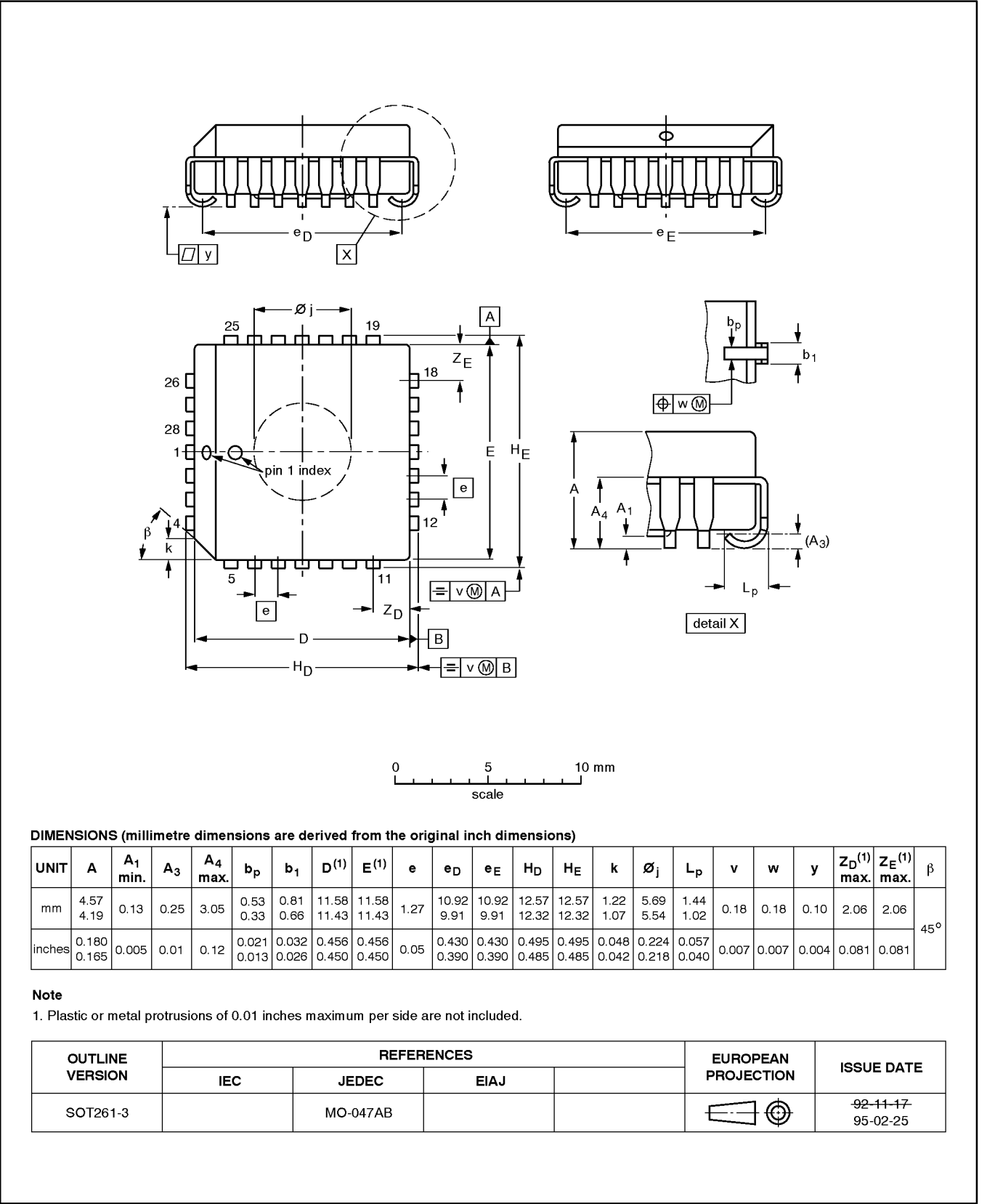


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PLCC28: plastic leaded chip carrer; 28 leads; pedestal

SOT261-3



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DEFINITIONS		
Data Sheet Identification	Product Status	Definition
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