DATA SHEET

82B715
I²C bus extender

Preliminary specification
Supesedes data of 1997 Apr 07
IC20 Data Handbook

1998 Jan 09

Philips
Semiconductors

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I²C bus extender 82B715

DESCRIPTION

The 82B715 is a bipolar integrated circuit intended for application in I²C bus systems.

While retaining all the operating modes and features of the I²C system it permits extension of the practical separation distance between components on the I²C bus by buffering both the data (SDA) and the clock (SCL) lines.

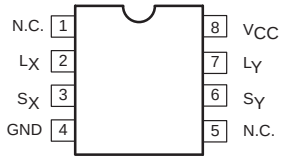
The I²C bus capacitance limit of 400pF restricts practical communication distances to a few meters. Using one 82B715 at each end of longer cables reduces the cable loading capacitance on the I²C bus by a factor of 10 times and may allow the use of low cost general purpose wiring to extend bus lengths.

FEATURES

- Dual, bi-directional, unity voltage gain buffer
- I²C bus compatible
- Logic signal levels may include both supply and ground
- X10 impedance transformation
- Wide supply voltage range

PIN CONFIGURATIONS

8-Pin Dual In-Line or SO
82B715



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PINNING

PIN	SYMBOL	FUNCTION
1	N.C.	
2	L_X	Buffered Bus, LDA or LCL
3	S_X	I²C Bus, SDA or SCL
4	GND	Negative Supply
5	N.C.	
6	S_Y	I²C Bus, SCL or SDA
7	L_Y	Buffered Bus, LCL or LDA
8	V_{CC}	Positive Supply

QUICK REFERENCE DATA

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
V_{CC}	Supply voltage	4.5		12	V
I_{CC}	Quiescent current		16		mA
I_{line}	Output sink capability	30			mA
V_{in}	Input voltage range	0		V_{CC}	V
V_{out}	Output voltage range	0		V_{CC}	V
Z_{in}/Z_{out}	Impedance transformation	8	10	13	
T_{amb}	Temperature range	–40		+85	°C

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
8-pin plastic dual In-line package	P82B715P N	SOT97-1
8-pin plastic small outline package	P82B715T D	SOT96-1

NOTE:
1. For applications requiring, 3V operation and additional buffer performance, see P82B96 Data Sheet.

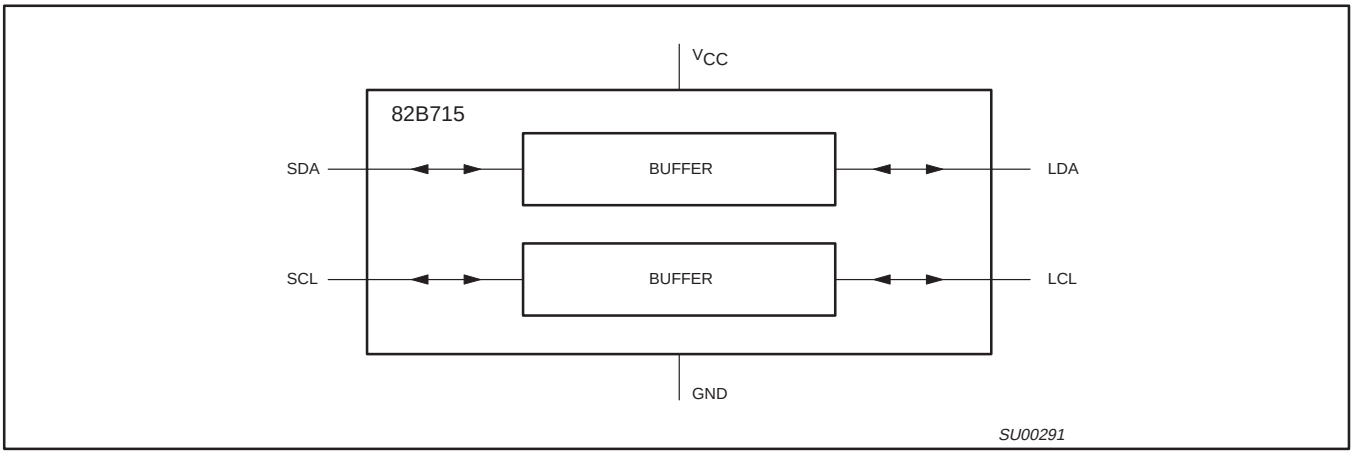


Figure 1. Block Diagram: 82B715

FUNCTIONAL DESCRIPTION

The 82B715 bipolar integrated circuit contains two identical buffer circuits which enable I²C and similar bus systems to be extended over long distances without degradation of system performance or requiring the use of special cables.

The buffer has an effective current gain of ten from I²C bus to Buffered bus. Whatever current is flowing out of the I²C bus side, ten times that current will be flowing into the Buffered bus side (see Figure 2).

As a consequence of this amplification the system is able to drive capacitive loads up to ten times the standard limit on the Buffered bus side. This current based buffering approach preserves the bi-directional, open-collector/open-drain characteristic of the I²C SDA/SCL lines.

To minimize interference and ensure stability, current rise and fall rates are internally controlled.

APPLICATION NOTES

By using two (or more) 82B715 ICs, a sub-system can be built which retains the interface characteristics of an I²C device so that it may be included in, or optionally added to, any I²C or related system.

The sub-system features a low impedance or “Buffered” bus, capable of driving large wiring capacities (see Figure 3).

I²C Systems

As with the standard I²C system, pull-up resistors are required to aprovide the logic HIGH levels on the Buffered bus. (Standard open-collector configuration of the I²C bus). The size and number of these pull-up resistors depends on the system.

If the buffer is to be permanently connected into the system, the circuit should be configured with only one pull-up resistor on the Buffered bus and none on the I²C bus.

Alternatively a buffer may be connected to an existing I²C system. In this case the Buffered bus pull-up will act in parallel with the I²C bus pull-up.

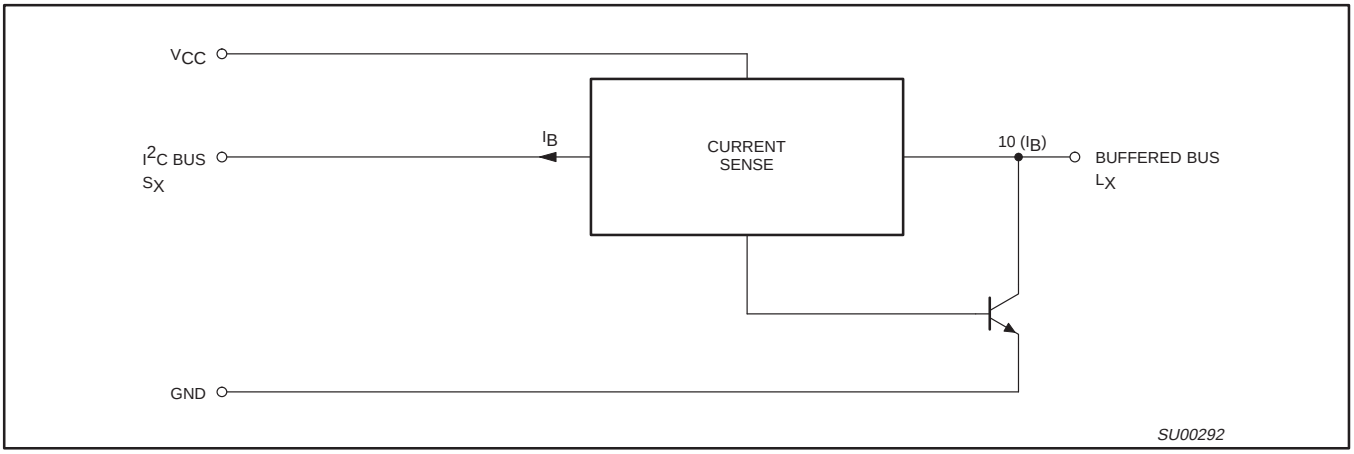


Figure 2. Equivalent Circuit: One Half 82B715

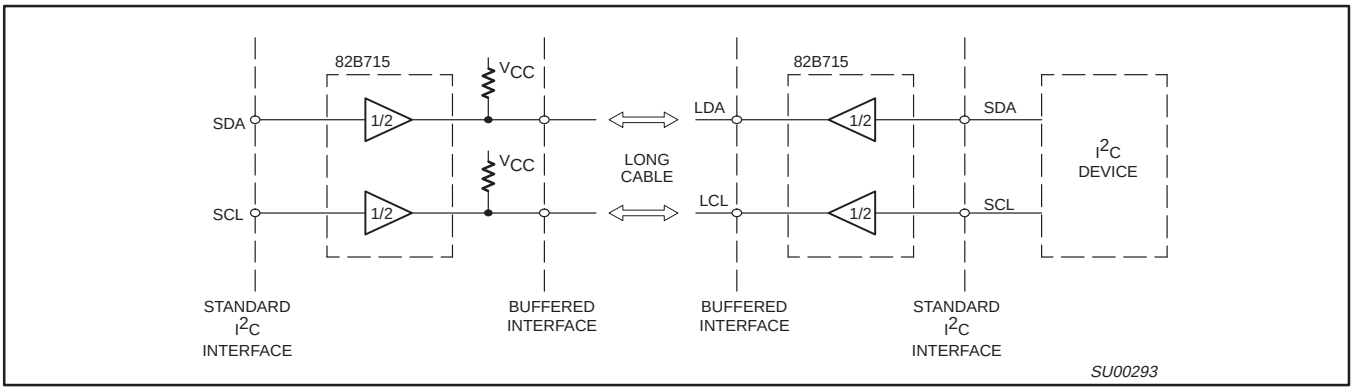


Figure 3. Minimum Sub-System with 82B715

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND (DIL-8 pin 4).

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC} to GND	Supply voltage range V_{CC}	–0.3	+12	V
V_{bus}	Voltage range I²C Bus, SCL or SDA	0	V_{CC}	V
V_{buff}	Voltage range Buffered Bus	0	V_{CC}	V
I	DC current (any pin)		60	mA
P_{tot}	Power dissipation		300	mW
T_{stg}	Storage temperature range	–55	+125	°C
T_{amb}	Operating ambient temperature range	–40	+85	°C

CHARACTERISTICS

At T_{amb} = +25°C and V_{CC} = 5 Volts, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
Power Supply					
V_{CC}	Supply voltage (operating)	4.5	—	12	V
I_{CC}	Supply current	—	16	—	mA
I_{CC}	Supply current at V_{CC} = 12V	—	22	—	mA
I_{CC}	Supply current, both I²C inputs LOW, both buffered outputs sinking 30mA.	—	28	—	mA
Drive Currents					
I_{Sx}, I_{Sy}	Output sink on I²C bus V_{Sx}, V_{Sy} LOW = 0.4V V_{Lx}, V_{Ly} LOW on Buffered bus = 0.3V	3	—	—	mA
I_{Lx}, I_{Ly}	Output sink on Buffered bus V_{Lx}, V_{Ly} LOW = 0.4V V_{Sx}, V_{Sy} LOW on I²C bus = 0.3V	30	—	—	mA
Input Currents					
I_{Sx}, I_{Sy}	Input current from I²C bus when I_{Lx}, I_{Ly} sink on Buffered bus = 30mA	—	—	3	mA
I_{Lx}, I_{Ly}	Input current from Buffered bus when I_{Sx}, I_{Sy} sink on I²C bus = 3mA	—	—	3	mA
I_{Lx}, I_{Ly}	Leakage current on Buffered bus V_{Lx}, V_{Ly} = V_{CC}, and V_{Sx}, V_{Sy} = V_{CC}	—	—	200	µA
Impedance Transformation					
Z_{in}/Z_{out}	Input/Output impedance	8	10	13	

Pull-Up Resistance Calculation

In calculating the pull-up resistance values, the gain of the buffer introduces scaling factors which must be applied to the system components. Viewing the system from the Buffered bus, all I²C bus capacitances have effectively 10 times their I²C bus value.

In practical systems the pull-up resistance is determined by the rise time limit for I²C systems. As an approximation this limit will be satisfied if the time constant (product of the net resistance and net capacitance) of the total system is set to 1 microsecond.

The total time constant may either be set by considering each bus node individually (i.e., the I²C nodes, and the Buffered bus node) and choosing pull-up resistors to give time constants of 1 microsecond for each node; or by combining the capacitances into an equivalent capacitive loading on the Buffered bus, and calculating the Buffered bus pull-up resistor required by this equivalent capacitance.

For each separate bus the pull-up resistor may be calculated as follows:

$$R = \frac{1\mu\,\text{sec}}{C_{device} + C_{wiring}}$$

Where: C_{device} = sum of device capacitances connected to each bus,

and C_{wiring} = total wiring and stray capacitance on each bus.

If these capacitances are not known then a good approximation is to assume that each device presents 10pF of load capacitance and 10pF of wiring capacitance.

The capacitance figures for one or more individual I²C bus nodes should be multiplied by a factor of 10 times, and then added to the Buffered bus capacitance. Calculation of a new Buffered bus pull-up resistor will alllow this single pull-up resistor to act for both the included I²C bus nodes and the Buffered bus. Thus it is possible to combine some or all of these separate pull-up resistors into a single resistor on the Buffered bus (the value of which is calculated from the sum of the scaled capacitances on the Buffered bus). If the buffer is to be permanently connected into the system then all the separate pull-up resistors should be combined. But if it is to be connected by adding it onto an existing system, then only those on the additional I²C bus system can be combined onto the Buffered bus if the original system is required to be able to still operate on a stand-alone basis.

A further restriction is that the maximum pull-up current, with the bus LOW, should not exceed the I²C bus specification maximum of 3mA, or 30mA on the Buffered bus. The following formula applies:

$$30\text{mA} > \frac{V_{CC} - 0.4}{R_P}$$

Where: R_P = scaled parallel combination of all pull-up resistors.

If this condition is met, the fall time specifications will also be met.

Figure 4 shows typical loading calculations for the expanded I²C bus.

Sx, Sy, I²C Bus, SDA or SCL

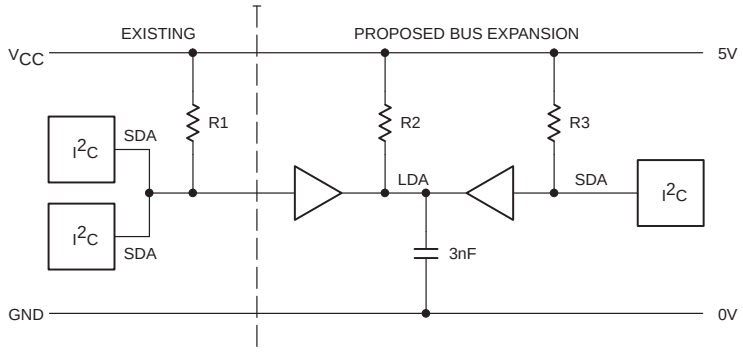
Because the two buffer circuits in the 82B715 are identical either input pin can be used as the I²C Bus SDA data line, or the SCL clock line.

Lx, Ly, Buffered Bus, LDA or LCL

On the buffered low impedance line side, the corresponding output becomes LDA and LCL.

V_{CC}, GND — Positive and Negative Supply Pins

In normal use the power supply voltages at each end of the low impedance line should be comparable. If these differ by a significant amount, noise margin is sacrificed.



EFFECTIVE CAPACITANCE NEAR I²C DEVICES

2 × I²C Devices	20pF
Strays	20pF
82B715 Buffer	10pF
TOTAL CAP.	50pF

I²C pull-up

$$R1 = \frac{1\mu sec}{50pF} = 20K\Omega$$

EFFECTIVE CAPACITANCE BUFFERED LINE

Wiring Cap.	3000pF
TOTAL CAP.	3000pF

Buffered Bus pull-up

$$R2 = \frac{1\mu sec}{3000pF} = 333\Omega$$

EFFECTIVE CAPACITANCE REMOTE I²C DEVICES

1 × I²C Devices	10pF
Strays	10pF
82B715 Buffer	10pF
TOTAL CAP.	30pF

I²C pull-up

$$R3 = \frac{1\mu sec}{30pF} = 33K\Omega$$

AS AN ADDITION TO AN EXISTING SYSTEM * :

R1 = 20KΩ

$$R2' = \frac{R2 \times 0.1R3}{R2 + 0.1R3} = 300\Omega$$

R3 not required since buffer always connected

FOR A PERMANENT SYSTEM * :

R1 not required since buffer always connected

$$R2' = \frac{1}{\frac{1}{0.1R1} + \frac{1}{0.1R2} + \frac{1}{0.1R3}} = 262\Omega$$

R3 not required since buffer always connected

*** NOTE:**
R1, R2 and R3 are calculated from the capacitive loading and a 1µsec time constant on each bus node. For an addition to an existing system, R2' (the new value for R2) is shown as being calculated from the parallel combination of R2 and the scaled value of R3; while for a permanent system R2, and scaled values of R1 and R3 have been used. Note that this example has used scaled resistor values and combined the node and cable capacitances.

CHECK FOR MAXIMUM PULL-UP CURRENT:

$$\frac{(5 - 0.4)V}{260\Omega} = 17.6mA < 30mA$$

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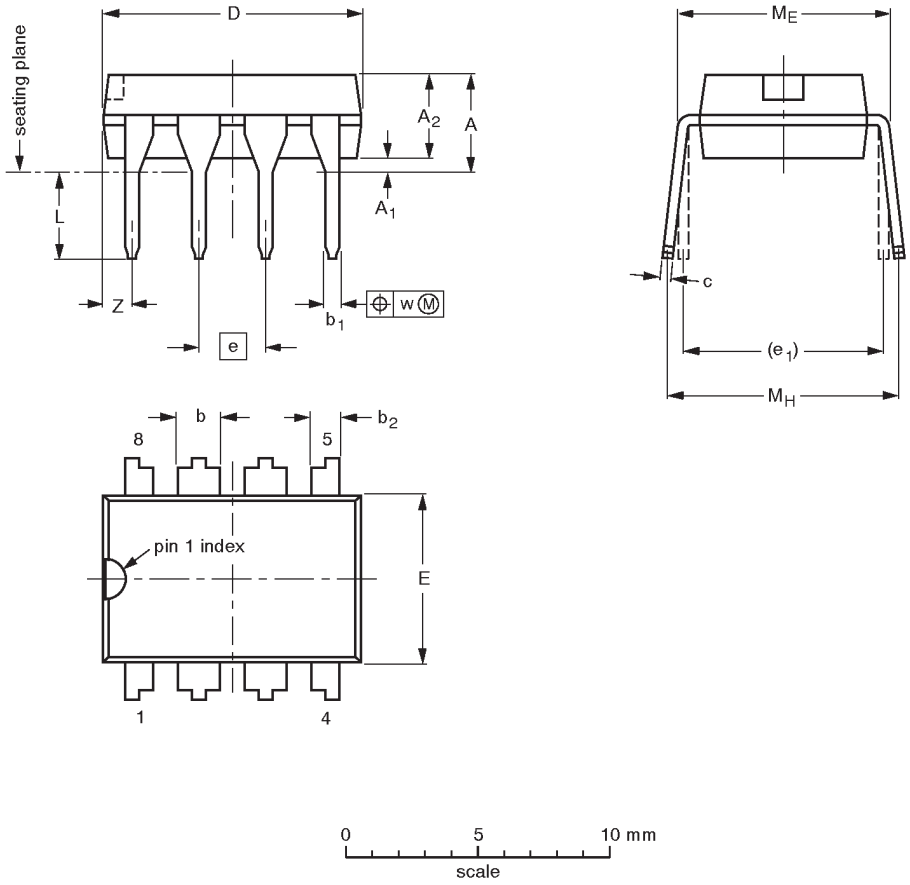
Figure 4. Typical Loading Calculation: I²C Bus with 82B715

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

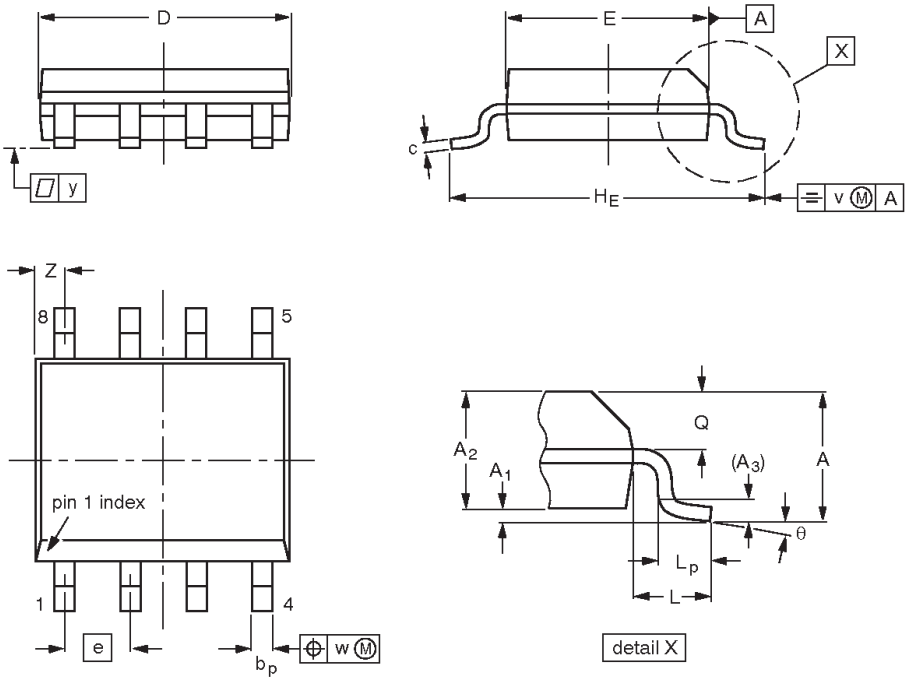
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

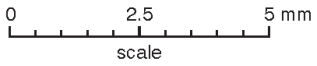
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 3.9mm SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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