IS80C52/32

CMOS SINGLE CHIP 8-BIT MICROCONTROLLER

ADVANCE INFORMATION ARPIL 1997

FEATURES

- 8K x 8 ROM (IS80C52 only)
- 256 x 8 RAM
- Three 16-bit timers/counters
- Full duplex serial channel
- Boolean processor
- Four 8-bit I/O ports, 32 I/O lines
- External memory expandable to 128K
- Two security bits
- CMOS and TTL compatible
- Maximum speed range: 40 MHz @ Vcc = 5V
- Packages available:
  - 40-pin DIP
  - 44-pin PLCC
  - 44-pin PQFP

GENERAL DESCRIPTION

The ISSI IS80C52/32 is a high-performance microcontroller fabricated using high-density CMOS technology. The CMOS IS80C52/32 is functionally compatible with the NMOS Intel 8052/32 microcontroller.

The IS80C52 is designed with 8K x 8 ROM; 256 x 8 RAM; 32 I/O lines for either multiprocessor communications, I/O expansion, or full duplex UART; three 16-bit timers/counters; a five-source, two-priority-level, nested interrupt structure; and an on-chip oscillator and clock circuit. The IS80C52 can be expanded using standard TTL compatible memory.

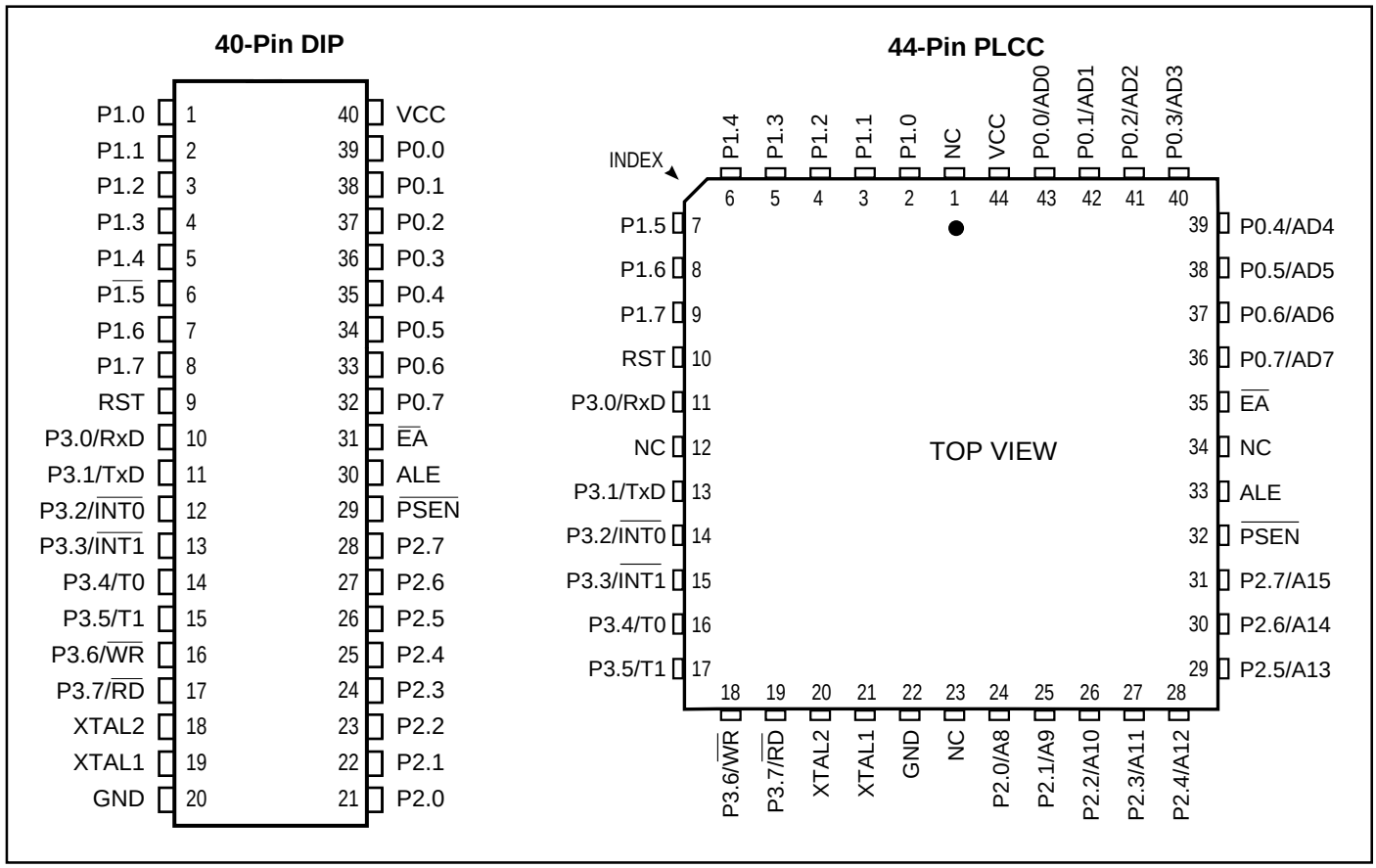

Figure 1. IS80C52/32 Pin Configurations

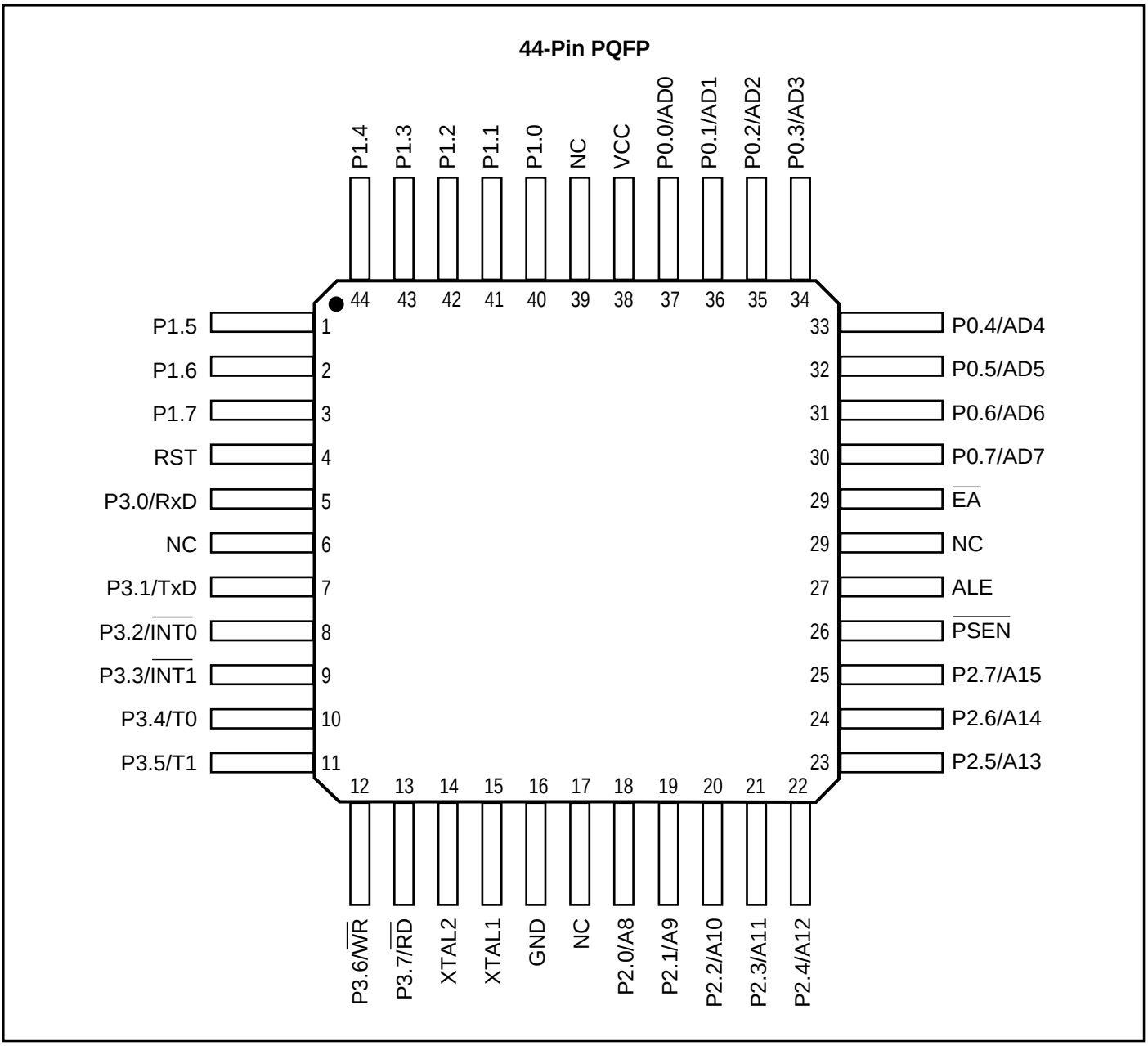

Figure 1. IS80C52/32 Pin Configurations *(continued)*

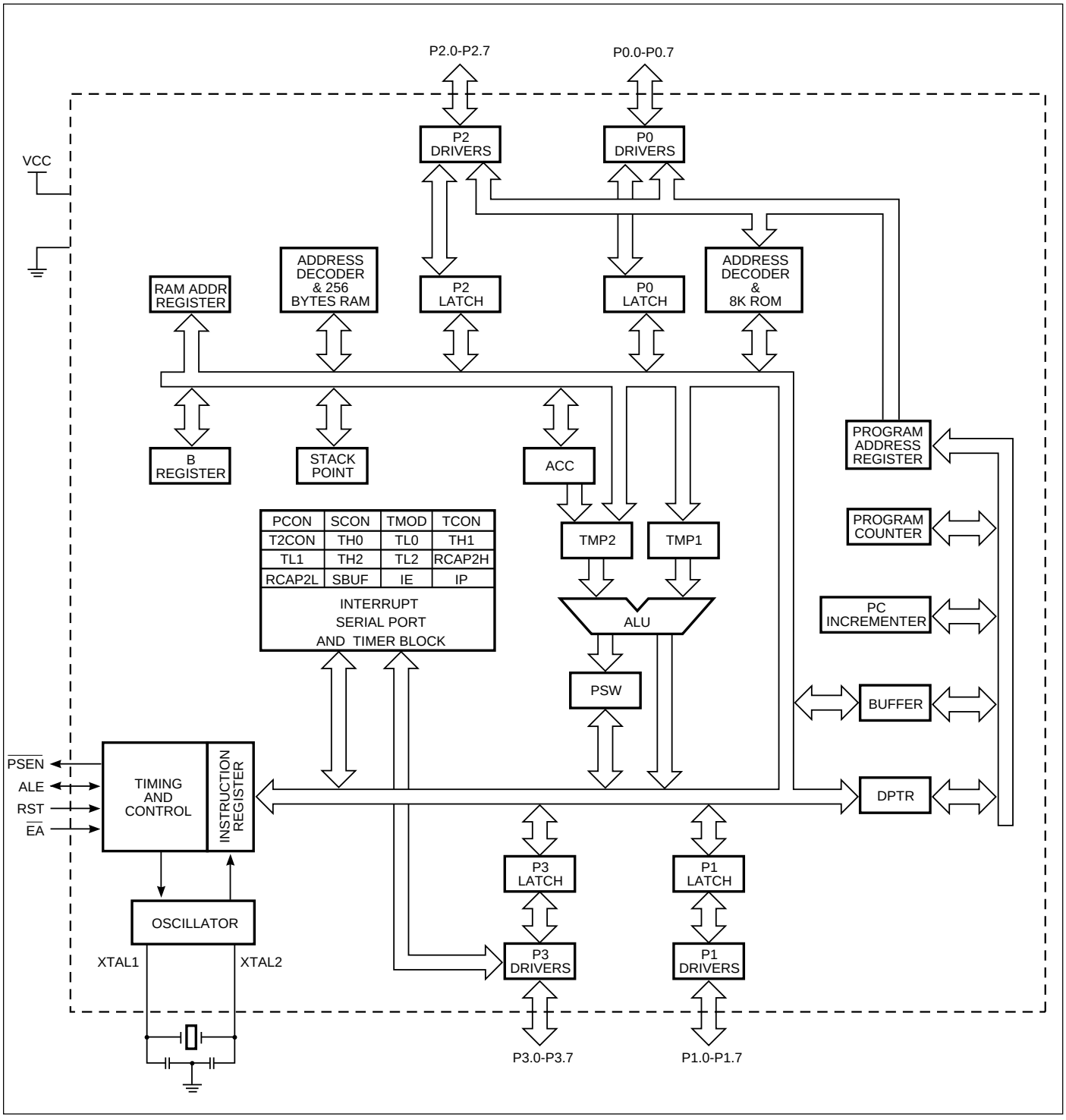

Figure 2. IS80C52 Block Diagram

PIN DESCRIPTION

Symbol	DIP	PLCC	QFP	I/O	Name and Function
P1.0-P1.7	1-8	2-9	40-44	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pullups.
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to GND permits a power-on reset using only an external capacitor. A small internal resistor permits power-on reset using only a capacitor connected to VCC.
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pullups. Port 3 also serves the special features of the IS80C52, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
XTAL 2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.
XTAL 1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
GND	20	22	16	I	Ground: 0V reference.
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pullups. Port 2 emits the high order address byte during fetches from external program memory and during accesses to external data memory that used 16-bit addresses. In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses, Port 2 emits the contents of the P2 special function register.

(continued)

PIN DESCRIPTION (continued)

Pin Symbol	DIP	PLCC	QFP	I/O	Name and Function
$\overline{\text{PSEN}}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
ALE	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an address to the external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and be used for external timing or clocking. Note that one ALE pulse is skipped during each access external data memory.
$\overline{\text{EA}}$	31	35	29	I	**External Access enable:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH.
P0.0-P0.7	39-32	43-36	30-37	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pullups when emitting 1s.
Vcc	40	44	38	I	**Power Supply:** This is the power supply voltage for operation.

OPERATING DESCRIPTION

The detail description of the IS80C52 included in this description are:

- Memory map and registers
- Timers/counters
- Serial interface
- Interrupt system
- Instruction
- Other information

Memory Map and Registers

Memory

The IS80C52 has separate address spaces for program and data memory. The program memory can be up 64K bytes long. The lower 4K can reside on-chip. Figure 3 shows a map of the IS80C52 program memory.

The IS80C52 has 256 bytes of on-chip RAM, plus a number of special function registers. The lower 128 bytes can be accessed either by direct addressing or by indirect addressing. Figure 4 shows data memory origination.

The 128 bytes of RAM which can be accessed by both direct and indirect addressing can be divided into three segments as listed below and shown in Figure 5.

1. *Register Banks 0-3:* locations 0 through 1FH (32 bytes). The device after reset defaults to register bank 0. To use the other register banks, the user must select them in software. Each register bank contains eight 1-byte registers 0-7. Reset initializes the stack point to location 07H, and is incremented once to start from 08H, which is the first register of the second bank.
2. *Bit Addressable Area:* 16 bytes have been assigned for this segment 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). The bits can be referred to in two ways, both of which are acceptable by most assemblers. One way is referencing to bytes 20H-2FH. Thus, bits 0-7 can also be referred to as bits 20.0-20.7, and bits 8-FH are the same as 21.0-21.7, and so on. Each of the 16 bytes in this segment can also be addressed as a byte.
3. *Scratch Pad Area:* 30-7FH are available to the user as data RAM. However, if the data pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.

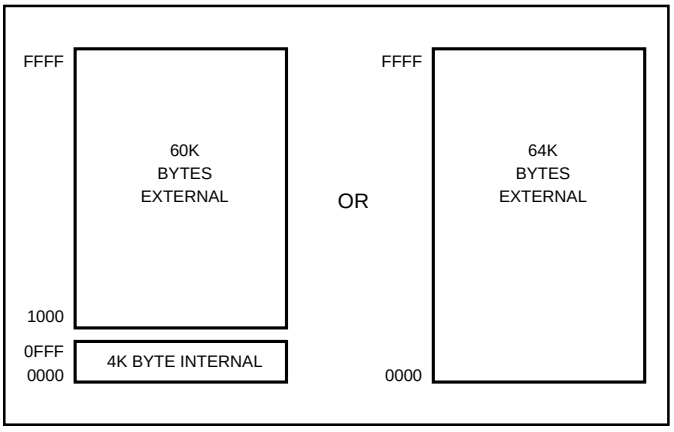

Figure 3. Program Memory Access Range

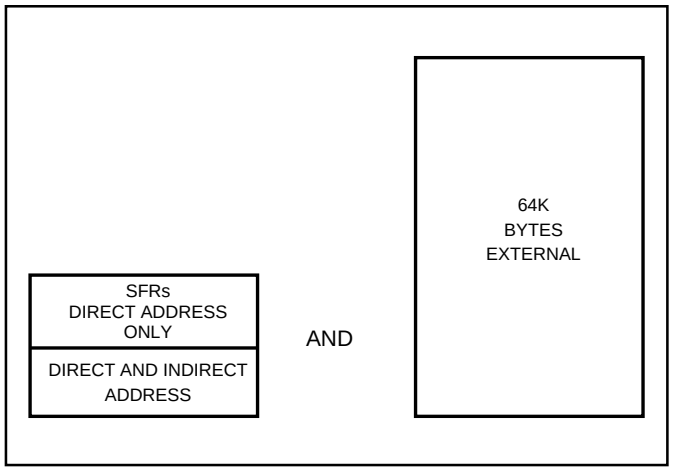

Figure 4. Data Memory Access Range

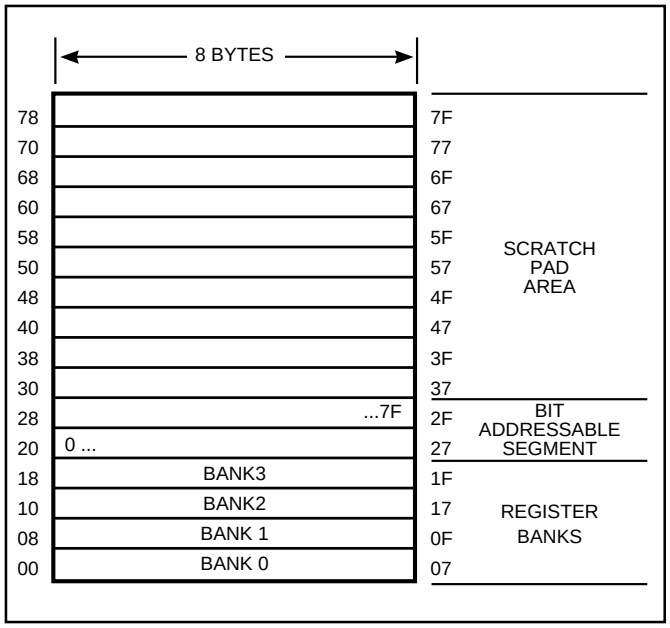

Figure 5. 128 Bytes of RAM Direct and Indirect Addressable

SPECIAL FUNCTION REGISTER

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function								Reset Value
ACC(1)	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B(1)	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPH	Data pointer high	83H									00H
DPL	Data pointer low	82H									00H
IE(1)	Interrupt enable	A8H	**AF** EA	**AE** —	**AD** —	**AC** ES	**AB** ET1	**AA** EX1	**A9** ET0	**A8** EX0	0X000000B
IP(1)	Interrupt priority	B8H	**BF** —	**BE** —	**BD** —	**BC** PS	**BB** PT1	**BA** PX1	**B9** PT0	**B8** PX0	XXX00000B
P0(1)	Port 0	80H	**87** P0.7	**86** P0.6	**85** P0.5	**84** P0.4	**83** P0.3	**82** P0.2	**81** P0.1	**80** P0.0	FFH
P1(1)	Port 1	90H	**97** P1.7	**96** P1.6	**95** P1.5	**94** P1.4	**93** P1.3	**92** P1.2	**91** P1.1	**90** P1.0	FFH
P2(1)	Port 2	A0H	**A7** P2.7	**A6** P2.6	**A5** P2.5	**A4** P2.4	**A3** P2.3	**A2** P2.2	**A1** P2.1	**A0** P2.0	FFH
P3(1)	Port 3	B0H	**B7** P3.7	**B6** P3.6	**B5** P3.5	**B4** P3.4	**B3** P3.3	**B2** P3.2	**B1** P3.1	**B0** P3.0	FFH
PCON	Power control	87H	SMOD	—	—	—	GF1	GF0	PD	IDL	0XXX0000B
PSW(1)	Program status word	D0H	**D7** CY	**D6** AC	**D5** F0	**D4** RS1	**D3** RS0	**D2** OV	**D1** —	**D0** P	00H
SBUF	Serial data buffer	99H									XXXXXXXXB
SCON(1)	Serial controller	98H	**9F** SM0	**9E** SM1	**9D** SM2	**9C** REN	**9B** TB8	**9A** RB8	**99** TI	**98** RI	00H
SP	Stack pointer	81H									07H
TCON(1)	Timer control	88H	**8F** TF1	**8E** TR1	**8D** TF0	**8C** TR0	**8B** IE1	**8A** IT1	**89** IE0	**88** IT0	
TH0	Timer high 0	8CH									00H
TH1	Timer high 1	8DH									00H
TL0	Timer low 0	8AH									00H
TL1	Timer low 1	8BH									00H
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

Note:
1. Denotes bit addressable.

The detail description of each bit is as follows:

PSW

CY	AC	F0	RS1	RS0	OV	—	P

CY	PSW.7	Carry flag
AC	PSW.6	Auxiliary carry flag
F0	PSW.5	Flag 0 available to the user for general purpose
RS1	PSW.4	Register bank selector bit 1
RS0	PSW.3	Register bank selector bit 0(1)
OV	PSW.2	Overflow flag
—	PSW.1	Usable as a general purpose flag
P	PSW.0	Parity flag. Set/clear by hardware each instruction cycle to indicate an odd/even number of "1" bus in the accumulator

Note:

1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	Register Bank	Address
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

PCON

SMOD	—	—	—	GF1	GF0	PD	IDL

SMOD	Double baud rate bit. If Timer 1 is used to generate baud rate and SMOD=1, the baud rate is doubled when the serial port is used in modes 1, 2, or 3.
—	Not implemented, reserve for future use.
—	Not implemented, reserve for future use.
—	Not implemented, reserve for future use.
GF1	General purpose flag bit.
GF0	General purpose flag bit.
PD	Power-down bit. Setting this bit activates power-down operation in the IS80C52.
IDL	Idle mode bit. Setting this bit activates idle mode operation in the IS80C52. If 1s are written to PD and IDL at the same time, PD takes precedence.

IE

EA	—	—	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disable all interrupts. If EA=0, no interrupt will be acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Not implemented, reserve for future use.
—	IE.5	Not implemented, reserve for future use.
ES	IE.4	Enable or disable the serial port interrupt.
ET1	IE.3	Enable or disable the timer 1 overflow interrupt.
EX1	IE.2	Enable or disable external interrupt 1.
ET0	IE.1	Enable or disable the timer 0 overflow interrupt.
EX0	IE.0	Enable or disable external interrupt 0.

IP

—	—	—	PS	PT1	PX1	PT0	PX0

—	IP.7	Not implemented, reserve for future use.
—	IP.6	Not implemented, reserve for future use.
—	IP.5	Not implemented, reserve for future use.
PS	IP.4	Defines the serial port interrupt priority level.
PT1	IP.3	Defines the timer 1 interrupt priority level.
PX1	IP.2	Defines the external interrupt 1 priority level
PT0	IP.1	Defines the timer 0 interrupt priority level.
PX0	IP.0	Defines the external interrupt 0 priority level

TCON

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1 TCON.7 Timer 1 overflow flag. Set by hardware when the timer/counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine.

TR1 TCON.6 Timer 1 run control bit. Set/cleared by software to turn timer/counter 1 ON/OFF.

TF0 TCON.5 Timer 0 overflow flag. Set by hardware when the timer/counter 0 overflows. Cleared by hardware as processor vectors to the interrupt service routine.

TR0 TCON.4 Timer 0 run control bit. Set/cleared by software to turn timer/counter 0 ON/OFF.

IE1 TCON.3 External interrupt 1 edge flag. Set by software when external interrupt edge is detected. Cleared by hardware when interrupt is processed.

IT1 TCON.2 Interrupt 1 type control bit. Set/ cleared by software specify falling edge/low level triggered external interrupt.

IE0 TCON.1 External interrupt 0 edge flag. Set by software when external interrupt edge is detected. Cleared by hardware when interrupt is processed.

IT0 TCON.0 Interrupt 0 type control bit. Set/cleared by software specify falling edge/ low level triggered external interrupt.

TMOD

Timer 1				Timer 0			
GATE	**C/T**	**M1**	**M0**	**GATE**	**C/T**	**M1**	**M0**

GATE When TRx (in TCON) is set and GATE=1, TIMER/COUNTERx will run only while INTx pin is high (hardware control). When GATE=0, TIMER/COUNTERx will run only while TRx=1 (software control).

C/T Timer or counter selector. Cleared for timer operation (input from internal system clock). Set for counter operation (input from Tx input pin).

M1 Mode selector bit.(2)

M0 Mode selector bit.(2)

Note 2:

M1	M0	Operating mode
0	0	Mode 0. (13-bit timer)
0	1	Mode 1. (16-bit timer/counter)
1	0	Mode 2. (8-bit auto-load timer/counter)
1	1	Mode 3. (TL0 is an 8-bit timer/counter controller by the standard timer 0 control bits. TH0 is an 8-bit timer and is controlled by timer 1 controller bits.)
1	1	Mode 3. (Timer/counter 1 stopped).

SCON

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SM0	SCON.7	Serial port mode specifier.(3)
SM1	SCON.6	Serial port mode specifier.(3)
SM2	SCON.5	Enable the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2=1 then RI will not be activated if valid stop bit was not receive. In mode 0, SM2 should be 0.
REN	SCON.4	Set/cleared by software to enable/disable reception.
TB8	SCON.3	The 9th bit that will be transmitted in mode 2 and 3. Set/cleared by software.
RB8	SCON.2	In modes 2 and 3, RB8 is the 9th data bit that was received. In mode 1, if SM2=0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	SCON.1	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software.
RI	SCON.0	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes (except see SM2). Must be cleared by software.

Note 3:

SM0	SM1	MODE	Description	Baud rate
0	0	0	Shift register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fosc/64 or Fosc/32
1	1	3	9-bit UART	Variable

Timers/counters

The IS80C52 contains two 16-bit counters for measuring time intervals, measuring pulse widths, counting events and generating precise, periodic interrupt request.

The operating mode is listed below.

Timer 1/Counter 1:
Timer 1/Counter 1 can be configured in one of four modes:

Mode 0: Provides an 8-bit counter with a divide-by-32 prescaler or an 8-bit timer with a divide-by-32 prescaler. A read/write of TH1 accesses counter 1's bits 12-5. A read/write of TL1 accesses counter 1's bits 7-0. TL1 bits 4-0 are the prescaler (counter 1's 4-0) while bits 7-5 are indeterminate and should be ignored. The programmer should clear the prescaler (counter 1's bits 4-0) before setting the run flag.

Mode 1: Configures counter 1 as a 16-bit timer/counter.

Mode 2: Configures counter 1 as an 8-bit auto-reload value. TH1 holds the reload value. TL1 is incremented. The value in TH1 is reload onto TL1 when TL1 overflows from all ones.

Mode 3: When counter 1's mode is repro-grammed to mode 3 (from mode 0, 1 or 2), it disables the incrementing of the counter. This mode is provided as an alternative to use TR1 bit (TCON.6) to start and stop counter 1.

The serial port receives a pulse each time that counter 1 overflows. The standard UART mode divides this pulse rate to generate the transmission rate.

Counter 0/ Timer 0:
Counter 0 can also be configured in one of four modes:

Mode 0-2: Mode 0-2 are the same as for counter 1.

Mode 3: In mode 3, the configure of TH0 is not affected by the bits in TMOD or TCON. It is configured solely as an 8-bit timer that is enabled for incrementing by TCON's TR1 bit. Upon TH0's overflow the TF1 flag gets set. Thus, neither TR1 nor TF1 is available to counter 1 when counter 0 is in mode 3. The function of TR1 can be done by placing counter 1 in mode 3, so only the function of TF1 is actually given up by counter 1. In mode 3, TL0 is configured as an 8-bit timer/counter and is controlled, as usual, by the GATE (TMOD. 3), C/ (TMOD.2), TR0 (TCON.4) and TF0 (TCON.5) control bits.

The use of the timers/counters is determined by two 8-bit registers, TMOD and TCON is shown in SFR. The counter input circuit is shown in Figures 6 and 7.

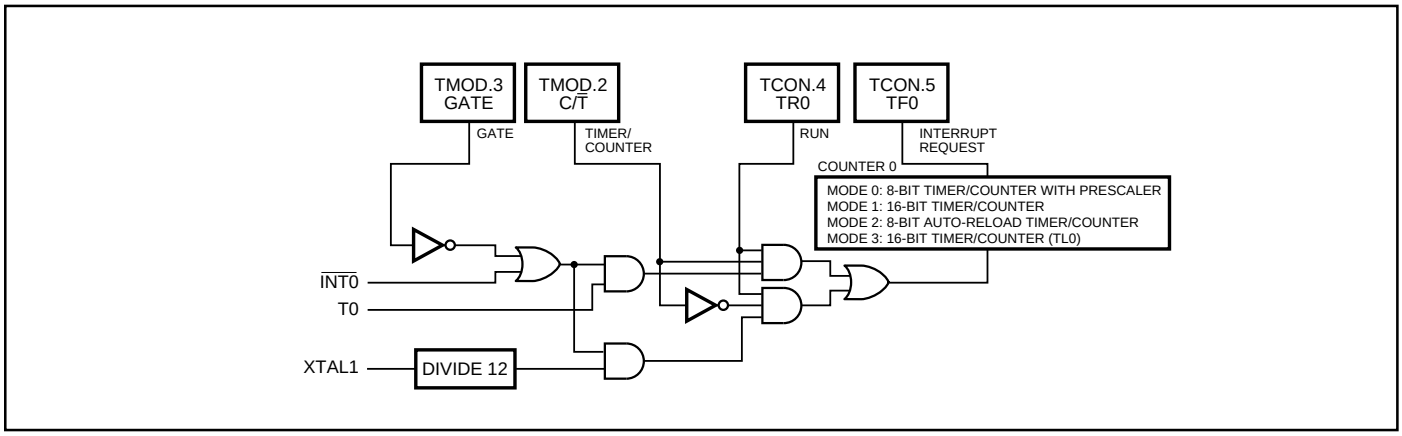

Figure 6. Timer/event Counter 0 Control and Status Flag Circiut

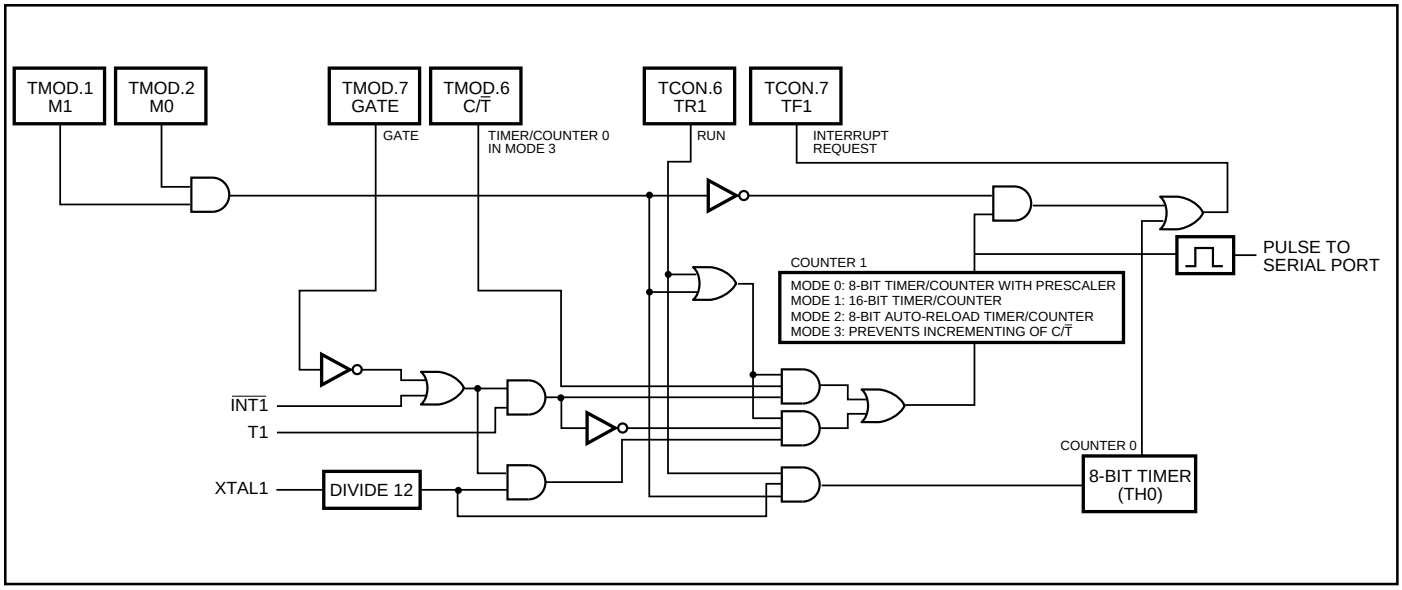

Figure 7. Timer/event Counter 1 Control and Status Flag Circiut

Serial Interface

The IS80C52 has a serial I/O port that is useful for serial linking peripheral devices as well as multiple IS80C52s through standard asynchronous protocol with full-duplex operations. The data for transmission to and from reception reside in the serial port buffer register (SBUF). The serial port control and the monitoring of its status is provided by the serial port control register (SCON). The contents of the 8-bit SCON register are shown in SFR.

The IS80C52 has a serial channel useful for serially linking UART (universal asynchronous receiver/ transmitter) devices and for expanding I/O. The full-duplex serial I/O port can be programmed to function in one of four operating modes:

Mode 0: Synchronous I/O expansion using TTL or CMOS shift registers.
Mode 1: UART interface with 10-bit frame and variable transmission rate.
Mode 2: UART interface with 11-bit frame and fixed transmission rate.
Mode 3: UART interface with 11-bit frame and variable transmission rate.

The serial interface circuit is shown in Figures 8 and 9. The use of the serial interface is determined by TCON and PCON registers is shown in SFR.

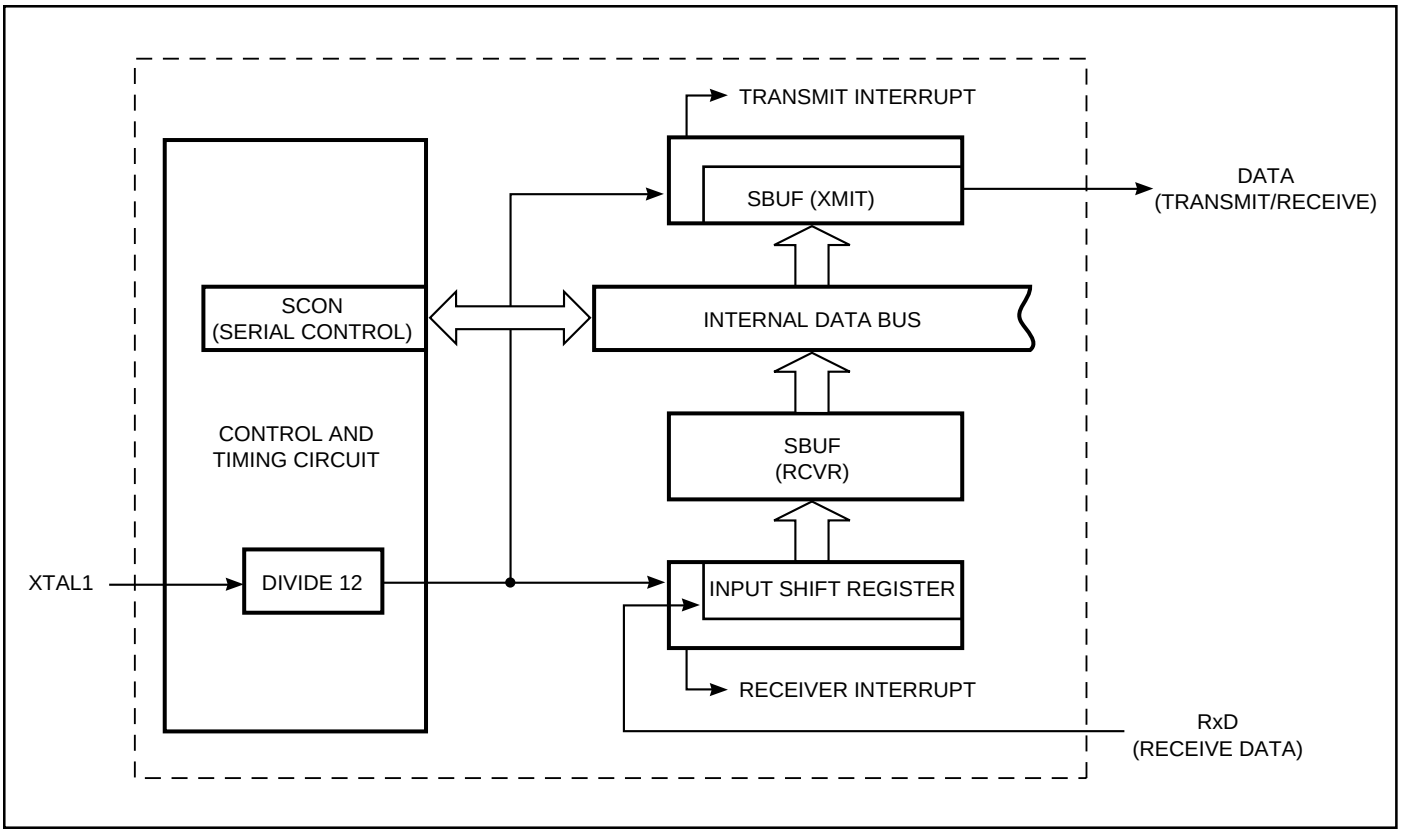

Figure 8. Serial Port: Synchronous Mode 0

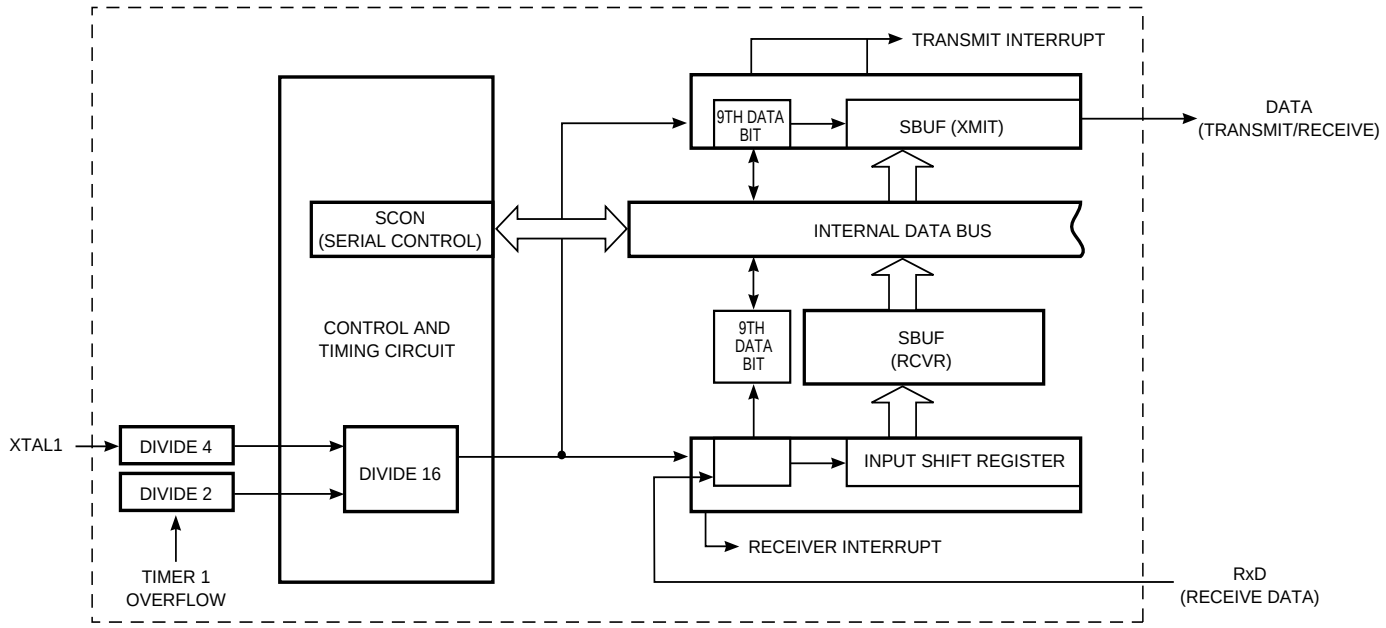

Figure 9. Serial Port: UART Mode 1, 2, and 3

Interrupt System

External events and the real-time driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two-priority-level, nested interrupt system is provided. The interrupt system is shown in Figure 10. The interrupt request flag and program memory location of interrupt service program is shown in the table below:

Interrupt Source	Request Flag	Bit Location	Start Address
External Request 0	IE0	TCON.1	3 (0003H)
Internal Timer 0/Counter 0	TF0	TCON.5	11 (000BH)
External Request 1	IE1	TCON.3	19 (0013H)
Internal Timer 1/Counter 1	TF1	TCON.7	27 (001BH)
Internal Serial Port (XMIT)	TI	SCON.1	35 (0023H)
Internal Serial Port (RCVR)	RI	SCON.0	35 (0023H)

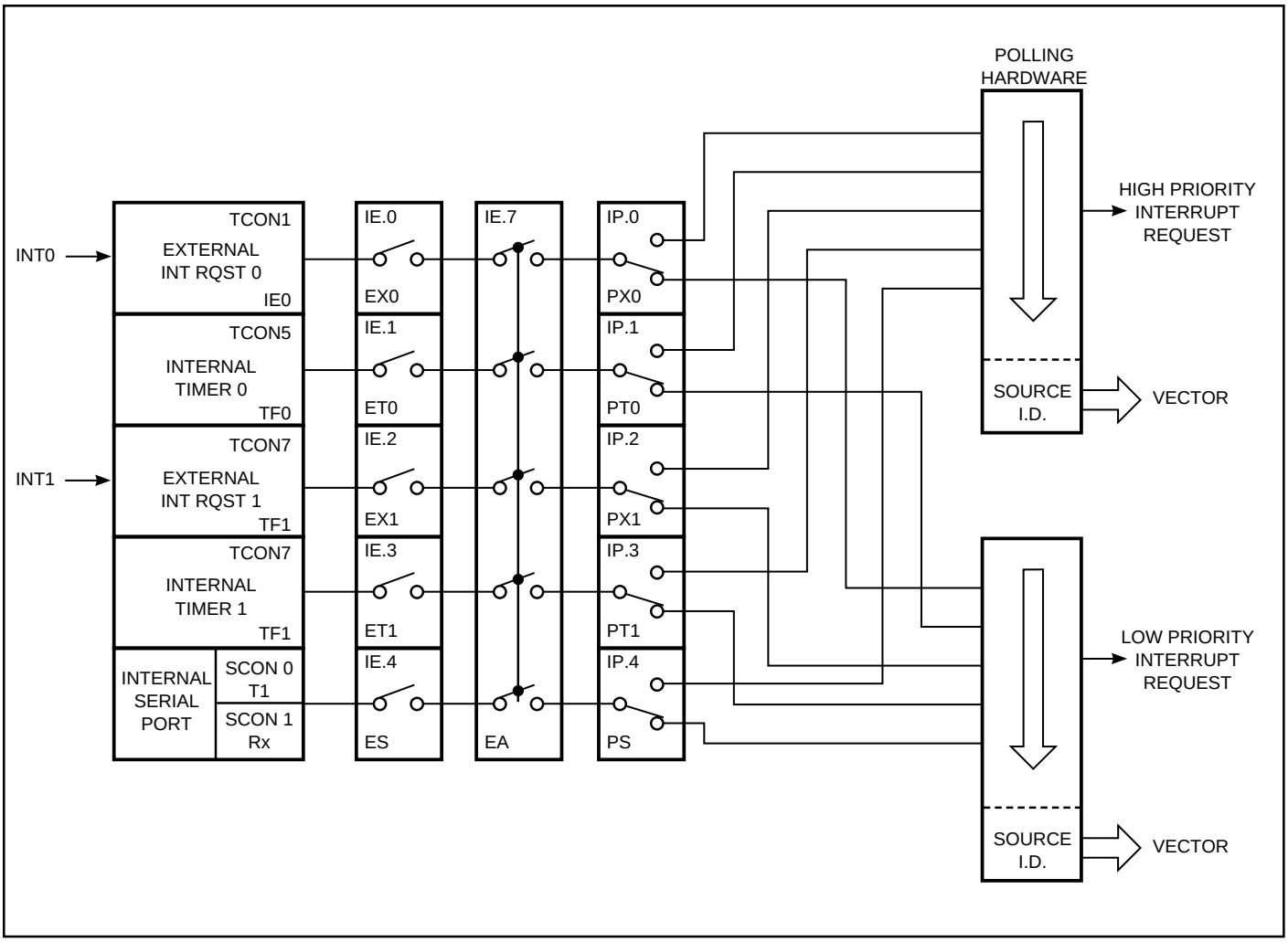

Figure 10. Interrupt System

ADDITIONAL INFORMATION

Idle mode

In idle mode, the CPU puts itself to sleep while all the on-chip perpherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the Special Function Register remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program exection, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle is terminated by reset, the instruction following the one that invokes idle should not be one that writes to a port pin or to external memory. The status of external pins is shown in the following table.

Power-down mode

In the power-down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and special function register retain their values until the power down mode is terminated.

The only exit from power-down mode is a hardware reset. Reset redefines the SFR but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize. The status of the external pins during idle and power-down mode is shown in the following table.

Status of the External Pins during Idle and Power-down modes.

Mode	Memory	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ROM Verification

The address of the program memory location to be read is applied to Port 1 and pins P2.3-P2.0. The other pins should be held at the “Verify” level are indicated in Figure 11. The contents of the addressed locations exits on Port 0. External pullups are required on Port 0 for this operation. Figure 11 shows the setup to verify the program memory.

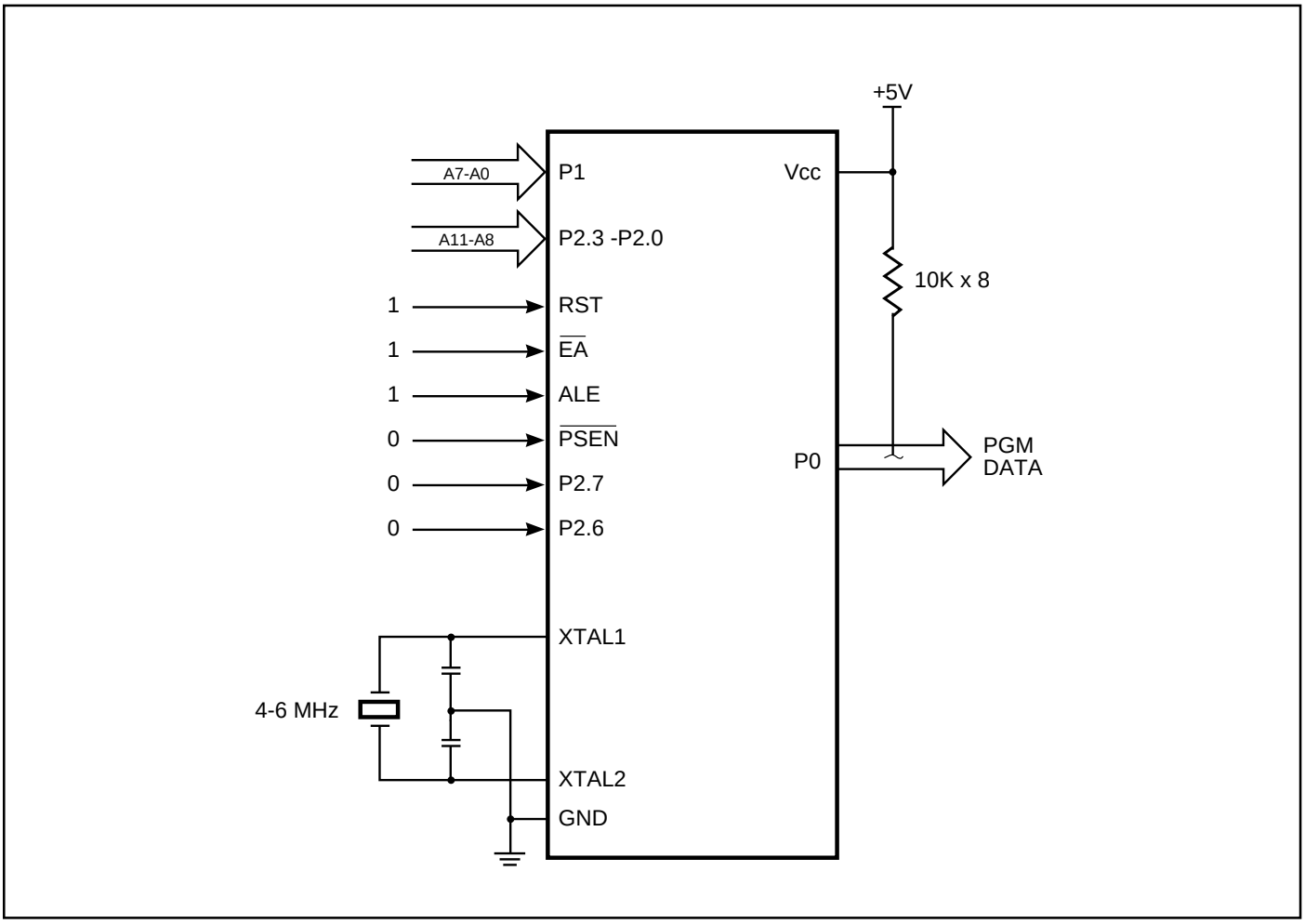

Figure 11. ROM Verification

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND(2)	–2.0 to +7.0	V
T_{BIAS}	Temperature Under Bias(3)	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +125	°C
P_T	Power Dissipation	1.5	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods less than 20 ns. Maximum DC voltage on output pins is Vcc + 0.5V which may overshoot to Vcc + 2.0V for periods less than 20 ns.
3. Operating temperature is for commercial products only defined by this specification.

OPERATING RANGE(1)

Range	Ambient Temperature	V_{CC}	Oscillator Frequency
Commercial	0°C to +70°C	5V ± 10%	3.5 to 24 MHz

Note:
1. Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(T_A = 0°C to 70°C; Vcc = 5V ± 10%; GND = 0V)

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{IL}	Input low voltage		–0.5	0.2Vcc – 0.1	V
V_{IL1}	Input low voltage		–0.5	0.2Vcc – 0.3	V
V_{IH}	Input high voltage (All except XTAL 1, RST)		0.2Vcc + 0.9	Vcc + 0.5	V
V_{IH1}	Input high voltage (XTAL 1)		0.7Vcc	Vcc + 0.5	V
V_{SCH}+	RST positive schmitt-trigger threshold voltage		0.7Vcc	Vcc + 0.5	V
V_{SCH}–	RST negative schmitt-trigger threshold voltage		0	0.3Vcc	V
V_{OL}(1)	Output low voltage (Ports 1, 2, and 3)	I_{OL} = 100 µA	—	0.3	V
		I_{OL} = 1.6 mA	—	0.45	V
		I_{OL} = 3.5 mA	—	1.0	V
V_{OL1}(1)	Output low voltage (Port 0, ALE, PSEN)	I_{OL} = 200 µA	—	0.3	V
		I_{OL} = 3.2 mA	—	0.45	V
		I_{OL} = 7.0 mA	—	1.0	V
V_{OH}	Output high voltage (Port 1, 2, 3, ALE, PSEN)	I_{OH} = –10 µA Vcc = 4.5V-5.5V	0.9Vcc	—	V
		I_{OL} = –25 µA	0.75Vcc	—	V
		I_{OL} = –60 µA	2.4	—	V
V_{OH1}	Output high voltage (Port 0, ALE, PSEN)	I_{OH} = –80 µA Vcc = 4.5V-5.5V	0.9Vcc	—	V
		I_{OH} = –300 µA	0.75Vcc	—	V
		I_{OH} = –800 µA	2.4	—	V
I_{IL}	Logical 0 input current (Port 1, 2, 3)	V_{IN} = 0.45V	—	–50	µA
I_{LI}	Input leakage current (Port 0)	0.45V < V_{IN} < Vcc	–10	+10	µA
I_{TL}	Logical 1-to-0 transition current (Port 1, 2, 3)	V_{IN} = 2.0V	—	–650	µA
RRST	RST pulldown resister		50	300	Kohm

Note:

1. Under steady state (non-transient) conditions, Iol must be externally limited as follows:
   Maximum I_{OL} per port pin: ..... 10 mA
   Maximum I_{OL} per 8-bit port
   Port 0: ..... 26 mA
   Port 1, 2, 3: ..... 15 mA
   Maximum total I_{OL} for all output pins: .... 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink greater than the listed test conditions.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Max	Unit
Icc	Power supply current[1]				
	Active mode	12 MHz	—	20	mA
		16 MHz	—	26	mA
		20 MHz	—	32	mA
		24 MHz	—	38	mA
		32 MHz	—	50	mA
		40 MHz	—	62	mA
	Idle mode	12 MHz	—	5	mA
		16 MHz	—	6	mA
		20 MHz	—	7.6	mA
		24 MHz	—	9	mA
		32 MHz	—	12	mA
		40 MHz	—	15	mA
	Power-down mode		—	50	µA

Note:
1. See Figures 12, 13, 14, and 15 for Icc test conditiions.

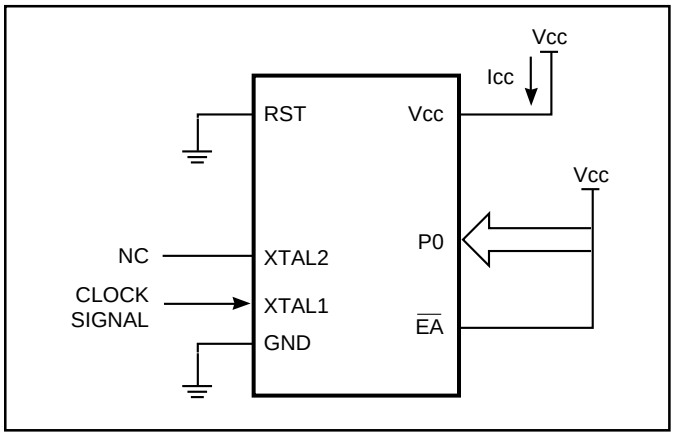

Figure 12. Active Mode

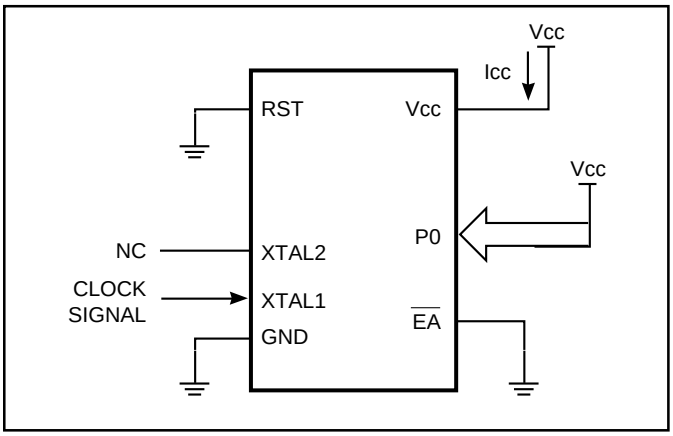

Figure 13. Idle Mode

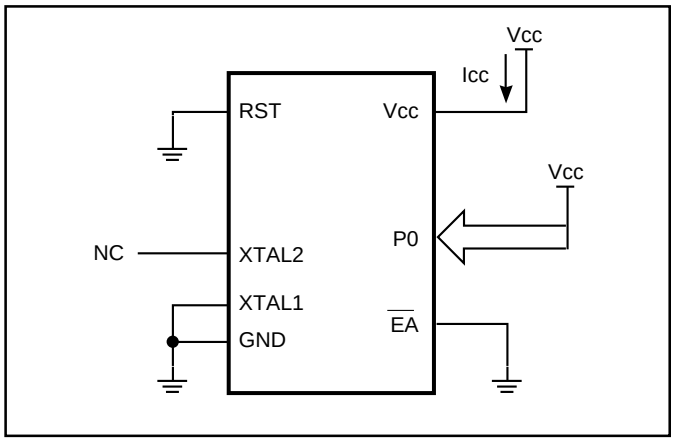

Figure 14. Power-down Mode

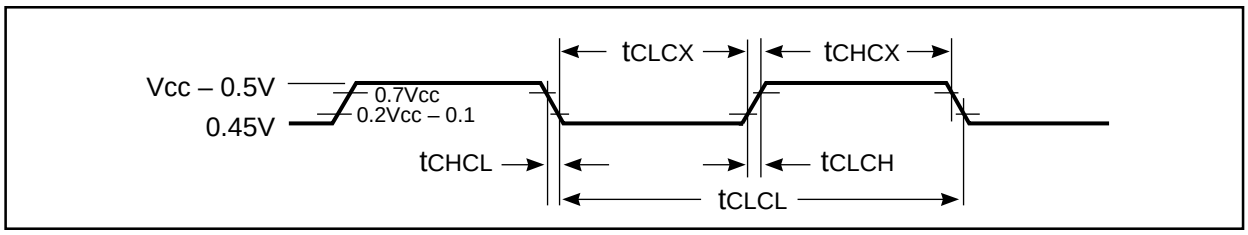

Figure 15. Icc Test Conditions

Clock signal waveform for Icc tests in active and idle mode ($t_{CLCH} = t_{CHCL} = 5$ ns)

AC CHARACTERISTICS

(T_A = 0°C to 70°C; Vcc = 5V ± 10%; GND = 0V; C_L for Port 0, ALE and $\overline{PSEN}$; Outputs = 100 pF; C_L for other outputs = 80 pF)

External Memory Characteristics

		24 MHz Clock		40 MHz Clock		Variable Oscillator		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$1/t_{CLCL}$	Oscillator frequency	—	—	—	—	3.5	40	MHz
t_{LHLL}	ALE pulse width	43	—	10	—	$2t_{CLCL}$–40	—	ns
t_{AVLL}	Address valid to ALE low	2	—	–15	—	t_{CLCL}–40	—	ns
t_{LLAX}	Address hold after ALE low	7	—	–10	—	t_{CLCL}–35	—	ns
t_{LLIV}	ALE low to valid instr in	—	105	—	55	—	$3t_{CLCL}$–20	ns
t_{LLPL}	ALE low to $\overline{PSEN}$ low	2	—	–15	—	t_{CLCL}–40	—	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	80	—	30	—	$3t_{CLCL}$–45	—	ns
t_{PLIV}	$\overline{PSEN}$ low to valid instr in	—	73	—	40	—	$2t_{CLCL}$–10	ns
t_{PXIX}	Input instr hold after $\overline{PSEN}$	0	—	0—	—	0	—	ns
t_{PXIZ}	Input instr float after $\overline{PSEN}$	—	73	—	40	—	$2t_{CLCL}$–10	ns
t_{AVIV}	Address to valid instr in	—	147	—	80	—	$4t_{CLCL}$–20	ns
t_{PLAZ}	$\overline{PSEN}$ low to address float	—	10	—	10	—	10	ns
t_{RLRH}	$\overline{RD}$ pulse width	150	—	50	—	$6t_{CLCL}$–100	—	ns
t_{WLWH}	$\overline{WR}$ pulse width	150	—	50	—	$6t_{CLCL}$–100	—	ns
t_{RLDV}	$\overline{RD}$ low to valid data in	—	114	—	30	—	$5t_{CLCL}$–95	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	—	0	—	0	—	ns
t_{RHDZ}	Data float after $\overline{RD}$	—	63	—	30	—	$2t_{CLCL}$–70	ns
t_{LLDV}	ALE low to valid data in	—	244	—	110	—	$8t_{CLCL}$–90	ns
t_{AVDV}	Address to valid data in	—	285	—	135	—	$9t_{CLCL}$–90	ns
t_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ low	75	175	25	125	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ low	77	—	10	—	$4t_{CLCL}$–90	—	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	2	—	–1.5	—	t_{CLCL}–40	—	ns
t_{WHQX}	Data hold after $\overline{WR}$	2	—	–1.5	—	t_{CLCL}–40	—	ns
t_{QVWH}	Data valid to $\overline{WR}$ high	219	—	105	—	$7t_{CLCL}$–70	—	ns
t_{RLAZ}	$\overline{RD}$ low to address float	—	63	—	30	—	$2t_{CLCL}$–20	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ high to ALE high	2	82	–15	65	t_{CLCL}–40	t_{CLCL}+40	ns

Serial Port Timing: Shift Register Mode

Symbol	Parameter	24 MHz Clock Min	24 MHz Clock Max	40 MHz Clock Min	40 MHz Clock Max	Variable Oscillator Min	Variable Oscillator Max	Unit
t_{XLXL}	Serial port clock cycle time	500	—	—	—	$12t_{CLCL}$	—	ns
t_{QVXH}	Output data setup to clock rising edge	284	—	117	—	$10t_{CLCL}$–133	—	ns
t_{XHQX}	Output data hold after clock rising edge	33	—	0	—	$2t_{CLCL}$–50	—	ns
t_{XHDX}	Input data hold after clock rising edge	0	—	0	—	0	—	ns
t_{XHDV}	Clock rising edge to input data valid	—	284	—	117	—	$10t_{CLCL}$–133	ns

External Clock Drive

Symbol	Parameter	Min	Max	Unit
$1/t_{CLCL}$	Oscillator Frequency	3.5	24	MHz
t_{CHCX}	High time	10	—	ns
t_{CLCX}	Low time	10	—	ns
t_{CLCH}	Rise time	—	10	ns
t_{CHCL}	Fall time	—	10	ns

ROM Verification Characteristics

Symbol	Parameter	Min	Max	Unit
$1/t_{CLCL}$	Oscillator Frequency	2.5	40	MHz
t_{AVQV}	Address to data valid	—	$48t_{CLCL}$	
t_{ELQV}	ENABLE low to data valid	—	$48t_{CLCL}$	
t_{EHQZ}	Data float after ENABLE	0	$48t_{CLCL}$	

TIMING WAVEFORMS

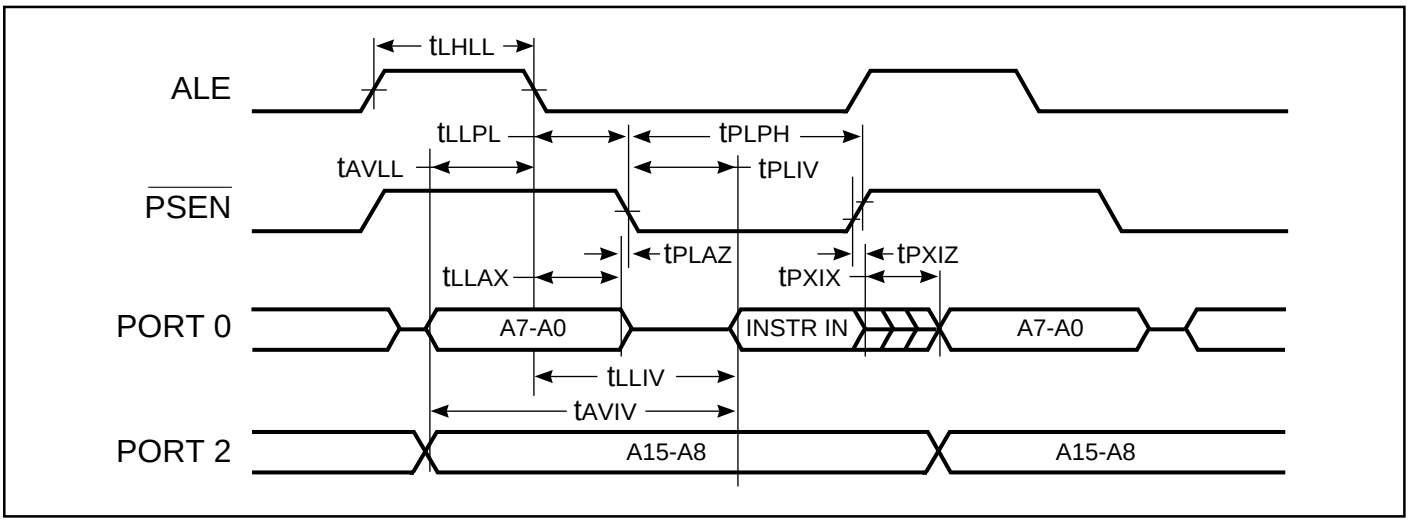

Figure 16. External Program Memory Read Cycle

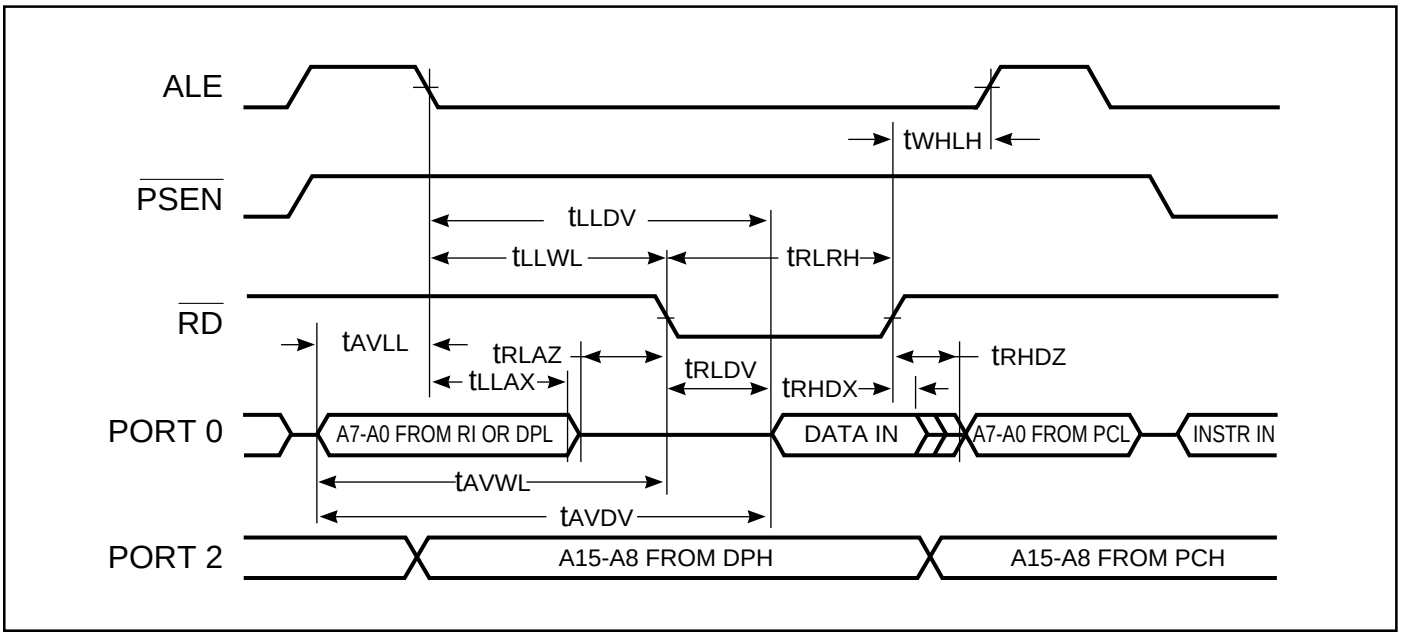

Figure 17. External Data Memory Read Cycle

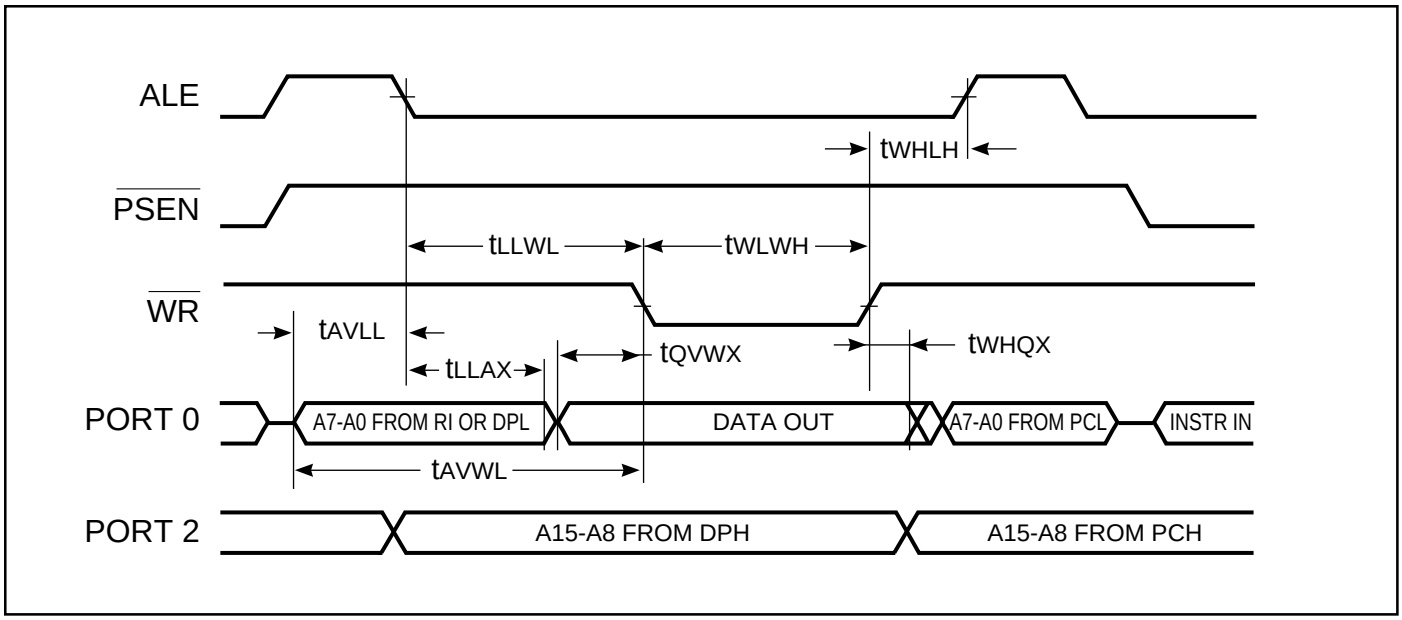

Figure 18. External Data Memory Write Cycle

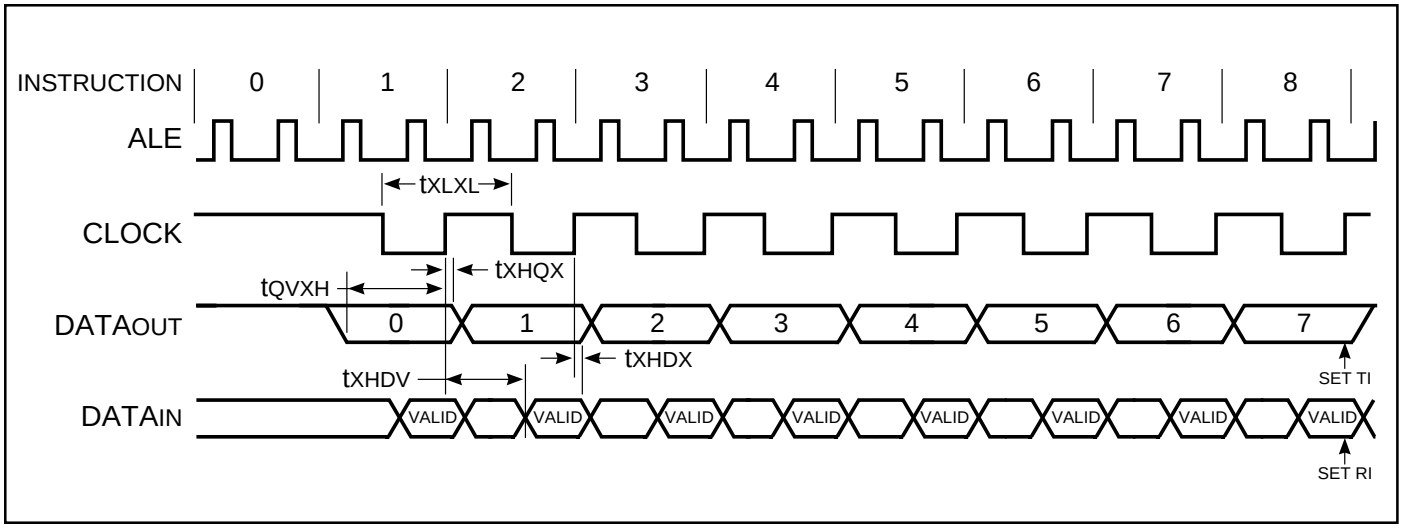

Figure 19. Shift Register Mode Timing Waveforms

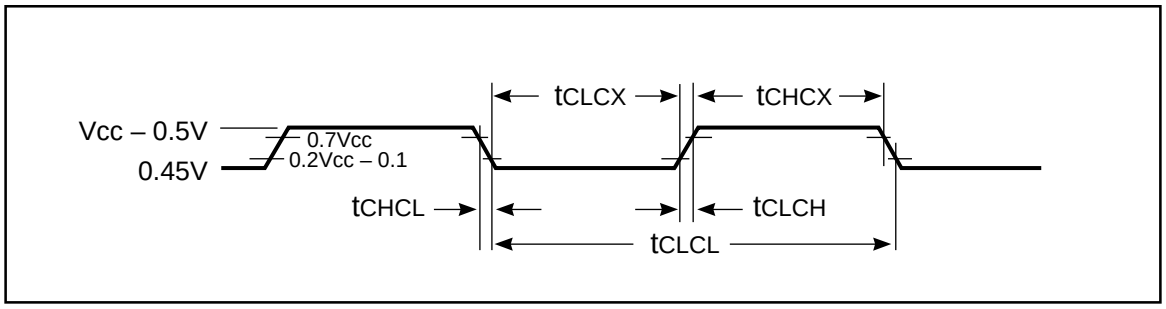

Figure 20. External Clock Drive Waveform

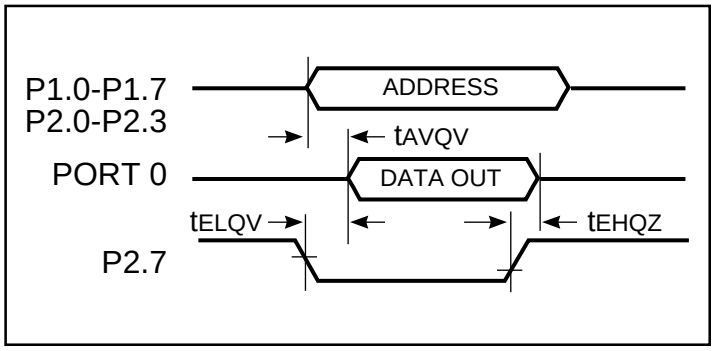

Figure 21. ROM Verification Waveforms

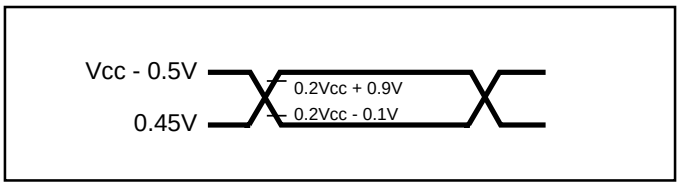

Figure 22. AC Test Point

Note:

1. AC inputs during testing are driven at VCC – 0.5V for logic "1" and 0.45V for logic "0". Timing measurements are made at V_{IH} min for logic "1" and max for logic "0".

ORDERING INFORMATION

Speed	Order Part Number	Package
12 MHz	IS80C52-12PL	PLCC – Plastic Leaded Chip Carrier
	IS80C52-12PQ	PQFP - Plastic Qual Flat Pack
	IS80C52-12W	600-mil Plastic DIP
20 MHz	IS80C52-20PL	PLCC – Plastic Leaded Chip Carrier
	IS80C52-20PQ	PQFP - Plastic Qual Flat Pack
	IS80C52-20W	600-mil Plastic DIP
24 MHz	IS80C52-24PL	PLCC – Plastic Leaded Chip Carrier
	IS80C52-24PQ	PQFP - Plastic Qual Flat Pack
	IS80C52-24W	600-mil Plastic DIP
40 MHz	IS80C52-40PL	PLCC – Plastic Leaded Chip Carrier
	IS80C52-40PQ	PQFP - Plastic Qual Flat Pack
	IS80C52-40W	600-mil Plastic DIP
12 MHz	IS80C32-12PL	PLCC – Plastic Leaded Chip Carrier
	IS80C32-12PQ	PQFP - Plastic Qual Flat Pack
	IS80C32-12W	600-mil Plastic DIP
20 MHz	IS80C32-20PL	PLCC – Plastic Leaded Chip Carrier
	IS80C32-20PQ	PQFP - Plastic Qual Flat Pack
	IS80C32-20W	600-mil Plastic DIP
24 MHz	IS80C32-24PL	PLCC – Plastic Leaded Chip Carrier
	IS80C32-24PQ	PQFP - Plastic Qual Flat Pack
	IS80C32-24W	600-mil Plastic DIP
40 MHz	IS80C32-40PL	PLCC – Plastic Leaded Chip Carrier
	IS80C32-40PQ	PQFP - Plastic Qual Flat Pack
	IS80C32-40W	600-mil Plastic DIP

Integrated Silicon Solution, Inc.
2231 Lawson Lane
Santa Clara, CA 95054
Fax: (408) 588-0806
Toll Free: 1-800-379-4774
http://www.issiusa.com