



74VHCT245A

OCTAL BUS TRANSCEIVER (3-STATE)

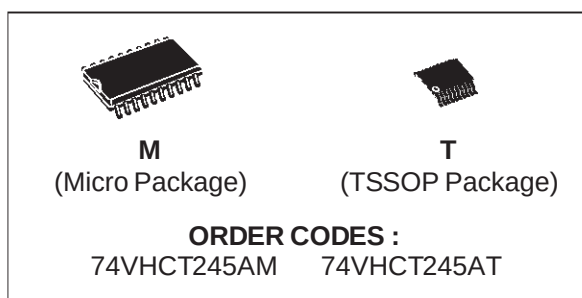
PRELIMINARY DATA

- HIGH SPEED: $t_{PD} = 4.5 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS:
 $V_{IH} = 2V$ (MIN), $V_{IL} = 0.8V$ (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 245
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.9V$ (Max.)

DESCRIPTION

The 74VHCT245A is an advanced high-speed CMOS OCTAL BUS TRANSCEIVER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^2 MOS technology. It has similar high speed performance of equivalent Bipolar Schottky TTL combined with true CMOS low power dissipation.

This IC is intended for two-way asynchronous

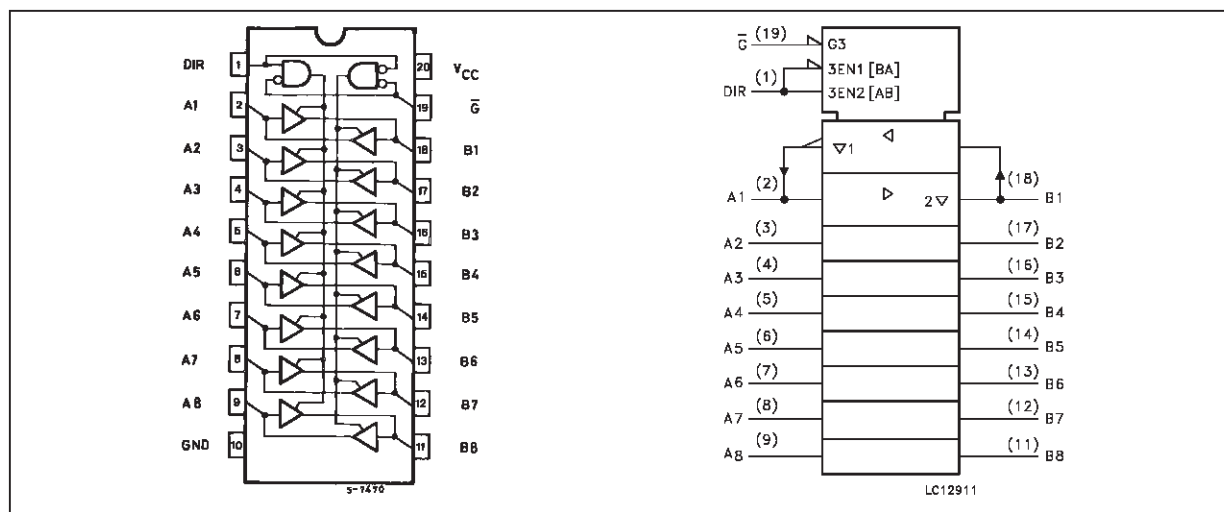


communication between data busses; the direction of data transmission is determined by the level of the DIR input. The enable input $\bar{G}$ can be used to disable the device so that the busses are effectively isolated.

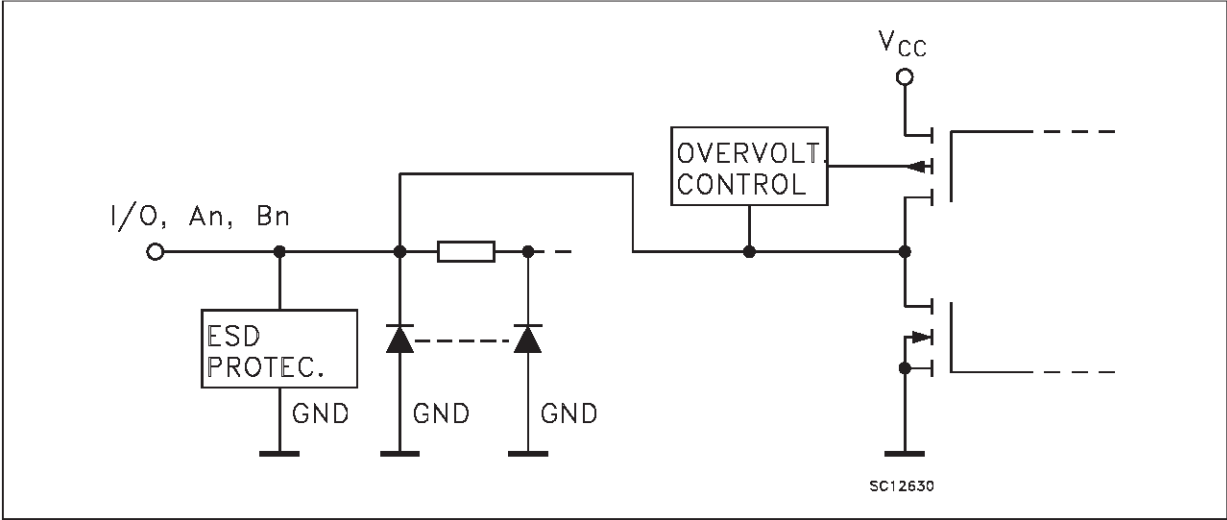
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

IT IS PROHIBITED TO APPLY A SIGNAL TO A TERMINAL WHEN IT IS IN OUTPUT MODE AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE) IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

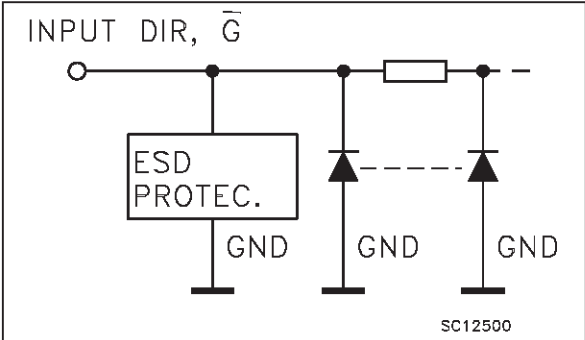
PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT/OUTPUT EQUIVALENT CIRCUIT



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	DIR	Directional Control
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
18, 17, 16, 15, 14, 13, 12, 11	B1 to B8	Data Inputs/Outputs
19	$\overline{G}$	Output Enable Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X: "H" or "L"
Z: High impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage (DIR, $\overline{G}$)	-0.5 to +7.0	V
$V_{I/O}$	DC Bus I/O Voltage (see note 1)	-0.5 to +7.0	V
$V_{I/O}$	DC Bus I/O Voltage (see note 2)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 75	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (10 sec)	300	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) Output in Off State

2) High or Low State. I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage (DIR, $\overline{G}$)	0 to 5.5	V
$V_{I/O}$	Bus I/O Voltage (see note 1)	0 to 5.5	V
$V_{I/O}$	Bus I/O Voltage (see note 2)	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	$^{\circ}\text{C}$
dt/dv	Input Rise and Fall Time (see note 3) ($V_{CC} = 5.0 \pm 0.5\text{V}$)	0 to 20	ns/V

1) $V_{CC} = 0\text{V}$

2) Output in Off State

3) High or Low State. I_{OUT} absolute maximum rating must be observed.

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V _{CC} (V)			T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	4.5 to 5.5			2			2		V
V _{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8	V
V _{OH}	High Level Output Voltage	4.5	V _I ^(*) = V _{IH} or V _{IL}	I _O =-50 μA	4.4	4.5		4.4		V
		4.5		I _O =-8 mA	3.94			3.8		
V _{OL}	Low Level Output Voltage	4.5	V _I ^(*) = V _{IH} or V _{IL}	I _O =50 μA		0.0	0.1		0.1	V
		4.5		I _O =8 mA			0.36		0.44	
I _{OZ}	3 State Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = 0V to 5.5V				±0.25		±2.5	μA
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND				±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND				2		20	μA
ΔI _{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V _{CC} or GND				1.35		1.5	mA
I _{OPD}	Output Leakage Current	0	V _{OUT} = 5.5V				0.5		5.0	μA

(*) All outputs loaded

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3 ns)

Symbol	Parameter	Test Condition			Value					Unit
		V _{CC} (*) (V)	C _L (pF)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	5.0	15		4.5	7.5	1.0	8.5	ns	
		5.0	50		5.5	8.5	1.0	9.5		
t _{PZL} t _{PZH}	Output Enable Time	5.0	15	R _L = 1KΩ	9.0	14.5	1.0	15.5	ns	
		5.0	50		10.0	15.5	1.0	16.5		
t _{PZL} t _{PZH}	Output Disable Time	5.0	50	R _L = 1KΩ	9.5	15.0	1.0	16.0	ns	
t _{OSLH} t _{OSHL}	Output to Output Skew Time (note 1)	5.0	50			1.0		1.0	ns	

(*) Voltage range is 5V ± 0.5V

Note 1: Parameter guaranteed by design. t_{SOZH} = |t_{PLHm} - t_{PLHn}|, t_{SOHL} = |t_{PHLm} - t_{PHLn}|

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T _A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance			4	10		10	pF
C _{I/O}	Bus Input Capacitance			8				pF
C _{PD}	Power Dissipation Capacitance (note 1)			13				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CD}/8$ (per circuit)

DYNAMIC SWITCHING CHARACTERISTICS

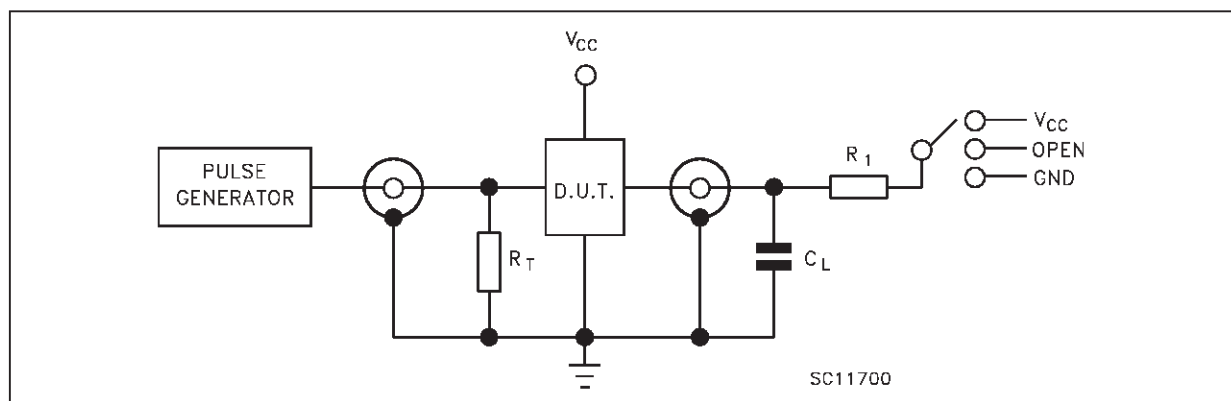
Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50 pF		0.6	0.9			V
V _{OLV}				-0.9	-0.6				
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		2					
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				0.8			

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.0V. Inputs under test switching: 3.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

TEST CIRCUIT



TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	V _{CC}
t _{PZH} , t _{PHZ}	GND

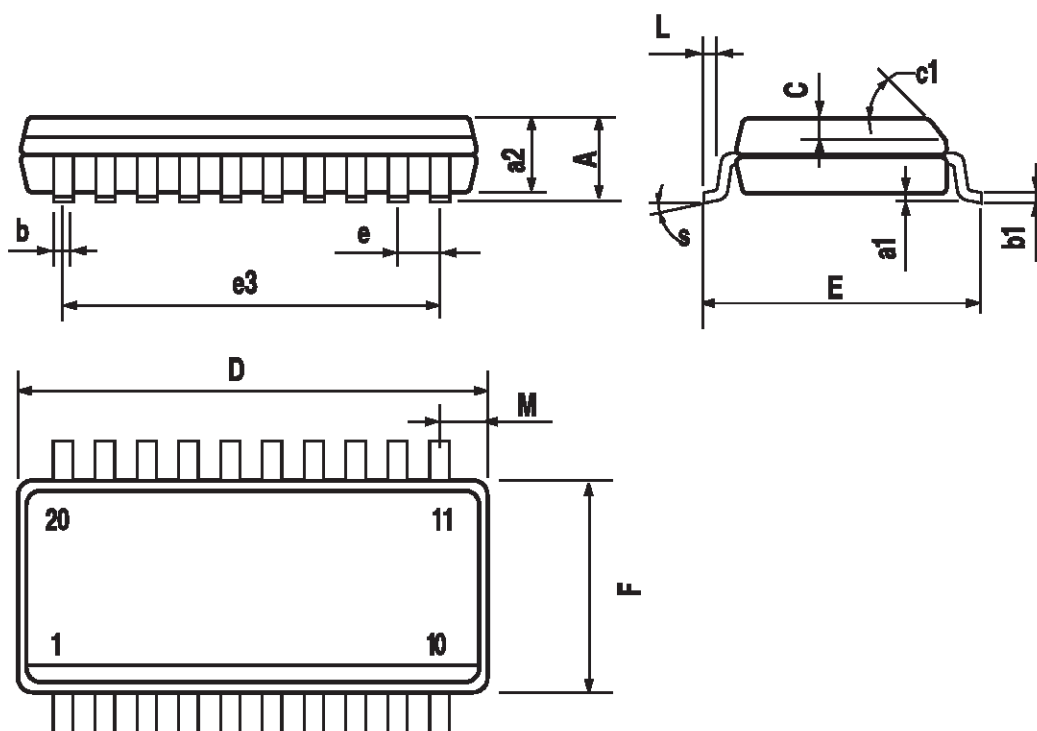
C_L = 15/50 pF or equivalent (includes jig and probe capacitance)

R_L = R₁ = 1KΩ or equivalent

R_T = Z_{OUT} of pulse generator (typically 50Ω)

SO-20 MECHANICAL DATA

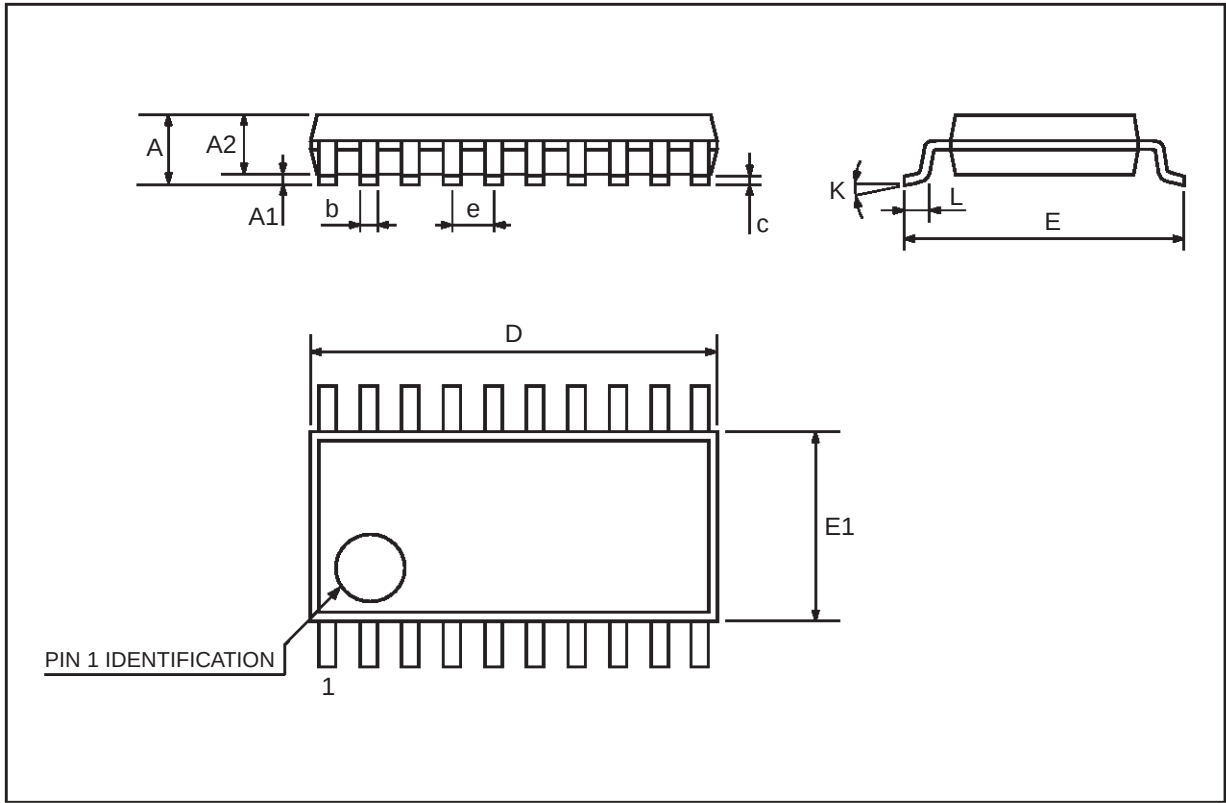
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1998 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands -
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.