

DATA SHEET

74LVC16373A/74LVCH16373A

**16-bit D-type transparent latch with 5 Volt
tolerant inputs/outputs (3-State)**

Product specification
Supersedes data of 1997 Aug 22
IC24 Data Handbook

1998 Mar 17

16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

74LVC16373A/ 74LVCH16373A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16373A only)
- High impedance when $V_{CC} = 0$

DESCRIPTION

The 74LVC(H)16373A is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. One latch enable (LE) input and one output enable (OE) are provided for each octal. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)16373A consists of 2 sections of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When OE is LOW, the contents of the eight latches are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the latches.

The 74LVCH16373A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn LE to Qn	$C_L = 50\text{pF}$ $V_{CC} = 3.3\text{V}$	3.0 3.4	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	$V_{CC} = 3.3\text{V}$	26	pF

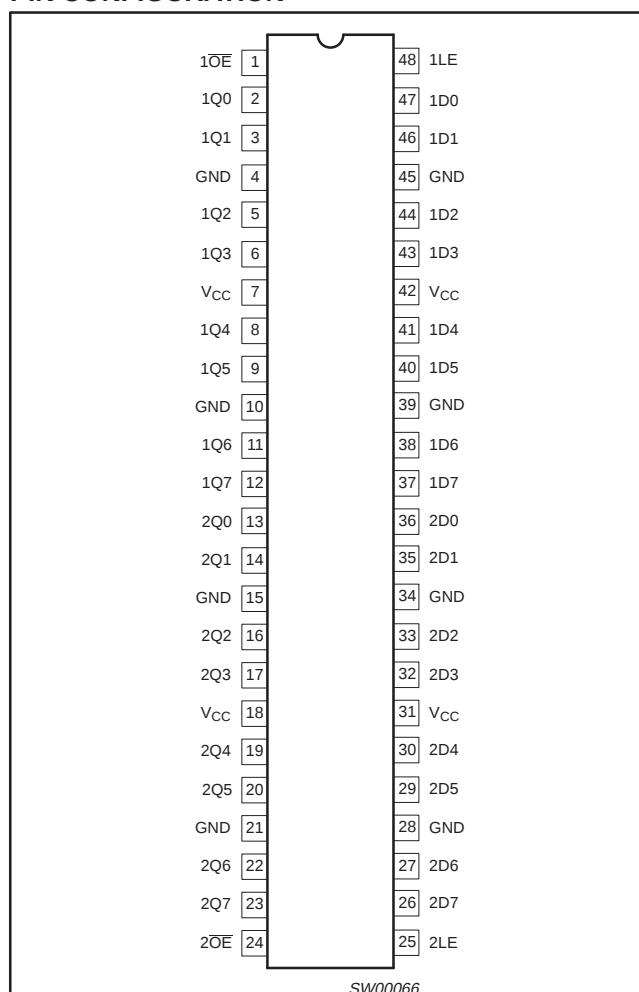
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74LVC16373A DL	VC16373A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74LVC16373A DGG	VC16373A DGG	SOT362-1
48-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74LVCH16373A DL	VCH16373A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74LVCH16373A DGG	VCH16373A DGG	SOT362-1

PIN CONFIGURATION



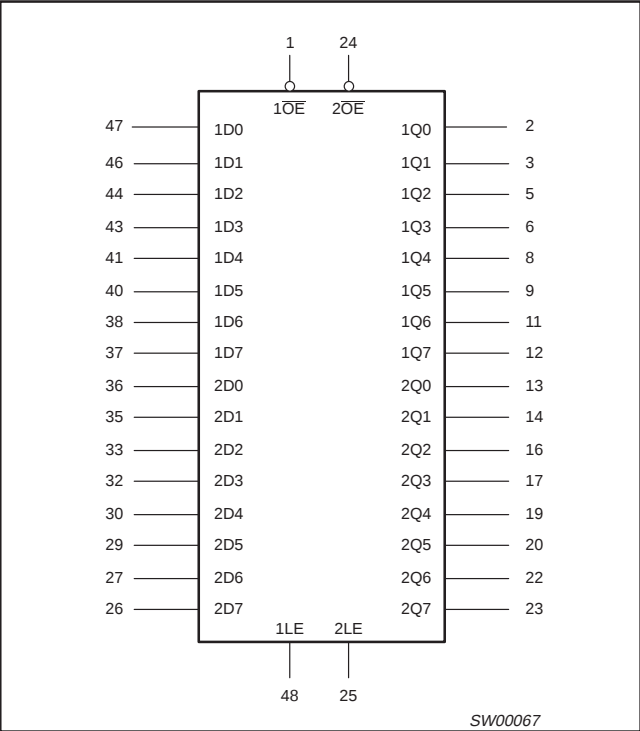
16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

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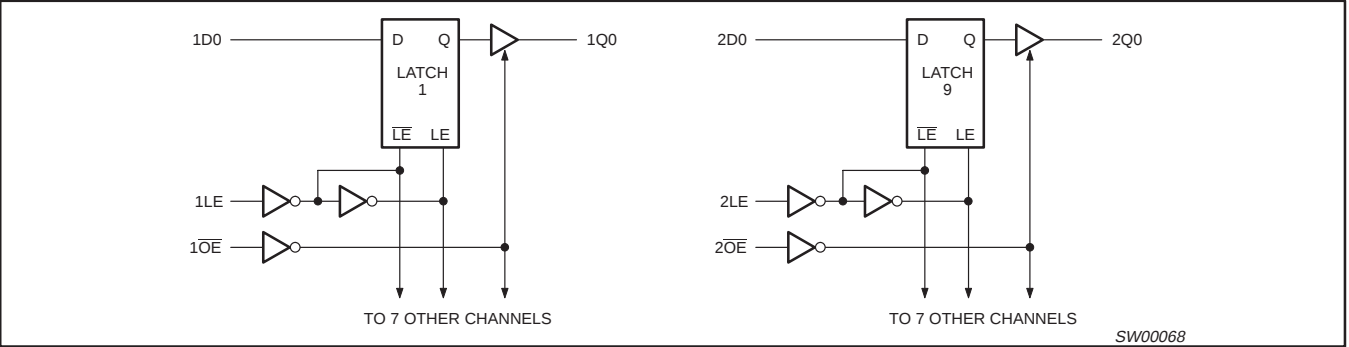
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1OE	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	Data inputs/outputs
24	2OE	Output enable input (active LOW)
25	2LE	Latch enable input (active HIGH)
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1LE	Latch enable input (active HIGH)

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE (per section of eight bits)

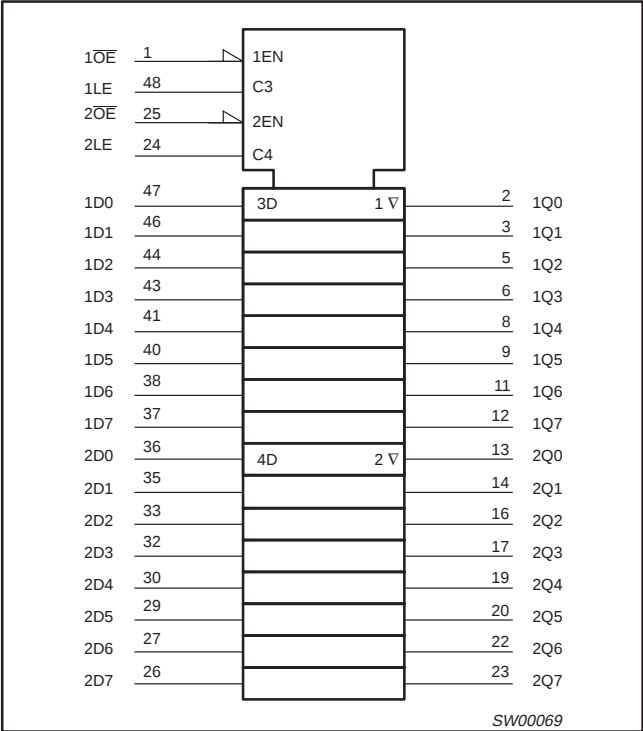
OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	OE	LE	Dn		Q0 to Q7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

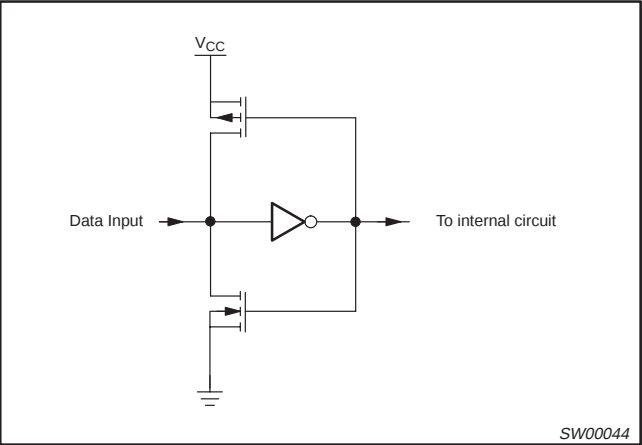
16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

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LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V _I	DC input voltage range		0	5.5	V
V _O	DC input voltage range; output HIGH or LOW state		0	V _{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _r , t _f	Input rise and fall times	V _{CC} = 1.2 to 2.7V	0	20	ns/V
		V _{CC} = 2.7 to 3.6V	0	10	

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ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	−0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package			mW
	– plastic mini-pack (SO)	above +70°C derate linearly with 8 mW/K	500	
	– plastic shrink mini-pack (SSOP and TSSOP)	above +60°C derate linearly with 5.5 mW/K	500	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = −12mA	V _{CC} − 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = −100μA	V _{CC} − 0.2	V _{CC}		V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = −18mA	V _{CC} − 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = −24mA	V _{CC} − 0.8			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA			0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND ⁶		± 0.1	± 5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND		0.1	± 5	μA
I _{off}	Power off leakage supply	V _{CC} = 0.0V; V _I or V _O = 5.5V			± 10	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	20	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} − 0.6V; I _O = 0		5	500	μA

16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

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DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
I _{BHL}	Bus hold LOW sustaining current	V _{CC} = 3.0V; V _I = 0.8V ^{2, 3, 4}	75			μA
I _{BHH}	Bus hold HIGH sustaining current	V _{CC} = 3.0V; V _I = 2.0V ^{2, 3, 4}	−75			μA
I _{BHLO}	Bus hold LOW overdrive current	V _{CC} = 3.6V ^{2, 3, 5}	500			μA
I _{BHHO}	Bus hold HIGH overdrive current	V _{CC} = 3.6V ^{2, 3, 5}	−500			μA

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$; $T_{amb} = -40^\circ C$ to $+85^\circ C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$	
			MIN	TYP ¹	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay Dn to Qn	1, 5	1.5	3.0	4.7	1.5	5.7	12	ns
t_{PHL} t_{PLH}	Propagation delay LE to Qn	2, 5	1.5	3.4	4.8	1.5	5.8	14	ns
t_{PZH} t_{PZL}	3-State output enable time OE to Qn	4, 5	1.5	3.5	5.5	1.5	6.5	18	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE to Qn	4, 5	1.5	3.9	5.4	1.5	6.4	11	ns
t_W	LE pulse width HIGH	2	3	2.0	—	3	—	—	ns
t_{su}	Set-up time Dn to LE	3	1.7	-0.1	—	1.7	—	—	ns
t_h	Hold time Dn to LE	3	1.2	0.1	—	1.2	—	—	ns

NOTE:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

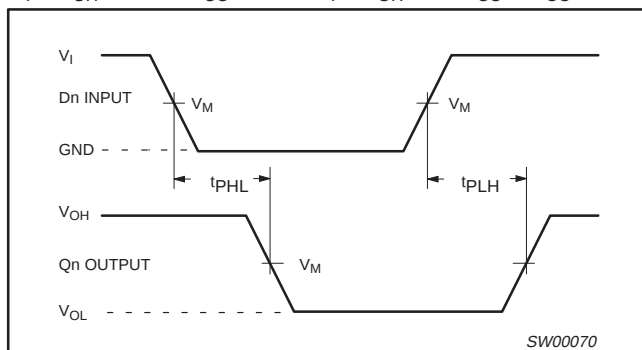
AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.

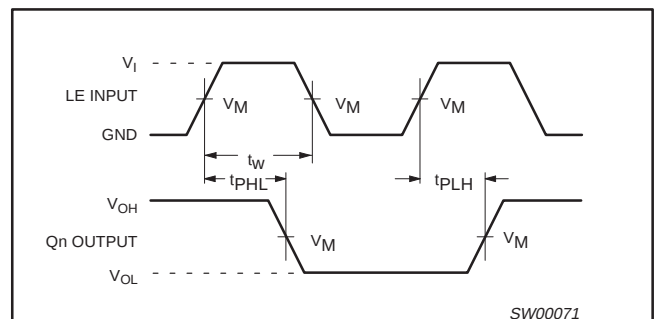
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$

$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$



Waveform 1. Input (Dn) to output (Qn) propagation delays



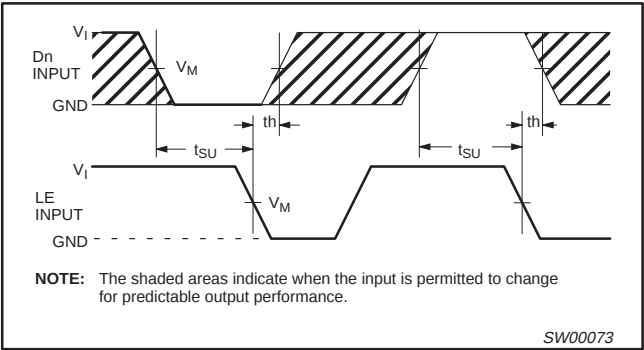
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays

16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

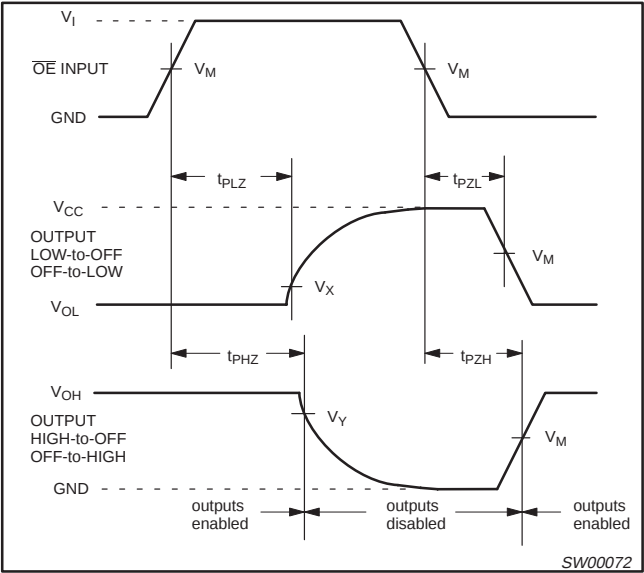
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AC WAVEFORMS (Continued)

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$

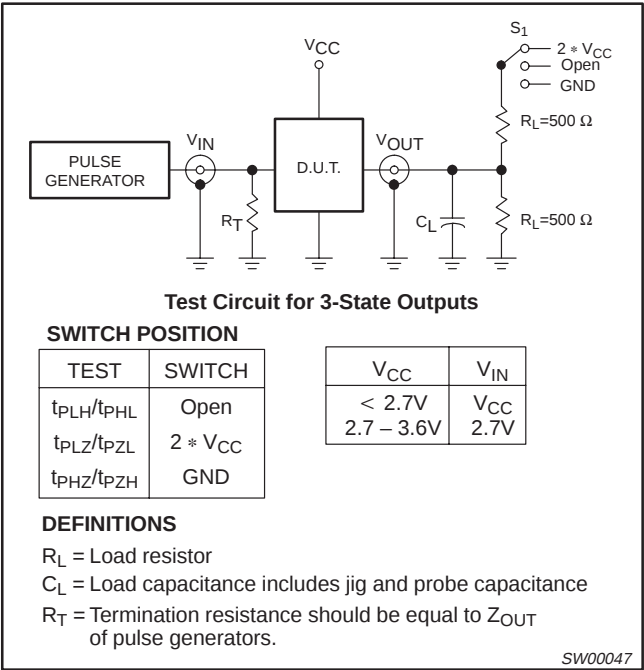


Waveform 3. Data set-up and hold times for the Dn input to the LE input



Waveform 4. 3-State enable and disable times

TEST CIRCUIT



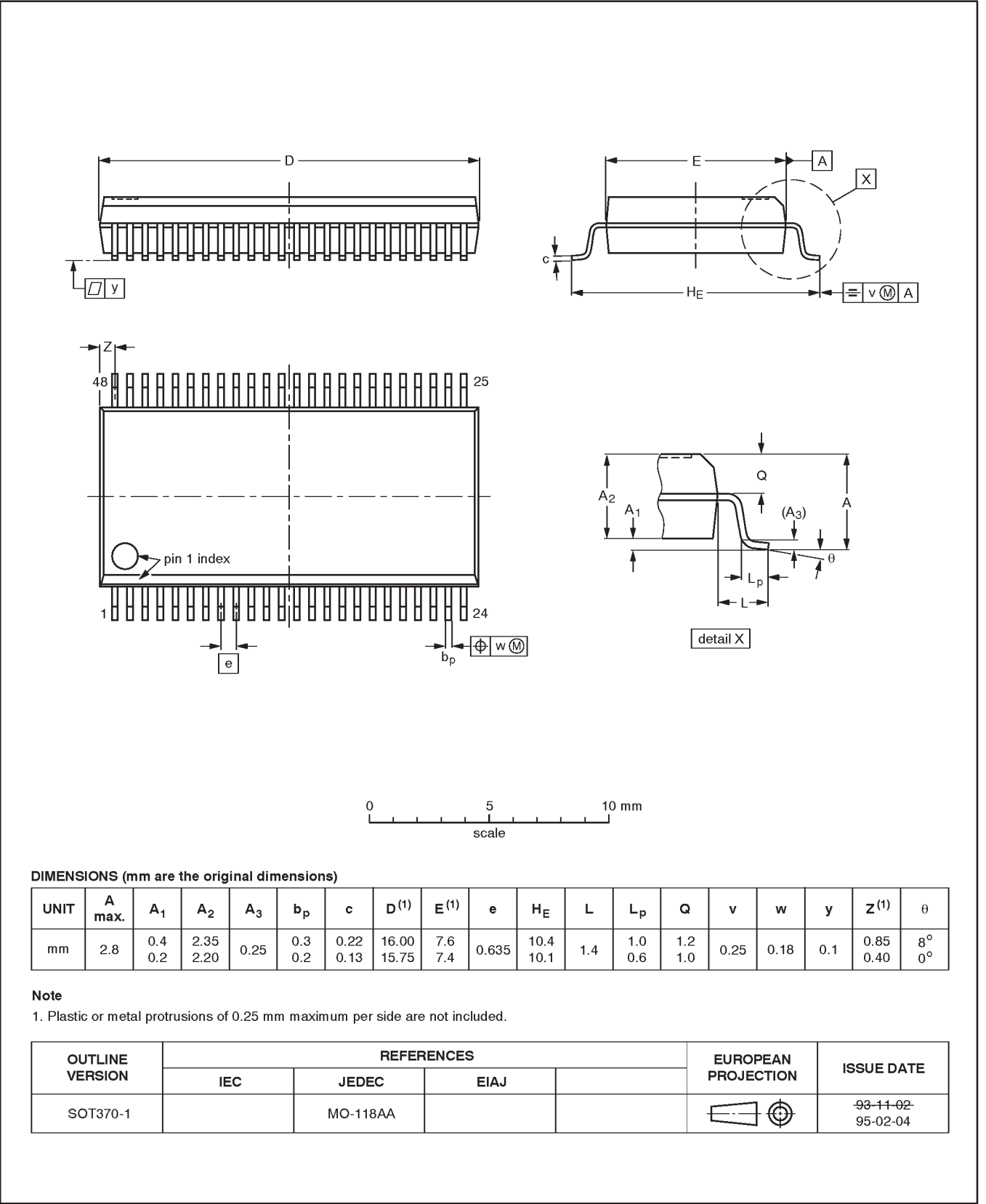
Waveform 5. Load circuitry for switching times

16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

74LVC16373A/
74LVCH16373A

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



16-bit D-type transparent latch with 5 Volt Tolerant inputs/outputs (3-State)

74LVC16373A/
74LVCH16373A

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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