

DATA SHEET

74LVC2245A

Octal transceiver with direction pin;
30 Ω series termination resistors;
5 V input/output tolerant; 3-state

Product specification
Supersedes data of 1999 Mar 23
File under Integrated Circuits, IC24

1999 Jun 15

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74LVC2245A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range of 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Integrated 30 Ω termination resistors

DESCRIPTION

The 74LVC2245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC2245A is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The '245' features an output enable ($\overline{\text{OE}}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{\text{OE}}$ controls the outputs so that the buses are effectively isolated.

The 74LVC2245A is designed with 30 Ω series termination resistors in both HIGH and LOW output stages to reduce line noise.

FUNCTION TABLE

See note 1.

INPUT		INPUT/OUTPUT	
$\overline{\text{OE}}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

Note

1. H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

ORDERING INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGE				
		TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC2245AD	74LVC2245AD	-40 to +85 °C	20	SO	plastic	SOT163-1
74LVC2245ADB	74LVC2245ADB		20	SSOP	plastic	SOT339-1
74LVC2245APW	74LVC2245APW DH		20	TSSOP	plastic	SOT360-1

Octal transceiver with direction pin; 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n ; B_n to A_n	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	3.9	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	$V_I = \text{GND to } V_{CC}$; note 1	27	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

PINNING

PIN	SYMBOL	DESCRIPTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{\text{OE}}$	output enable input (active LOW)
20	V_{CC}	DC supply voltage

Octal transceiver with direction pin; 30 Ω series
termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

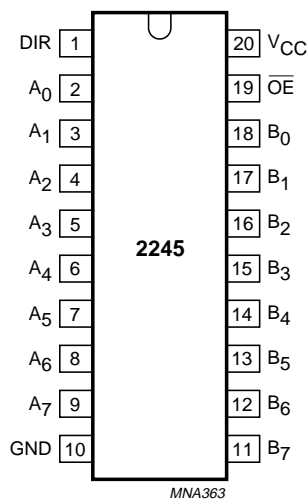


Fig.1 Pin configuration.

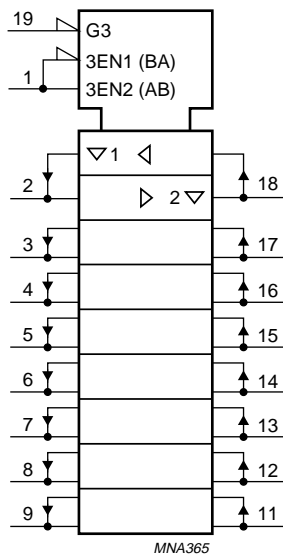


Fig.3 IEC logic symbol.

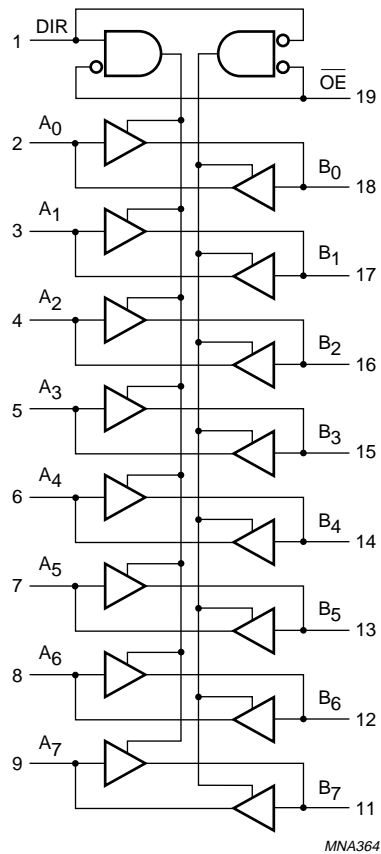


Fig.2 Logic symbol.

Octal transceiver with direction pin; 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; 3-state		0	5.5	V
T_{amb}	operating ambient temperature range	see DC and AC characteristics per device	-40	+85	$^{\circ}\text{C}$
t_r, t_f	input rise and fall times	$V_{CC} = 1.2$ to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ to 3.6 V	0	10	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	-	-50	mA
V_I	DC input voltage	note 1	-0.5	+5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	± 50	mA
V_O	DC output voltage; output HIGH or LOW	note 1	-0.5	$V_{CC} + 0.5$	V
	DC output voltage; output 3-state	note 1	-0.5	+6.5	V
I_O	DC output diode current	$V_O = 0$ to V_{CC}	-	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		-	± 100	mA
T_{stg}	storage temperature range		-65	+150	$^{\circ}\text{C}$
P_{tot}	power dissipation per package plastic mini-pack (SO)	above +70 $^{\circ}\text{C}$ derate linearly with 8 mW/K	-	500	mW
	plastic shrink mini-pack (SSOP and TSSOP)	above +60 $^{\circ}\text{C}$ derate linearly with 5.5 mW/K	-	500	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver with direction pin; 30 Ω series
termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

DC CHARACTERISTICS

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)			UNIT
		OTHER	V _{CC} (V)	−40 to +85			
				MIN.	TYP. ⁽¹⁾	MAX.	
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	−	−	V
			2.7 to 3.6	2.0	−	−	
V _{IL}	LOW-level input voltage		1.2	−	−	GND	V
			2.7 to 3.6	−	−	0.8	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = −6 mA	2.7	V _{CC} − 0.5	−	−	V
		V _I = V _{IH} or V _{IL} ; I _O = −100 μA	3.0	V _{CC} − 0.2	V _{CC}	−	
		V _I = V _{IH} or V _{IL} ; I _O = −12 mA	3.0	V _{CC} − 0.8	−	−	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 6 mA	2.7	−	−	0.40	V
		V _I = V _{IH} or V _{IL} ; I _O = 100 μA	3.0	−	−	0.20	
		V _I = V _{IH} or V _{IL} ; I _O = 12 mA	3.0	−	−	0.55	
I _I	input leakage current	V _I = 5.5 V or GND	3.6	−	±0.1	±5	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND	3.6	−	0.1	±10	μA
I _{off}	power off leakage supply	V _I or V _O = 5.5 V	0.0	−	0.1	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	−	0.1	20	μA
ΔI _{CC}	additional quiescent supply current per control pin	V _I = V _{CC} − 0.6 V; I _O = 0	2.7 to 3.6	−	5	500	μA

Note

1. All typical values are at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

Octal transceiver with direction pin; 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

AC CHARACTERISTICS

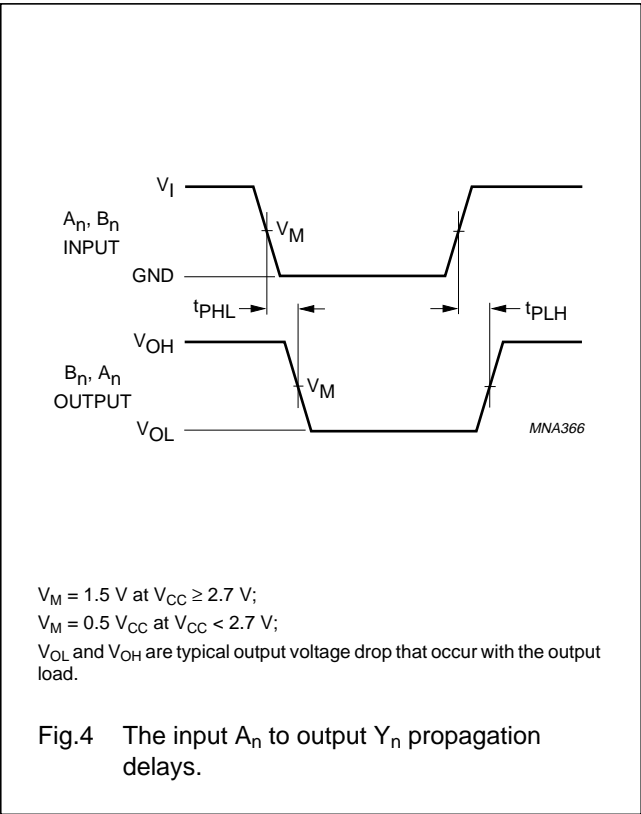
GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			V _{CC} = 3.3 V ±0.3 V			V _{CC} = 2.7 V		
			MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.	
t _{PHL} /t _{PLH}	propagation delay A _n to B _n ; B _n to A _n	see Figs 4 and 6	1.5	3.9	6.5	1.5	7.5	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to A _n ; OE to B _n	see Figs 5 and 6	1.5	5.7	9.0	1.5	10.0	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to A _n ; OE to B _n	see Figs 5 and 6	1.5	4.2	5.9	1.5	6.9	ns

Note

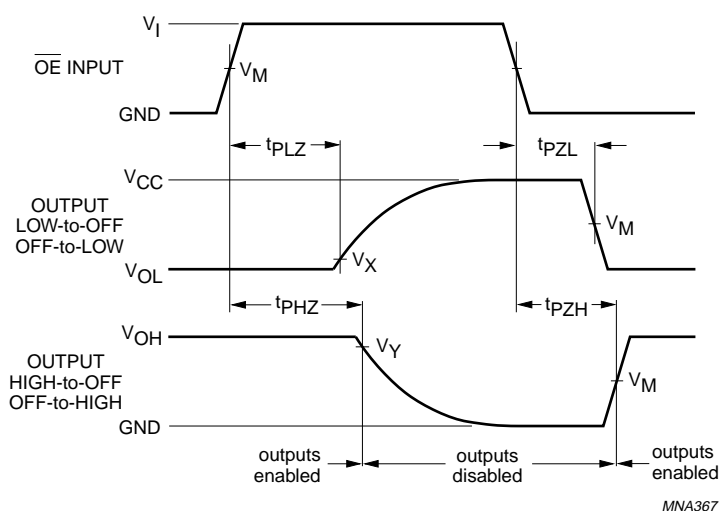
1. Typical values at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

AC WAVEFORMS



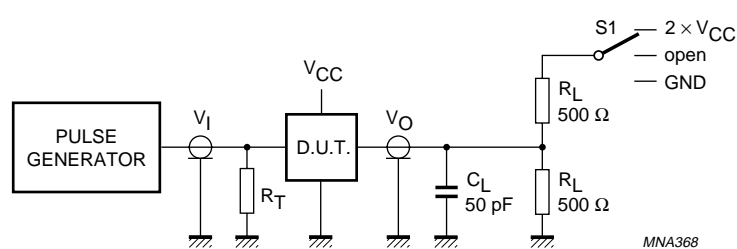
Octal transceiver with direction pin; 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

 $V_M = 1.5 \text{ V at } V_{CC} \geq 2.7 \text{ V};$
$$V_M = 0.5V_{CC} \text{ at } V_{CC} < 2.7 \text{ V};$$
$$V_X = V_{OL} + 0.3 \text{ V at } V_{CC} \geq 2.7 \text{ V};$$
$$V_X = V_{OL} + 0.1 \text{ V at } V_{CC} < 2.7 \text{ V};$$
$$V_Y = V_{OH} - 0.3 \text{ V at } V_{CC} \geq 2.7 \text{ V;}$$
$$V_Y = V_{OH} - 0.1 \text{ V at } V_{CC} < 2.7 \text{ V};$$

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 The 3-state enable and disable times.



TEST	S ₁
t _{PLH} /t _{PHL}	open
t _{PLZ} /t _{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	GND

V_{CC}	V_I
<2.7 V	V_{CC}
2.7 to 3.6 V	2.7 V

Definitions for test circuit:

R_L = Load resistor; see Chapter "AC characteristics".

C_L = Load capacitance including jig and probe capacitance (see Chapter "AC characteristics").

R_T = Termination resistance should be equal to the output Impedance Z_0 of the pulse generator.

Fig.6 Load circuitry for switching times.

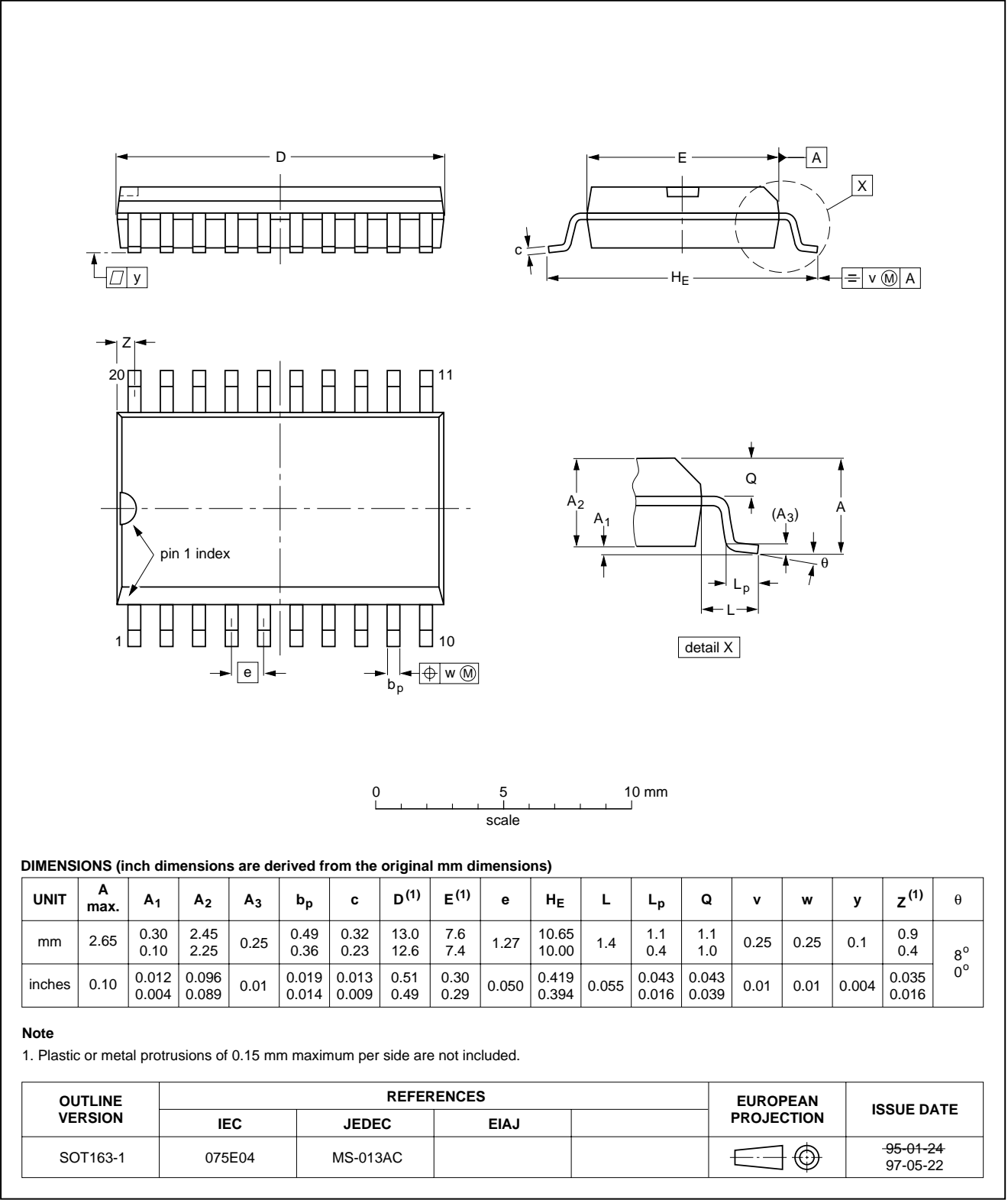
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termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

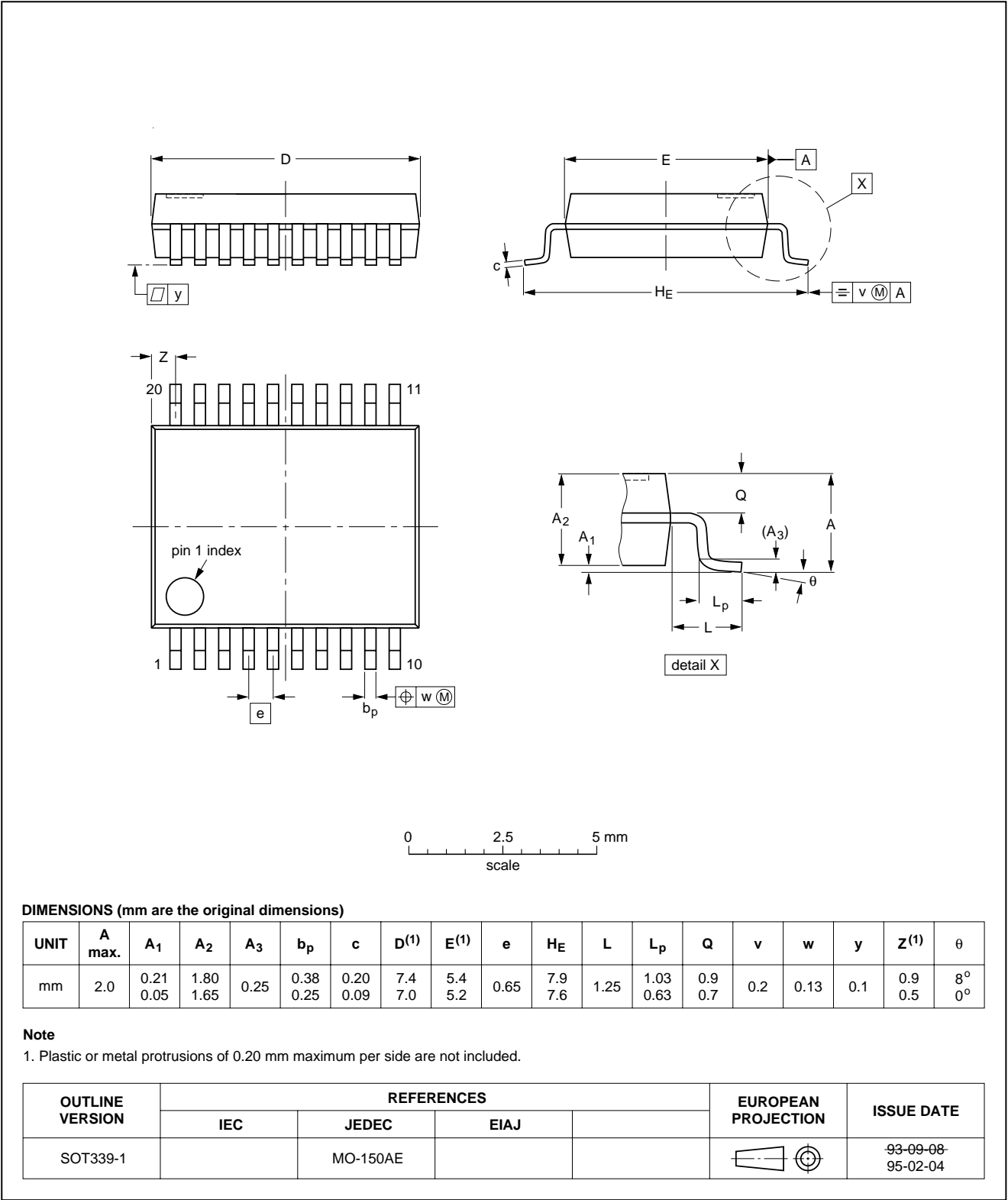


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termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

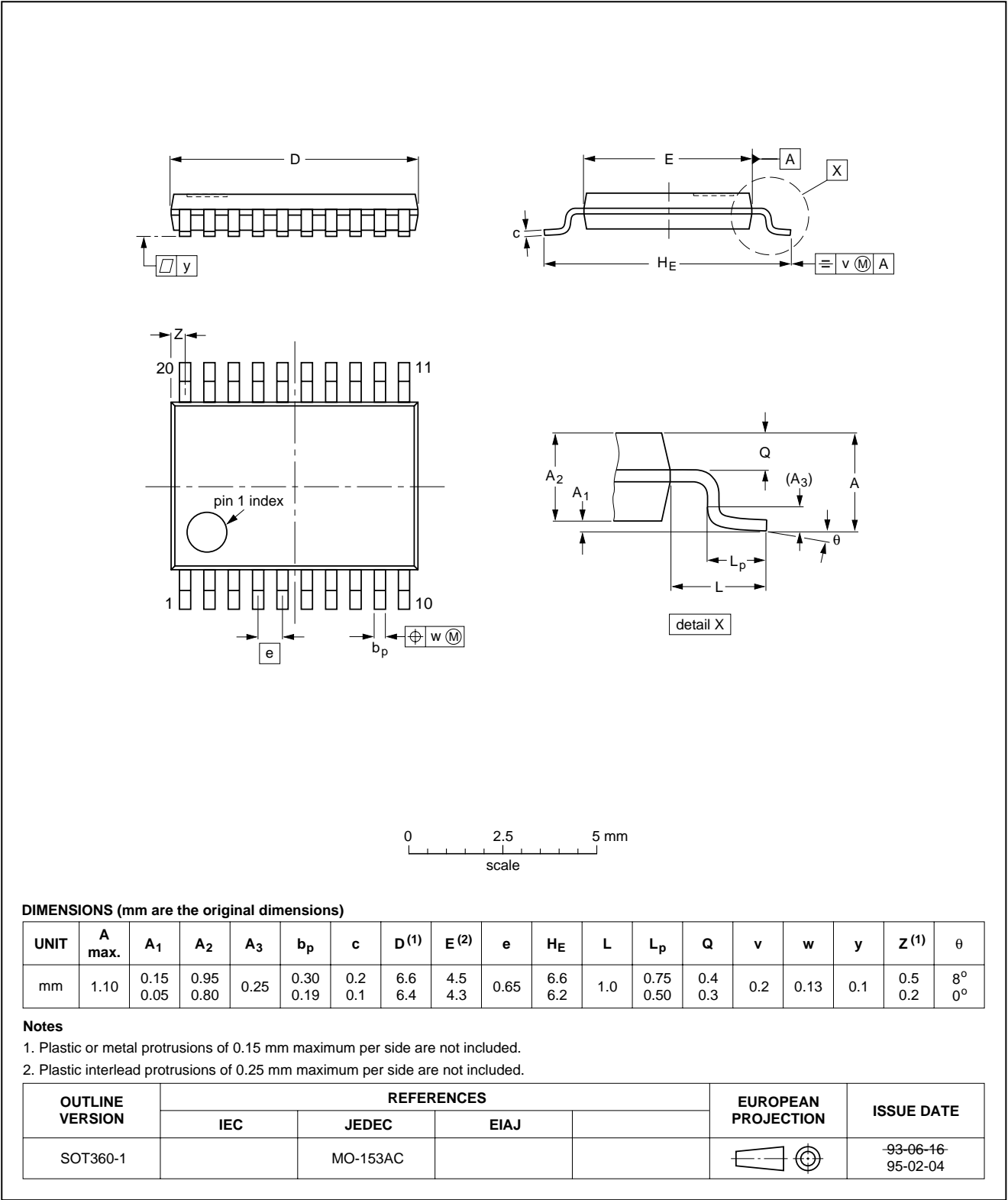


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74LVC2245A

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



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74LVC2245A

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Octal transceiver with direction pin; 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Octal transceiver with direction pin; 30 Ω series
termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

NOTES

Octal transceiver with direction pin; 30 Ω series
termination resistors; 5 V input/output tolerant; 3-state

74LVC2245A

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Printed in The Netherlands

245004/02/pp16

Date of release: 1999 Jun 15

Document order number: 9397 750 05624

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