DATA SHEET

74F779
8-bit bidirectional binary counter (3-State)

Product specification

1989 Sep 20

IC15 Data Handbook

Philips
Semiconductors

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8-bit bidirectional binary counter (3-State) 74F779

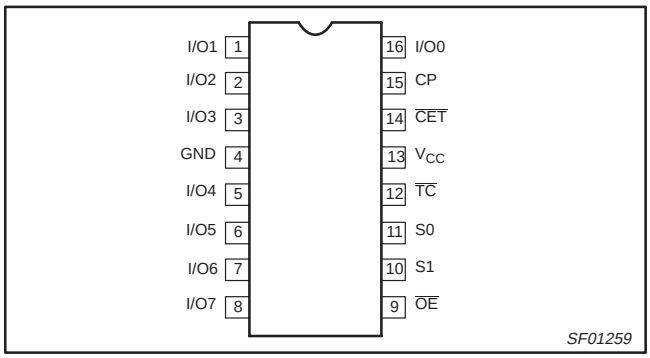
FEATURES

- Multiplexed 3-State I/O ports for bus oriented applications
- Built-in look-ahead carry capability
- Center power pins to reduce effects of package inductance
- Count frequency 145MHz typical
- Supply current 90mA typical
- See 74F269 for 24-pin separate I/O port version
- See 74F579 for 20-pin version
- See 74F1779 for extended function version of the 74F799

DESCRIPTION

The 74F779 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-State I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pine (S0, S1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{CET}$ is High the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779	145MHz	90mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-Pin Plastic DIP	N74F779N	SOT38-4
16-Pin Plastic SOL	N74F779D	SOT 162-1

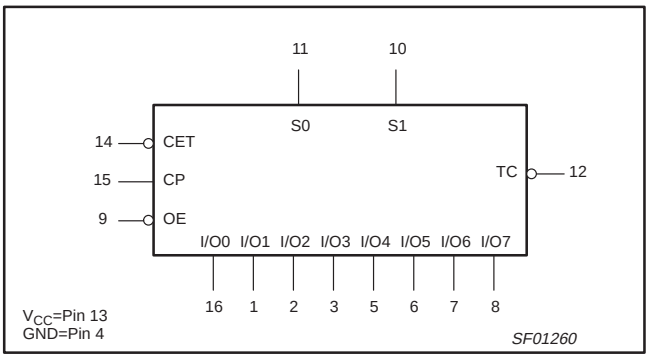
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S0, S1	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA

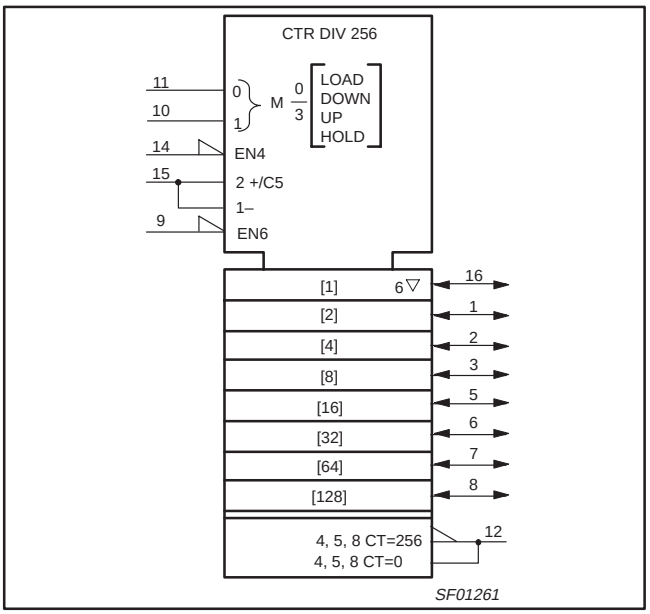
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

8-bit bidirectional binary counter (3-State) 74F779

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

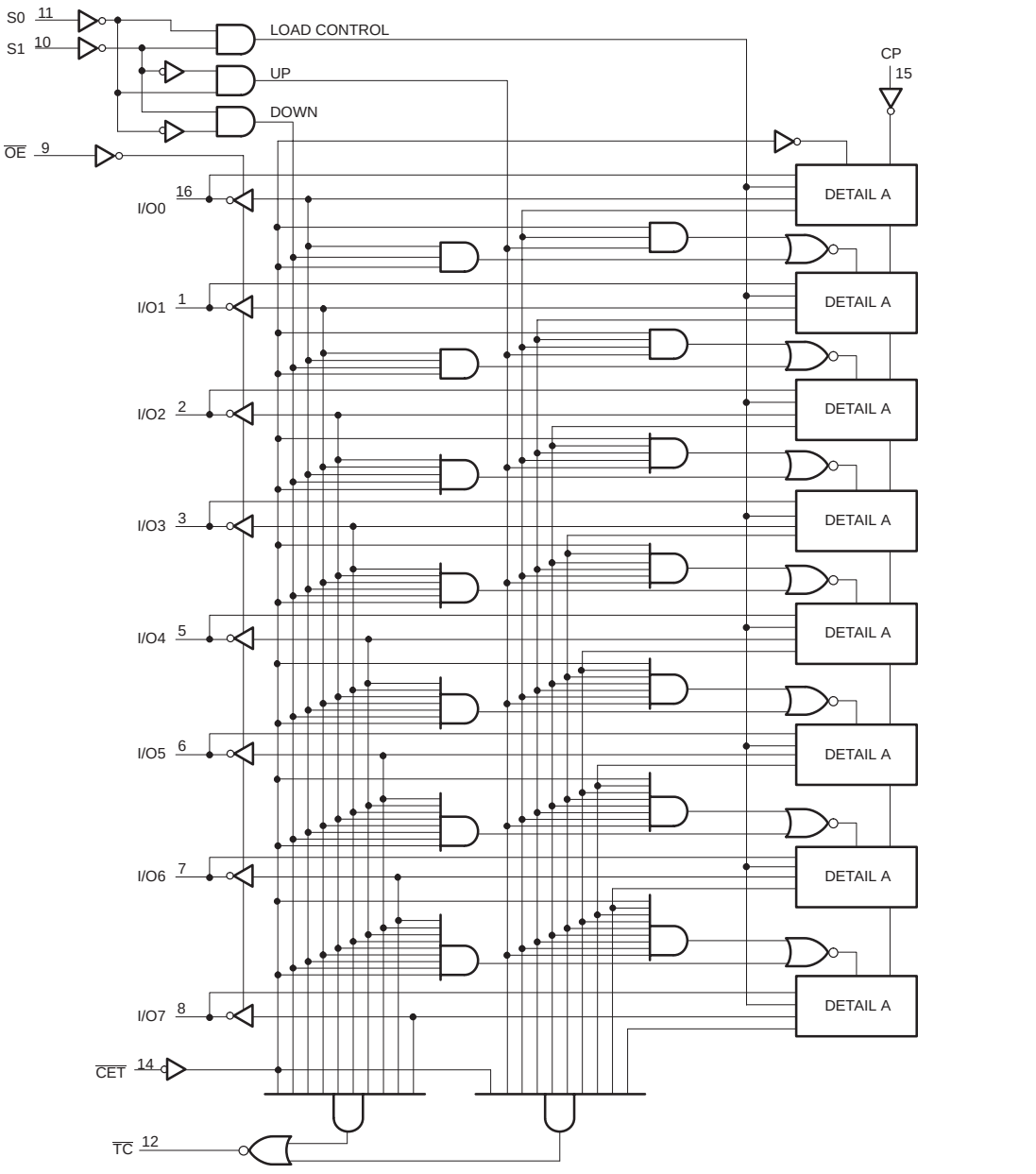


FUNCTION TABLE

INPUTS					OPERATING MODE
S1	**S0**	**$\overline{CET}$**	**$\overline{OE}$**	**CP**	
X	X	X	H	X	I/O0 to I/O7 in High impedance
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S0 and S1 should never be Low voltage level at the same time in the hold mode only.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/On	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	$\overline{TC}$			–1	mA
		I/On			–3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/On			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]			LIMITS			UNIT
						MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	I/On	V_{CC} = 5.5V, V_I = 5.5V					1	mA
		others	V_{CC} = 5.5V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	except I/On	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	I/On	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–600	µA
I_{OS}	Short-circuit output current[NO TAG]		V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				82	116	mA
		I_{CCL}					91	128	mA
		I_{CCZ}					97	136	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	125	145		115		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/On	Waveform 1	4.5 5.5	7.0 8.0	10.5 10.5	4.5 5.5	11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 4.5	7.0 7.0	9.0 9.0	4.5 4.5	10.0 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.5	2.5 2.5	7.5 8.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	2.5 4.5	4.5 6.5	7.0 9.0	2.5 4.5	8.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Enable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.5 7.0	1.0 1.0	8.0 8.0	ns ns

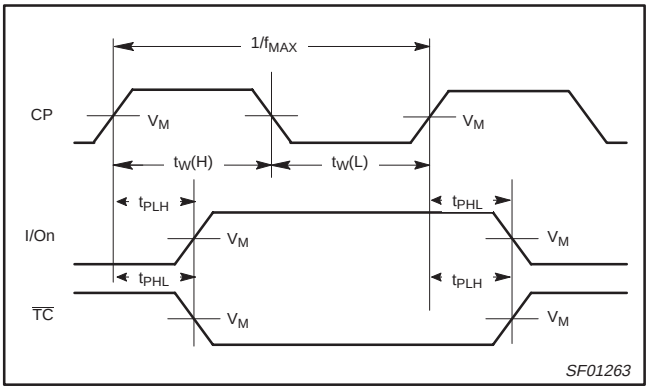
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	5.0 5.0			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	5.0 5.5			5.0 6.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low Sn to CP	Waveform 3	8.0 8.0			8.5 8.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Sn to CP	Waveform 3	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 4.0			4.0 4.0		ns ns

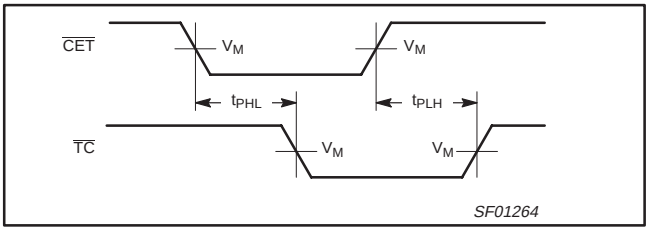
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

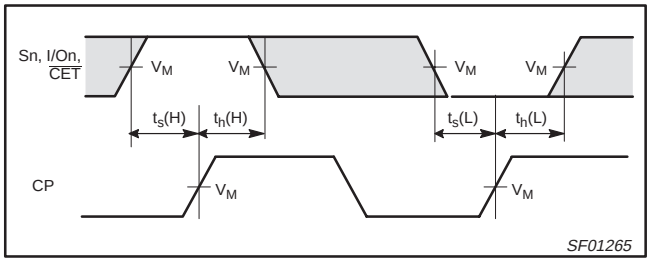
The shaded areas indicate when the input is permitted to change for predictable output performance.



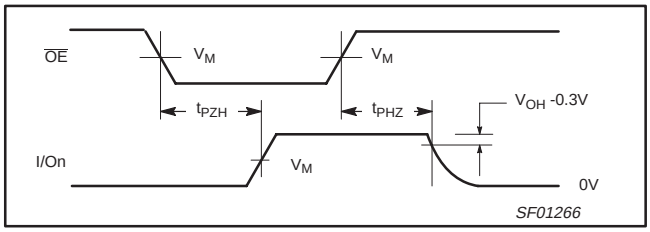
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



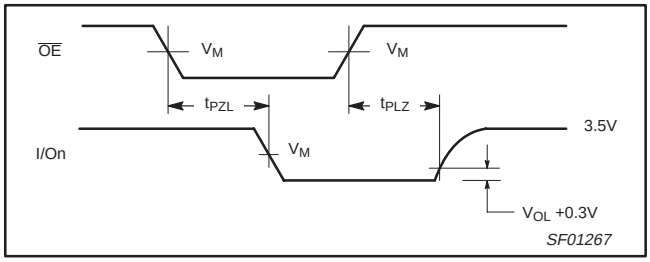
Waveform 2. Propagation Delay $\overline{CET}$ Input to Terminal Count Output



Waveform 3. Data Setup and Hold Times

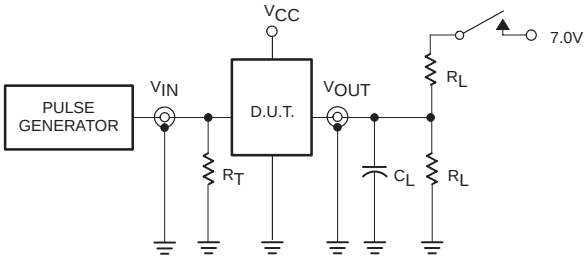


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

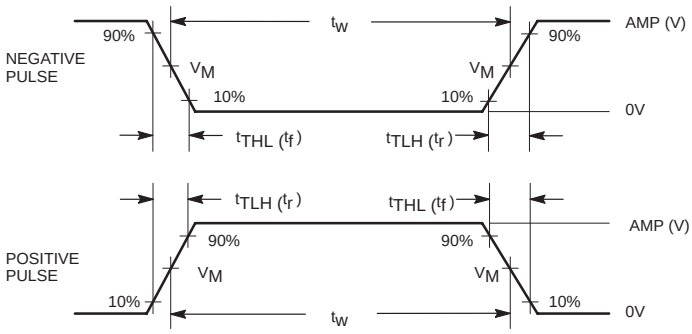


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

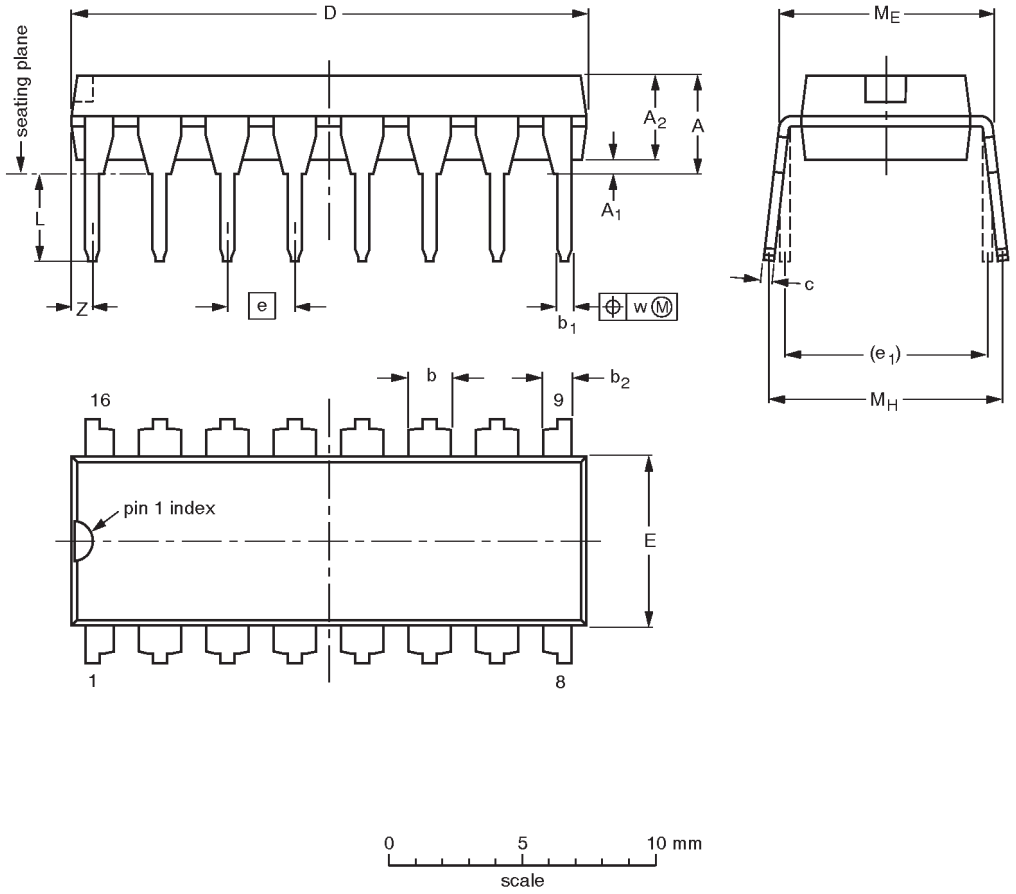
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

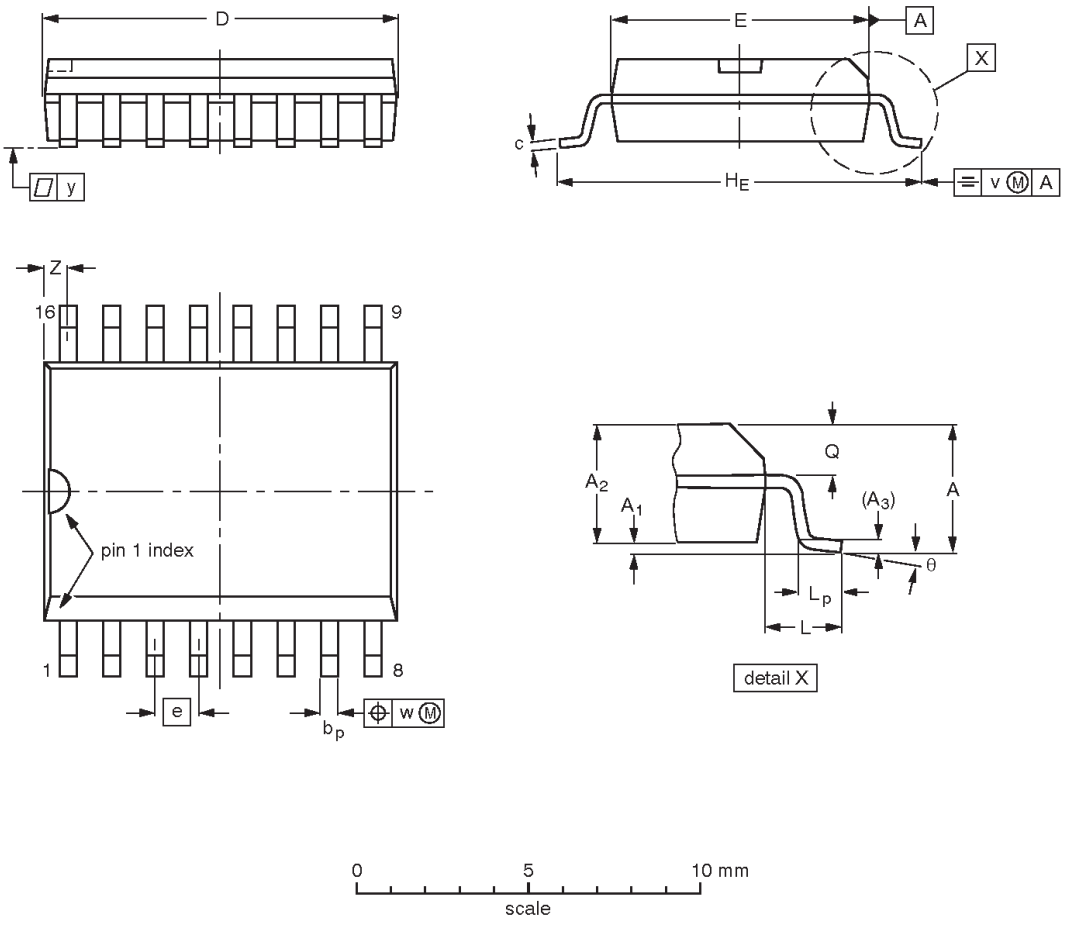
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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