

# DATA SHEET

## **74F597**

**8-bit shift register with input storage registers**

Product specification

1991 Sep 13

IC15 Data Handbook

## 8-bit shift register with input storage registers

74F597

## FEATURES

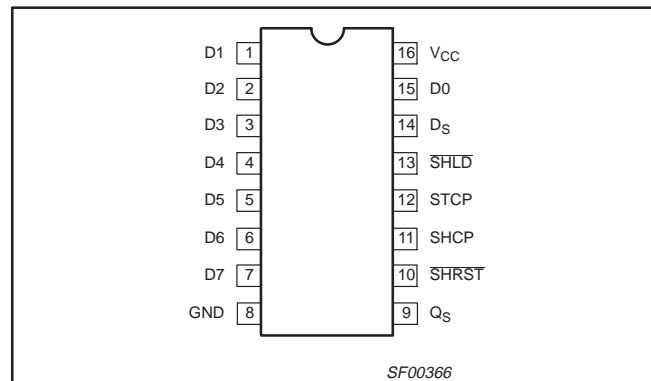
- High impedance PNP base inputs for reduced loading (20 $\mu$ A in High and Low states)
- 8-bit parallel storage register
- 3-State output buffers
- Shift register has asynchronous direct overriding reset
- Shift load  $\overline{\text{SHLD}}$  is functional when SHCP is Low and locked out when SHCP is High
- Guaranteed shift frequency DC to 105MHz

## DESCRIPTION

The 74F597 consists of an 8-bit storage register feeding a parallel-in/serial-in, serial-out 8-bit shift register. The storage register and shift register have separate positive edge triggered clocks. The shift register has asynchronous reset and when SHCP is Low, it has asynchronous load.

The shift register load function has been modified to load when both  $\overline{\text{SHLD}}$  and SHCP are Low. When SHCP is High the shift register load operation is not performed. Data will be properly shifted on the rising edge of SHCP when  $\overline{\text{SHLD}}$  is High.

## PIN CONFIGURATION



TYPE	TYPICAL $f_{\text{MAX}}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	135MHz	42mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{\text{CC}} = 5V \pm 10\%$ , $T_{\text{amb}} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	PKG DWG #
16-pin plastic DIP	N74F597N	SOT38-4
16-pin plastic SO	N74F597D	SOT109-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ds	Serial data input	1.0/0.033	20 $\mu$ A/20 $\mu$ A
D0–D7	Parallel data inputs	1.0/0.033	20 $\mu$ A/20 $\mu$ A
SHCP	Shift register clock pulse input	1.0/0.033	20 $\mu$ A/20 $\mu$ A
STCP	Storage register clock pulse input	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{\text{SHLD}}$	Shift register load input (active Low)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
SHRST	Shift register reset input (active Low)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
Qs	Serial data output	50/33	1.0mA/20mA

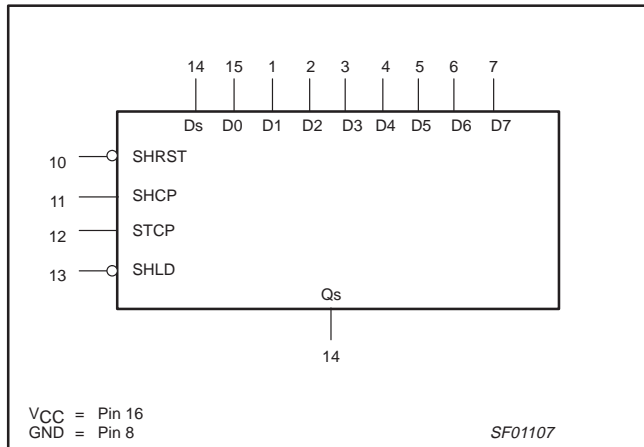
## NOTE:

One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

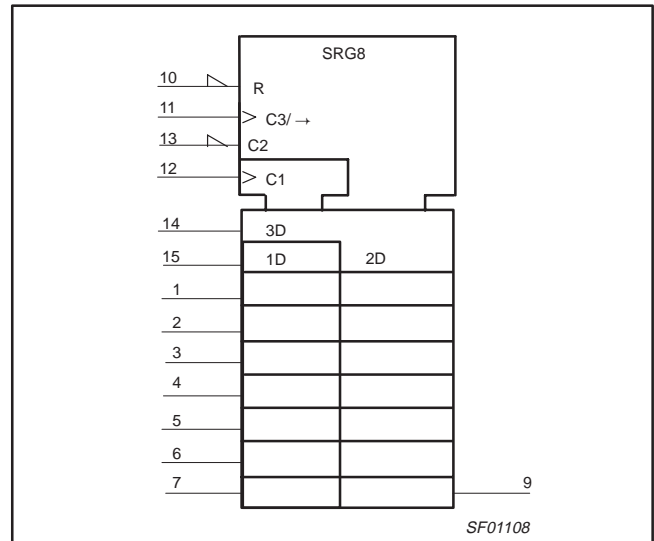
# 8-bit shift register with input storage registers

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## LOGIC SYMBOL



## IEC/IEEE SYMBOL (IEEE/IEC)



## FUNCTION TABLE

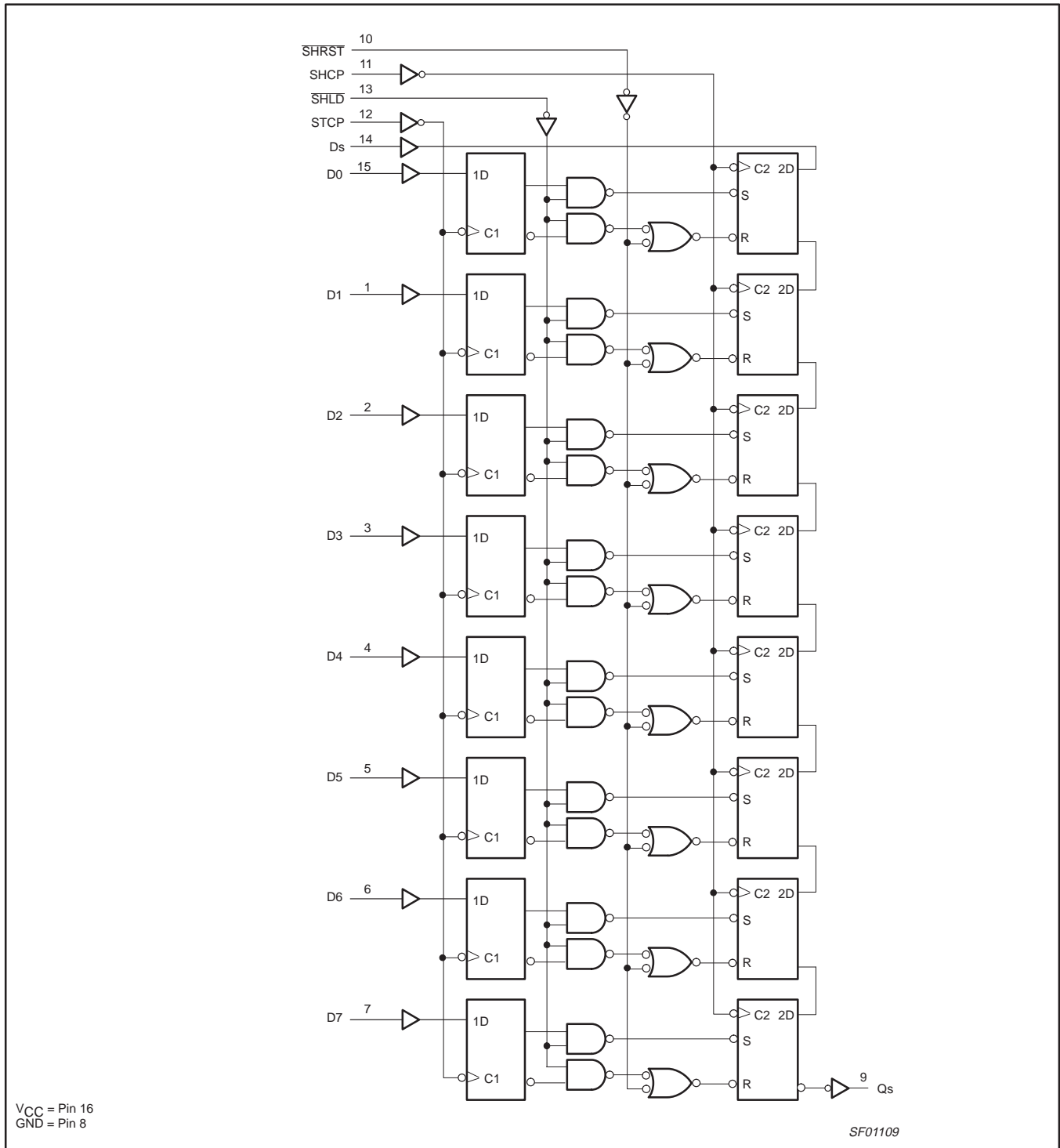
INPUTS				OPERATING MODES
STCP	SHCP	SHLD	SHRST	
↑	X	X	X	Data loaded to storage registers
↑	L	L	H	Data loaded from inputs to shift register
↑	L	L	H	Data transferred from storage registers to shift registers
X	L	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked, Qn=Qn-1, Q0=Ds
↑	H	X	H	Hold

- H = High voltage level
- L = Low voltage level
- X = Don't care
- ↑ = Low-to-High clock transition
- ↑ = Not a Low-to-High clock transition

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## LOGIC DIAGRAM



## 8-bit shift register with input storage registers

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>NO TAG</sup>		LIMITS			UNIT	
				MIN	TYP NO TAG	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -1mA	±10%V <sub>CC</sub>	2.5		V	
				±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX		±10%V <sub>CC</sub>		0.30	0.50	V
				±5%V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				-20	μA	
I <sub>OS</sub>	Short-circuit output current <sup>NO TAG</sup>	V <sub>CC</sub> = MAX			-60	-150	mA	
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX			43	65	mA
		I <sub>CCL</sub>				41	60	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$f_{MAX}$	Maximum clock frequency	Waveform NO TAG	120	135		105		MHz
$t_{PLH}$ $t_{PHL}$	Propagation delay SHCP to Qs	Waveform NO TAG	7.0 6.0	8.5 7.5	11.0 10.0	6.0 5.5	12.5 10.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay SHLD to Qs	Waveform NO TAG	8.0 6.0	9.5 7.5	12.0 10.0	7.0 5.5	13.5 11.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay STCP to Qs	Waveform NO TAG	7.5 8.0	9.5 9.5	11.5 12.0	6.5 7.5	13.0 13.0	ns
$t_{PHL}$	Propagation delay SHRST to Qs	Waveform NO TAG	2.5	5.5	9.0	2.5	9.5	ns

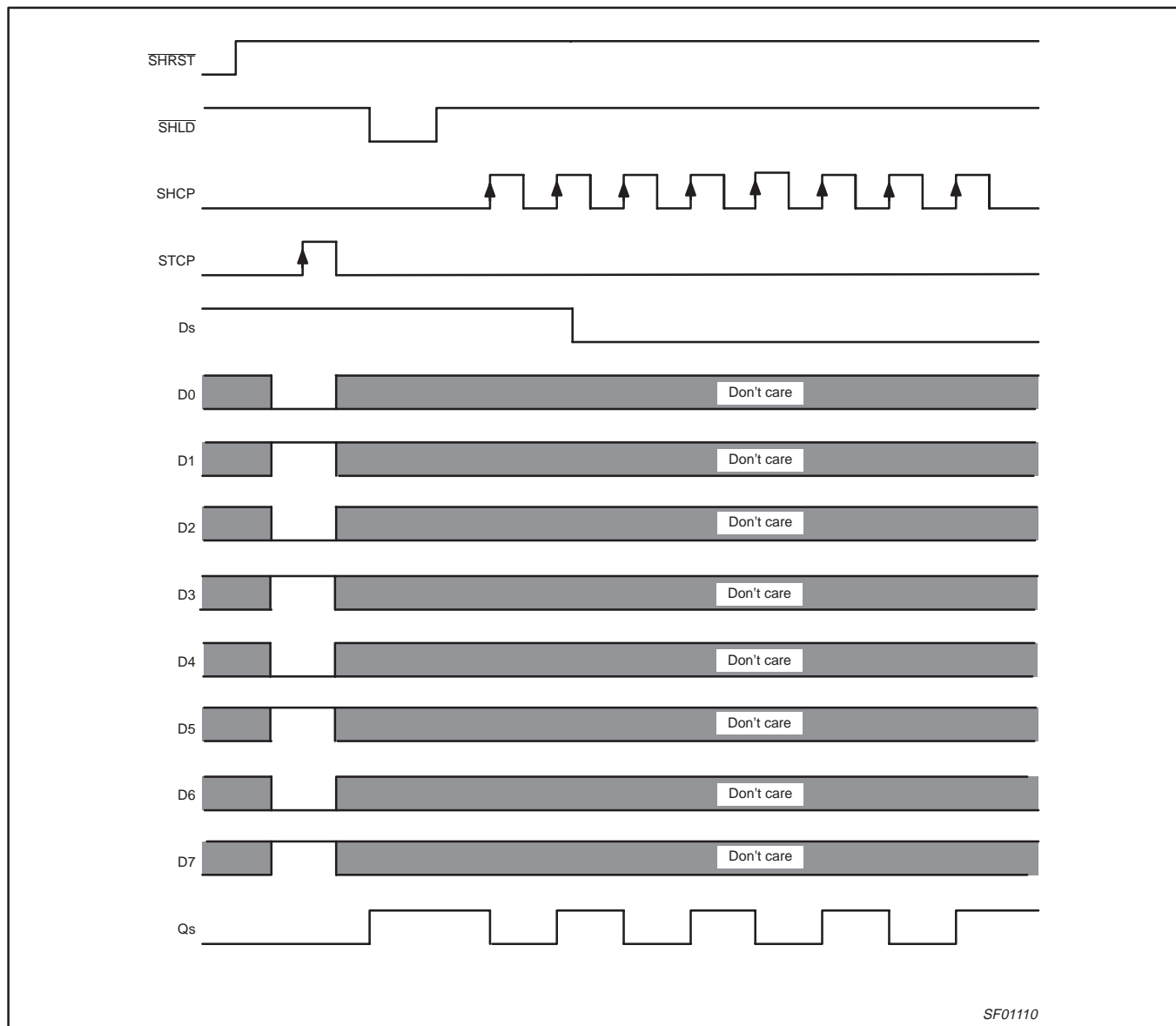
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to STCP	Waveform NO TAG	1.0 1.5			1.5 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to STCP	Waveform NO TAG	2.0 2.0			2.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low Ds to SHCP	Waveform NO TAG	1.0 1.5			1.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Ds to SHCP	Waveform NO TAG	1.5 2.0			2.0 2.5		ns
$t_s(H)$	Setup time, High STCP to SHLD $\uparrow$	Waveform 4	8.5			9.0		ns
$t_h(L)$	Hold time, Low STCP to SHLD $\uparrow$ (hold mode)	Waveform NO TAG	0.0			0.0		ns
$t_s(H)$	Setup time, High SHLD to SHCP $\uparrow$	Waveform NO TAG	6.0			6.5		ns
$t_W(H)$ $t_W(L)$	SHCP Pulse width High or Low	Waveform NO TAG	4.5 4.5			5.5 4.5		ns
$t_W(H)$ $t_W(L)$	STCP Pulse width High or Low	Waveform NO TAG	4.5 4.5			5.0 4.5		ns
$t_W(L)$	SHRST Pulse width, Low	Waveform NO TAG	4.5			4.5		ns
$t_W(L)$	SHLD Pulse width, Low	Waveform NO TAG	4.5			4.5		ns
$t_{REC}$	Recovery time, SHRST to SHCP	Waveform NO TAG	2.0			2.5		ns

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## TYPICAL TIMING DIAGRAM



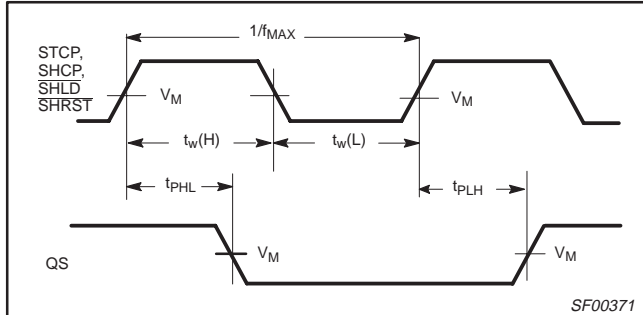
# 8-bit shift register with input storage registers

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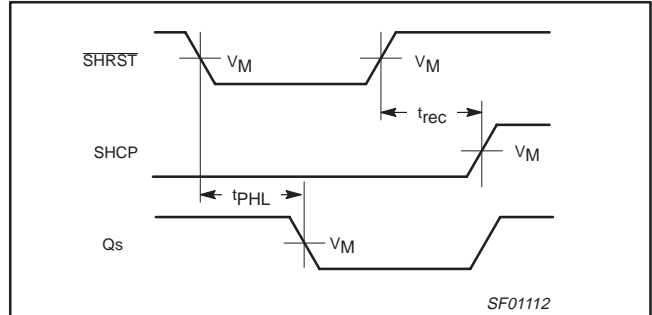
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

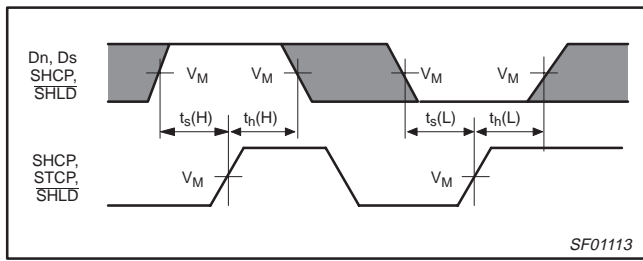
The shaded areas indicate when the input is permitted to change for predictable output performance.



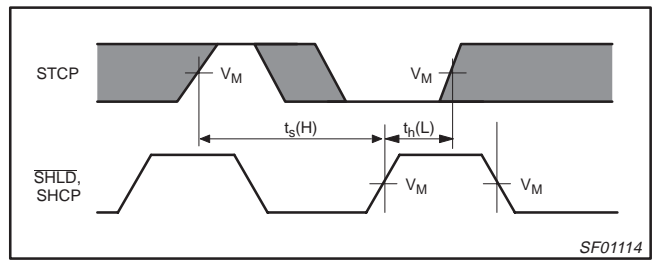
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency, Shift Register Reset and Load Inputs to Serial Data Output**



**Waveform 2. Propagation Delay, Shift Register Reset and Load Inputs to Serial Data Output, Shift Register Reset and Load Inputs to Shift Register Clock Pulse Input Recovery Time**

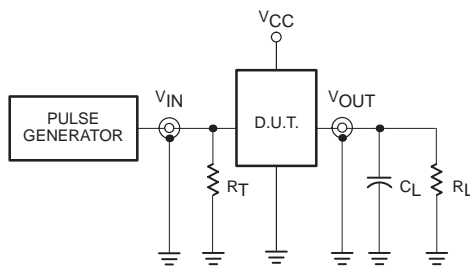


**Waveform 3. Setup and Hold Times**

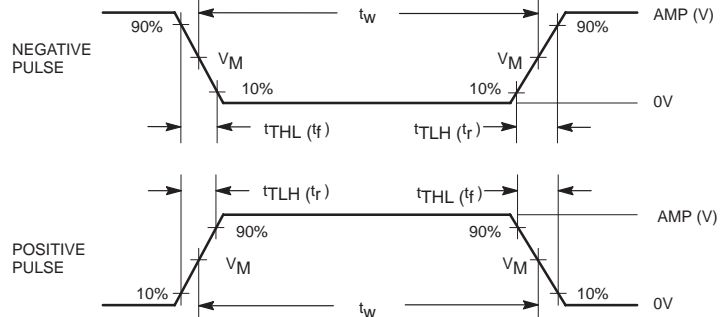


**Waveform 4. Setup and Hold Time**

## TEST CIRCUIT AND WAVEFORMS



**Test Circuit for Totem-Pole Outputs**



**Input Pulse Definition**

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

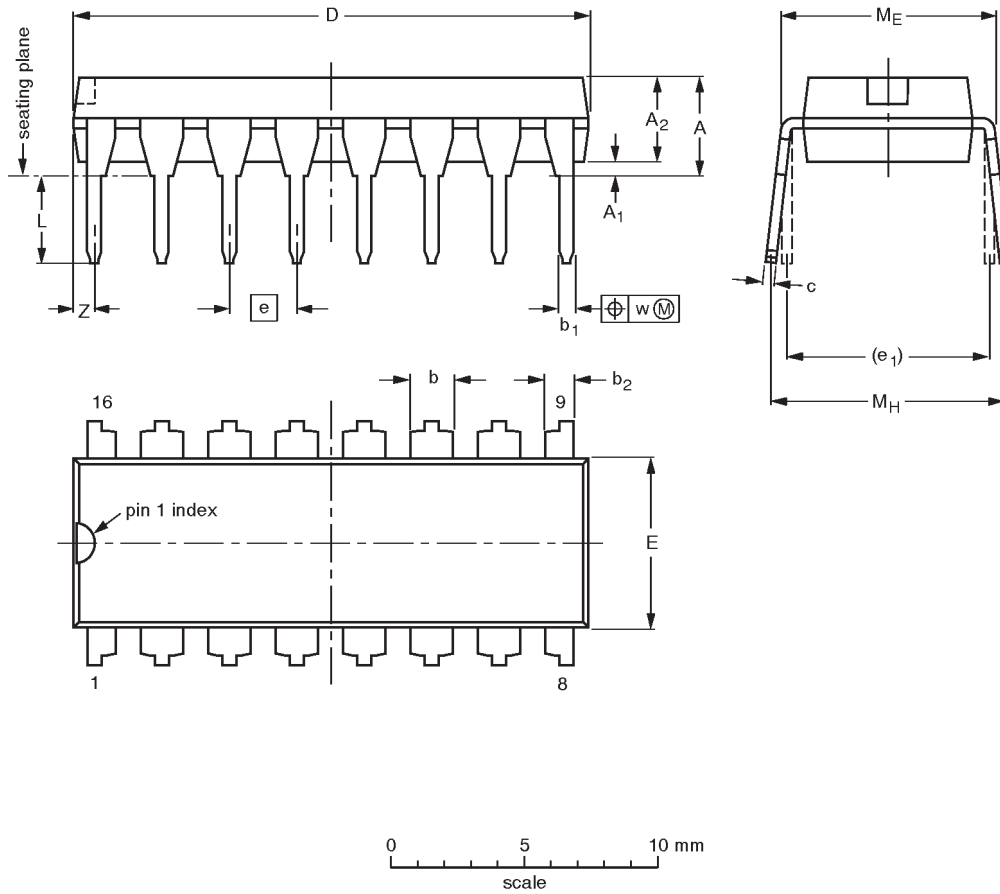


# 8-bit shift register with input storage registers

74F597

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

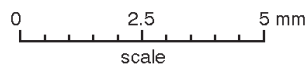
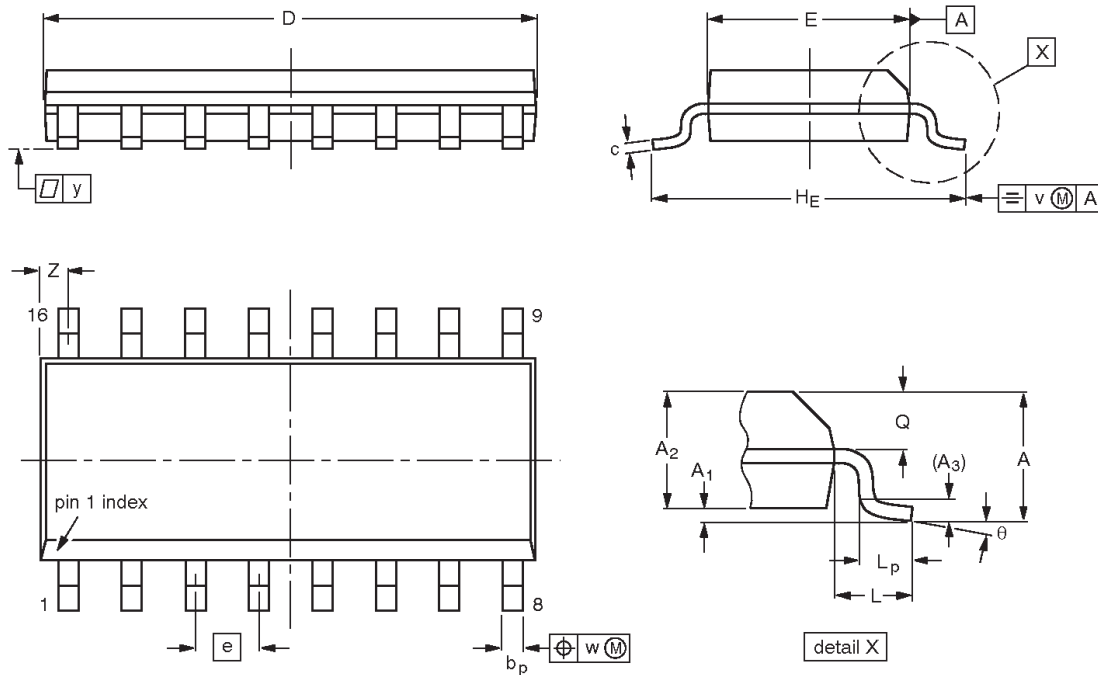
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

# 8-bit shift register with input storage registers

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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## NOTES

## 8-bit shift register with input storage registers

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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