INTEGRATED CIRCUITS

DATA SHEET

74F3038

Quad 2-input NAND 30 Ω line driver (open collector)

Product specification Supersedes data of 1990 Jan 29 IC15 Data Handbook





Quad 2-input NAND 30 Ω line driver (open collector)

74F3038

FEATURES

- 30Ω line driver
- 160mA output drive capability
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V_{CC} and GND when both side pins are used

DESCRIPTION

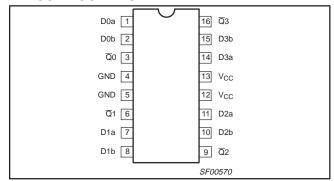
The 74F3038 is a high current Open-Collector Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The 74F3038 can sink 160mA with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OL} not more than 0.8V while driving impedances as low as 30Ω . This is applicable with any combination of outputs using continuous duty.

The AC specifications for the 74F3038 were determined using the standard FAST load for open-collector parts of 50pF capacitance, a 500 Ω pull-up resistor and a 500 Ω pull-down resistor. (See Test Circuit).

Reducing the load resistors to 100Ω will decrease the t_{PLH} propagation delay by approximately 50% while increasing t_{PHL} only slightly. The graph of typical propagation delay versus load resistor (see AC Characteristics section for Graph) shows a spline fit curve from four measured data points, $R_L=30\Omega,\ R_L=100\Omega,\ R_L=300\Omega,$ and $R_L=500\Omega.$

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	6.0ns	17mA

ORDERING INFORMATION

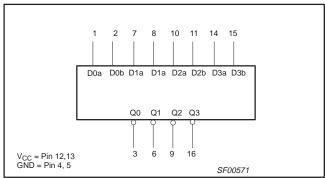
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V $\pm 10\%$, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
16-pin Plastic DIP	N74F3038N	SOT38-4
16-pin Plastic SOL	N74F3038D	SOT162-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

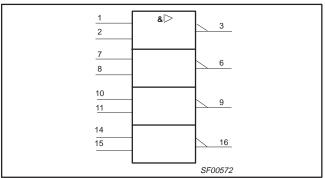
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
Qn	Data outputs	OC/266	OC/160mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state. OC = Open Collector.

LOGIC SYMBOL



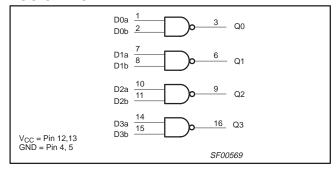
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

INP	OUTPUT	
Dna	Dnb	Qn
L	L	Н
L	Н	Н
н	L	Н
Н	Н	L

H = High voltage level L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	−30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	−0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	320	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DADAMETED		UNIT		
STWIBUL	PARAMETER	MIN	NOM	MAX	UNII
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
V _{OH}	High-level output voltage			4.5	V
I _{OL}	Low-level output current			160	mA
T _{amb}	Operating free-air temperature range	0		+70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

CVMDOL	PARAMETER			CT CONDITION	e1		LIMITS		TINU
SYMBOL	PARAMETER		"	TEST CONDITIONS ¹				MAX	UNII
I _{OH}	High-level output current		$V_{CC} = MIN, V_{II}$	$=$ MAX, $V_{IH} = M$	$IN, V_{OH} = MAX$			250	μΑ
V	Low level output ourrent		$V_{CC} = MIN$ $V_{II} = MAX$	I _{OL} = 100mA	±10% V _{CC}		0.42	0.55	V
VOL	V _{OL} Low-level output current		V _{IH} = MIN	$I_{OL} = 160 \text{mA}^3$	±5% V _{CC}			0.80	V
V _{IK}	Input clamp voltage		$V_{CC} = MIN, I_I = I_{IK}$				-0.73	-1.2	V
I _I	Input current at maximum voltage	n input	$V_{CC} = MAX, V_I = 7.0V$					100	μΑ
I _{IH}	High-level input current		$V_{CC} = MAX, V_I = 2.7V$					20	μΑ
I _{IL}	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$					-0.6	mA
	I _{CCH}		V MANY		V _{IN} = GND		3.5	6.0	mA
Icc	Supply current (total)	I _{CCL}	$V_{CC} = MAX$		V _{IN} = 4.5V		30	40	mA

NOTES:

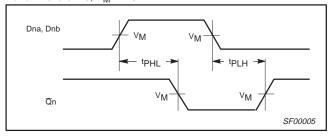
- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- 2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C. 3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_{L} = 50\text{pF}, R_{L} = 500\Omega$			T _{amb} = 0°C V _{CC} = +5. C _L = 50pF,	UNIT	
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	6.0 1.0	8.5 2.0	11.5 5.0	6.0 1.0	12.0 5.0	ns

AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

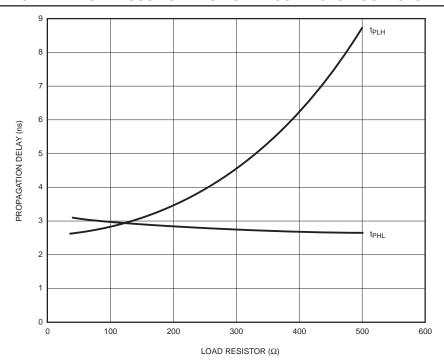


Waveform 1. **Propagation Delay for Inputs to Output**

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TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

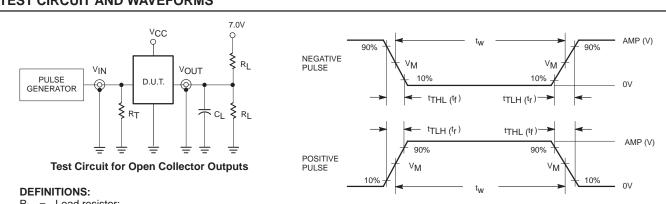


NOTE:

When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the tPLH. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL} . However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total $I_{IL}s$ of the receivers does not exceed the I_{OL} maximum specification.

SF01361

TEST CIRCUIT AND WAVEFORMS



 R_L = Load resistor;

see AC electrical characteristics for value.

Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS										
laililly	amplitude	V_{M}	rep. rate	t _w	t _{TLH}	t _{THL}					
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns					

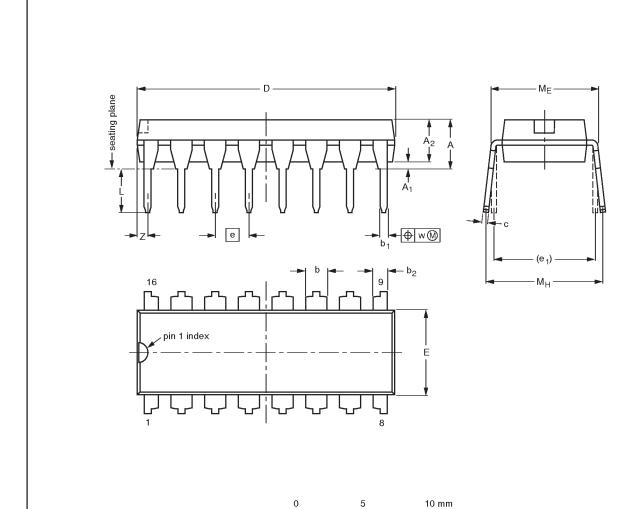
SF00027

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

scale

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT38-4					-92-11-17 95-01-14	

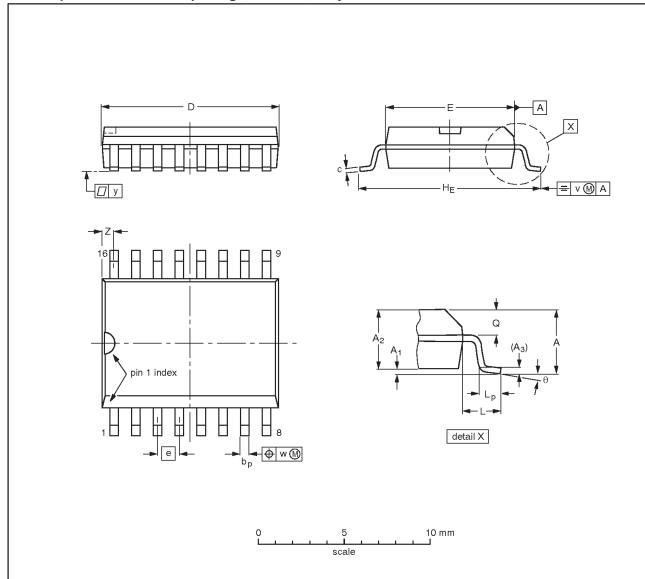
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SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	e	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT162-1	075E03	MS-013AA			95 01 24 97-05-22	

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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