# INTEGRATED CIRCUITS

# DATA SHEET

# 74ALVT162821

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

Product specification Supersedes data of 1997 Feb 13 IC23 Data Handbook





# 2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with 30 $\Omega$ termination resistors (3-State)

# 74ALVT162821

#### **FEATURES**

- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- 20-bit positive-edge triggered register
- 5V I/O Compatible
- Multiple V<sub>CC</sub> and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Output capability +12mA/-12mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

#### DESCRIPTION

The 74ALVT162821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for  $V_{CC}$  operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT162821 has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (nOE) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ( $n\overline{OE}$ ) controls all ten 3-State buffers independent of the register operation. When  $n\overline{OE}$  is Low, the data in the register appears at the outputs. When  $n\overline{OE}$  is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74ALVT162821 is designed with  $30\Omega$  series resistance in both High and Low output stages. This design reduces the line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters. The series termination resistors reduce overshoot and undershoot and are ideal for driving memory arrays.

#### **QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	TYPI	UNIT	
STIMBOL	FARAMETER	T <sub>amb</sub> = 25°C		3.3V	ONIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nCP to nQ	C <sub>L</sub> = 50pF	4.4 3.8	3.2 3.2	ns
C <sub>IN</sub>	Input capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	3	3	pF
C <sub>OUT</sub>	Output capacitance	$V_O = 0$ or $V_{CC}$	9	9	pF
I <sub>CCZ</sub>	Total supply current	Outputs disabled	40	70	μΑ

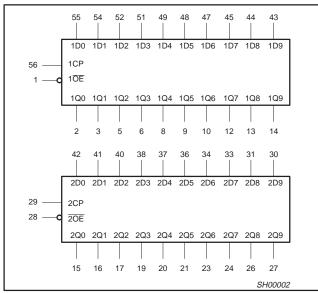
#### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ALVT162821 DL	AV162821 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVT162821 DGG	AV162821 DGG	SOT364-1

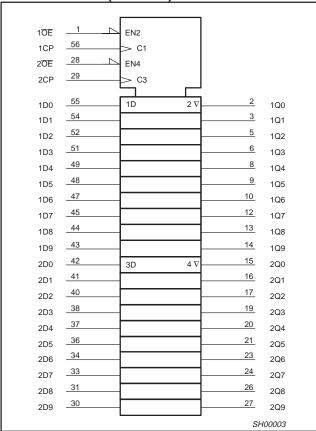
2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

# 74ALVT162821

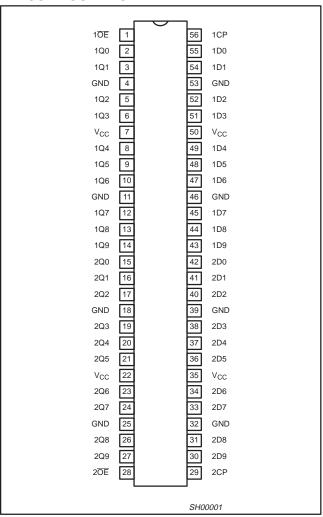
### LOGIC SYMBOL



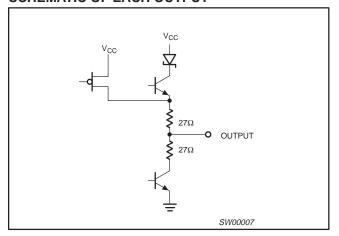
# LOGIC SYMBOL (IEEE/IEC)



#### **PIN CONFIGURATION**



## **SCHEMATIC OF EACH OUTPUT**



2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

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# **PIN DESCRIPTION**

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	1 <del>0E</del> , 2 <del>0E</del>	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V <sub>CC</sub>	Positive supply voltage

# **FUNCTION TABLE**

ı	NPUTS	5	INTERNAL	OUTPUTS	OPERATING
nOE	nCP	nDx	REGISTER	nQ0 - nQ9	MODE
L	$\uparrow$	l h	L H	L H	Load and read register
L	1	Х	NC	NC	Hold
H	<b></b>	X Dn	NC Dn	Z Z	Disable outputs

High voltage level

High voltage level one set-up time prior to the Low-to-High clock transition

Low voltage level

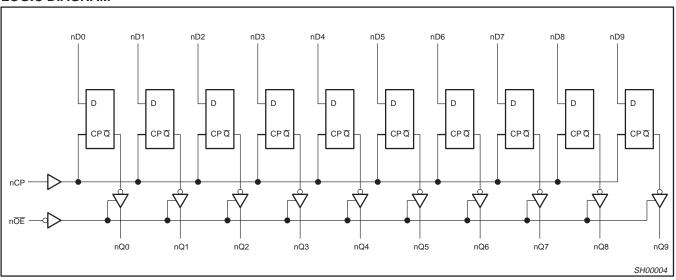
Low voltage level one set-up time prior to the Low-to-High clock transition

No change

Don't care

High impedance "off" state
Low to High clock transition
Not a Low-to-High clock transition

# **LOGIC DIAGRAM**



2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

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# ABSOLUTE MAXIMUM RATINGS1, 2

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
VI	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
	DC sustaint sussant	Output in Low state	128	A
Гоит	DC output current	Output in High state	-64	mA
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C

## **RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	2.5V RANG	GE LIMITS	3.3V RANG	UNIT	
STWIDOL	FARAMETER	MIN	MAX	MIN	MAX	UNII
V <sub>CC</sub>	DC supply voltage	2.3	2.7	3.0	3.6	V
VI	Input voltage	0	5.5	0	5.5	V
$V_{IH}$	High-level input voltage	1.7		2.0		V
$V_{IL}$	Input voltage		0.7		0.8	V
I <sub>OH</sub>	High-level output current		-8		-12	mA
I <sub>OL</sub>	Low-level output current		12		12	mA
Δt/Δν	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	-40	+85	°C

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

<sup>3.</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with $30\Omega$ termination resistors (3-State)

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DC ELECTRICAL CHARACTERISTICS (3.3V  $\pm$  0.3V RANGE)

					LIMITS		
				MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	$V_{CC} = 3.0V; I_{IK} = -18mA$			-0.85	-1.2	V
\/	High-level output voltage	$V_{CC} = 3.0 \text{ to } 3.6\text{V}; I_{OH} = -100\mu\text{A}$		V <sub>CC</sub> -0.2	V <sub>CC</sub>		V
V <sub>OH</sub>	High-level output voltage	$V_{CC} = 3.0V; I_{OH} = -32mA$		2.0	2.3		\ \
		$V_{CC} = 3.0V; I_{OL} = 100\mu A$			0.07	0.2	
\/	Low-level output voltage	V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA			0.25	0.4	V
$V_{OL}$	Low-level output voltage	$V_{CC} = 3.0V; I_{OL} = 32mA$			0.3	0.5	\ \ \
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 64mA			0.4	0.55	
V <sub>RST</sub>	Power-up output low voltage <sup>6</sup>	$V_{CC} = 3.6V; I_{O} = 1mA; V_{I} = V_{CC} \text{ or GNE}$	)			0.55	V
		$V_{CC} = 3.6V$ ; $V_I = V_{CC}$ or GND	Control pins		0.1	±1	
	Innut lands an assument	$V_{CC} = 0 \text{ or } 3.6V; V_I = 5.5V$			0.1	10	
ł <sub>l</sub>	Input leakage current	$V_{CC} = 3.6V; V_{I} = V_{CC}$	Data nino4	1	0.5	1	μΑ
		$V_{CC} = 3.6V; V_{I} = 0V$	Data pins <sup>4</sup>		0.1	-5	
I <sub>OFF</sub>	Off current	$V_{CC} = 0V; V_{I} \text{ or } V_{O} = 0 \text{ to } 4.5V$			0.1	±100	μΑ
	Bus Hold current	$V_{CC} = 3V; V_{I} = 0.8V$		75	130		
$I_{HOLD}$		$V_{CC} = 3V; V_{I} = 2.0V$		-75	-140		μΑ
	Data inputs <sup>7</sup>	$V_{CC} = 0V \text{ to } 3.6V; V_{CC} = 3.6V$		±500			
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V			10	125	μА
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	$V_{CC} \le 1.2V$ ; $V_O = 0.5V$ to $V_{CC}$ ; $V_I = GN$ OE/OE = Don't care	D or V <sub>CC</sub>		1	±100	μА
I <sub>OZH</sub>	3-State output High current	$V_{CC} = 3.6V; V_{O} = 3.0V; V_{I} = V_{IL} \text{ or } V_{IH}$			0.5	5	μА
I <sub>OZL</sub>	3-State output Low current	$V_{CC} = 3.6V; V_{O} = 0.5V; V_{I} = V_{IL} \text{ or } V_{IH}$			0.5	-5	μΑ
I <sub>CCH</sub>		$V_{CC} = 3.6V$ ; Outputs High, $V_I = GND$ or $V_{CC}$ , $I_{O} = 0$			0.07	0.1	
I <sub>CCL</sub>	Quiescent supply current	$V_{CC} = 3.6V$ ; Outputs Low, $V_I = GND$ or $V_{CC}$ , $I_{O} = 0$			5.1	7	m/
I <sub>CCZ</sub>	1	V <sub>CC</sub> = 3.6V; Outputs Disabled; V <sub>I</sub> = GN	D or $V_{CC}$ , $I_{O} = 0^5$	1	0.07	0.1	
Δl <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	$V_{CC}$ = 3V to 3.6V; One input at $V_{CC}$ -0.6 Other inputs at $V_{CC}$ or GND	SV,		0.04	0.4	mΑ

 All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
 This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND
 This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 3.3V ± 0.2V a transition time of 100 $\mu$ sec is permitted. This parameter is valid for  $T_{amb} = 25$ °C only.

4. Unused pins at V<sub>CC</sub> or GND.

- 5. I<sub>CCZ</sub> is measured with outputs pulled up to V<sub>CC</sub> or pulled down to ground.
  6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- 7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V  $\pm$  0.3V RANGE) GND = 0V;  $t_R=t_F=2.5 ns;~C_L=50 pF;~R_L=500\Omega;~T_{amb}=-40 ^{\circ}C~to~+85 ^{\circ}C.$ 

SYMBOL	PARAMETER	WAVEFORM		T <sub>amb</sub> = -40 to +85°C V <sub>CC</sub> = +3.3V		
			MIN	TYP	MAX	
f <sub>MAX</sub>	Maximum clock frequency	1	150			MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nCP to nQx	1	1.0 1.0	3.2 3.2	5.0 4.7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High and Low level	3 4	1.0 0.5	3.4 2.3	5.6 3.7	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High and Low level	3 4	1.5 1.5	3.7 3.0	5.4 4.3	ns

<sup>1.</sup> All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25$ °C.

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

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# AC SETUP REQUIREMENTS (3.3V $\pm 0.3V$ RANGE) GND = 0V, $t_R = t_F = 2.5 ns, \, C_L = 50 pF, \, R_L = 500 \Omega$

			LIN	IITS	
SYMBOL	PARAMETER	WAVEFORM	T <sub>amb</sub> = -40 to +85°C V <sub>CC</sub> = +3.3V ±0.3V		UNIT
			MIN	TYP	
t <sub>S</sub> (H) t <sub>S</sub> (L)	Setup time, High or Low nDx to nCP	1	1.5 1.5	0.1 0.1	ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low nDx to nCP	2	0.5 0.5	0.1 0.1	ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	nCP pulse width High or Low	2	1.5 1.5		ns

## DC ELECTRICAL CHARACTERISTICS (2.5V $\pm$ 0.2V RANGE)

		TEST CONDITIONS			LIMITS		
SYMBOL	PARAMETER			Temp = -40°C to		+85°C	UNIT
				MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	$V_{CC} = 2.3V; I_{IK} = -18mA$			-0.85	-1.2	V
V	High-level output voltage	$V_{CC} = 2.3 \text{ to } 3.6\text{V}; I_{OH} = -100\mu\text{A}$		V <sub>CC</sub> -0.2	V <sub>CC</sub>		V
V <sub>OH</sub>	I light-level output voltage	$V_{CC} = 2.3V; I_{OH} = -8mA$		1.8	2.1		ľ
		$V_{CC} = 2.3V; I_{OL} = 100 \mu A$			0.07	0.2	
$V_{OL}$	Low-level output voltage	$V_{CC} = 2.3V; I_{OL} = 24mA$			0.3	0.5	V
		$V_{CC} = 2.3V; I_{OL} = 8mA$				0.4	
V <sub>RST</sub>	Power-up output low voltage <sup>7</sup>	$V_{CC} = 2.7V$ ; $I_O = 1mA$ ; $V_I = V_{CC}$ or GND				0.55	V
		$V_{CC} = 2.7V$ ; $V_I = V_{CC}$ or GND	Control pins		0.1	±1	
I.	Input leakage current	$V_{CC} = 0 \text{ or } 2.7V; V_1 = 5.5V$			0.1	10	μΑ
Η	Imput leakage current	$V_{CC} = 2.7V; V_{I} = V_{CC}$	Data pins <sup>4</sup>		0.1	1	
		$V_{CC} = 2.7V; V_I = 0$	Data piris		0.1	-5	
I <sub>OFF</sub>	Off current	$V_{CC} = 0V$ ; $V_{I}$ or $V_{O} = 0$ to 4.5V			0.1	±100	μΑ
I <sub>HOLD</sub>	Bus Hold current	$V_{CC} = 2.3V; V_I = 0.7V$			90		μΑ
	Data inputs <sup>6</sup>	$V_{CC} = 2.3V; V_I = 1.7V$			-10		μΑ
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 2.3V			10	125	μА
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	$V_{CC} \le 1.2V$ ; $V_O = 0.5V$ to $V_{CC}$ ; $V_I = GNDOE/OE = Don't$ care	or V <sub>CC</sub>		1	±100	μА
I <sub>OZH</sub>	3-State output High current	$V_{CC} = 2.7V; V_{O} = 2.3V; V_{I} = V_{IL} \text{ or } V_{IH}$			0.5	5	μΑ
I <sub>OZL</sub>	3-State output Low current	$V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} \text{ or } V_{IH}$			0.5	<b>-</b> 5	μΑ
I <sub>CCH</sub>		$V_{CC} = 2.7V$ ; Outputs High, $V_I = GND$ or $V_{CC}$ , $I_{O} = 0$			0.04	0.1	
I <sub>CCL</sub>	Quiescent supply current	$V_{CC}$ = 2.7V; Outputs Low, $V_I$ = GND or $V_{CC}$ , $I_{O}$ = 0			2.3	4.5	mA
I <sub>CCZ</sub>		$V_{CC} = 2.7V$ ; Outputs Disabled; $V_I = GND$	or $V_{CC}$ , $I_{O} = 0^5$		0.04	0.1	
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	$V_{CC}$ = 2.3V to 2.7V; One input at $V_{CC}$ -0. Other inputs at $V_{CC}$ or GND	6V,		0.04	0.4	mA

### NOTES:

- All typical values are at V<sub>CC</sub> = 2.5V and T<sub>amb</sub> = 25°C.
   This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND
- 3. This parameter is valid for any  $V_{CC}$  between 0V and 1.2V with a transition time of up to 10msec. From  $V_{CC}$  = 1.2V to  $V_{CC}$  = 2.5V  $\pm$  0.3V a transition time of 100 $\mu$ sec is permitted. This parameter is valid for  $T_{amb}$  = 25°C only.
- 4. Unused pins at V<sub>CC</sub> or GND.
- 5. I<sub>CCZ</sub> is measured with outputs pulled up to V<sub>CC</sub> or pulled down to ground.
  6. Not guaranteed.
- 7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

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AC CHARACTERISTICS (2.5V  $\pm$  0.2V RANGE) GND = 0V;  $t_R = t_F = 2.5 ns; \ C_L = 50 pF; \ R_L = 500 \Omega; \ T_{amb} = -40 ^{\circ} C$  to +85  $^{\circ} C.$ 

SYMBOL PARAMETER		WAVEFORM	T <sub>ar</sub>	UNIT		
			MIN	TYP	MAX	
f <sub>MAX</sub>	Maximum clock frequency	1	150			MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nCP to nQx	1	1.0 1.0	4.4 3.8	7.0 6.4	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High and Low level	3 4	1.5 1.0	4.6 2.8	7.5 4.6	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High and Low level	3 4	1.5 1.0	3.5 3.7	5.5 5.7	ns

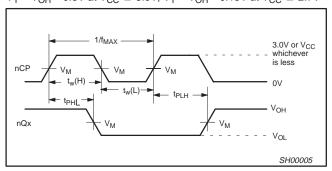
NOTE:

# AC SETUP REQUIREMENTS (2.5V $\pm$ 0.2V RANGE) GND = 0V, $t_R=t_F=2.5 ns,\, C_L=50 pF,\, R_L=500\Omega$

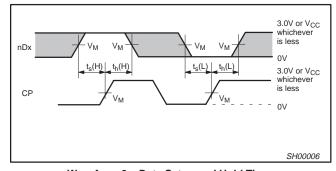
			LIN	NITS	
SYMBOL	PARAMETER	WAVEFORM T <sub>am</sub>		$T_{amb}$ = -40 to +85°C $V_{CC}$ = +2.5 ±0.2V	
			MIN	TYP	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low nDx to nCP	1	1.5 2.0	0.1 0.5	ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low nDx to nCP	2	0.3 0.5	-0.5 -0.1	ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	nCP pulse width High or Low	2	1.5 1.5		ns

## **AC WAVEFORMS**

 $V_M$  = 1.5V at  $V_{CC}$  ≥ 3.0V;  $V_M$  =  $V_{CC}/2$  at  $V_{CC}$  ≤ 2.7V  $V_X$  =  $V_{OL}$  + 0.3V at  $V_{CC}$  ≥ 3.0V;  $V_X$  =  $V_{OL}$  + 0.15V at  $V_{CC}$  ≤ 2.7V  $V_Y$  =  $V_{OH}$  - 0.3V at  $V_{CC}$  ≥ 3.0V;  $V_Y$  =  $V_{OH}$  - 0.15V at  $V_{CC}$  ≤ 2.7V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock frequency

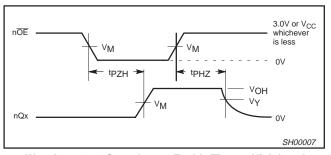


Waveform 2. Data Setup and Hold Times

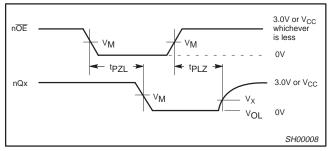
<sup>1.</sup> All typical values are at  $V_{CC}$  = 3.3V and  $T_{amb}$  = 25°C.

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

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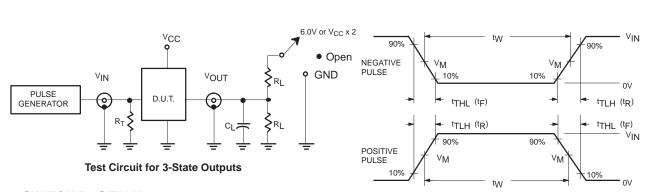


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

# **TEST CIRCUIT AND WAVEFORM**



### **SWITCH POSITION**

TEST	SWITCH
t <sub>PLZ</sub> /t <sub>PZL</sub>	6V or V <sub>CC x 2</sub>
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

### **DEFINITIONS**

 $R_L$  = Load resistor; see AC CHARACTERISTICS for value.

C<sub>L</sub> = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS								
PAWILT	Amplitude	Rep. Rate	$t_{\text{VV}}$	t <sub>R</sub>	t <sub>F</sub>				
74ALVT16	3.0V or V <sub>CC</sub> whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns				

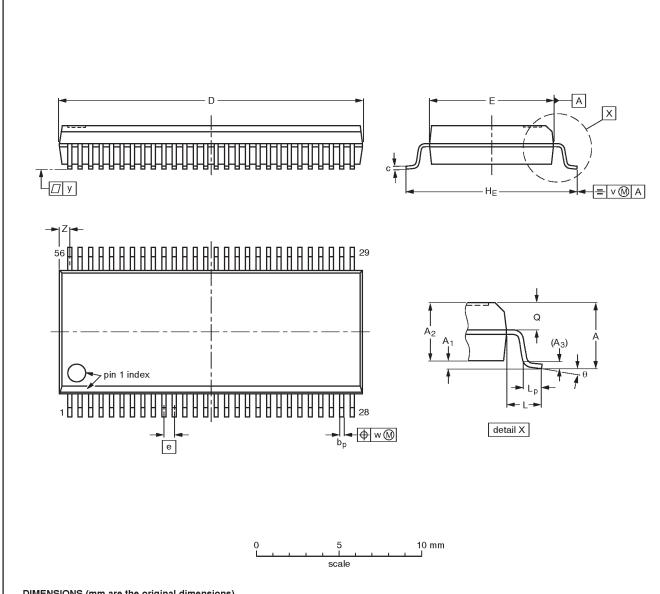
SW00025

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

74ALVT162821

# SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



### DIMENSIONS (mm are the original dimensions)

UNIT	A max.	Α <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	рb	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

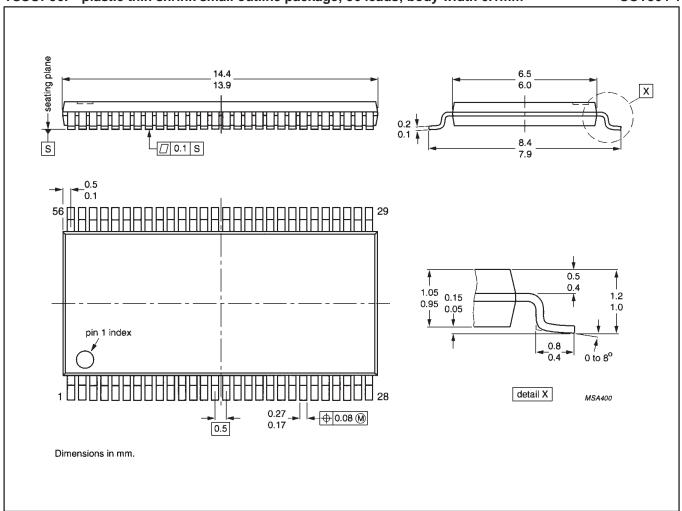
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT371-1		MO-118AB				<del>93-11-02</del> 95-02-04

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

74ALVT162821

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with  $30\Omega$  termination resistors (3-State)

74ALVT162821

#### Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

<sup>[1]</sup> Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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