INTEGRATED CIRCUITS



Product specification Supersedes data of 2000 Mar 14 IC24 Data Handbook 2000 Jun 20



74ALVC162835A

56 GND

55

54

53 GND

52

50 V_{CC}

49

48

47

46

45

44

43

42

41

40

39 GND

38

37

36

35 V_{CC}

34

33

32 GND

31

30 CP

29 GND

NC

 A_1

 A_2 51

A₃

 A_4

 A_5

A₆

A₇

A₈

A₉

A₁₀

A₁₁

A₁₂

A₁₃

A₁₄

 A_{15}

A₁₆

A₁₇

A₁₈

SH00188

GND

PIN CONFIGURATION

NC

NC 2

Y₁ 3

 Y_2 5

 Y_3 6

V_{CC} 7

> Y_4 8

 Y_5 9

 Y_6

Y₇

Y9 14

Y₁₀ 15

Y₁₁ 16

GND

Y₁₃

Y₁₄ 20

Y₁₅

V_{CC}

Y₁₆

Y₁₇ 24

GND 25

Y₁₈ 26

OE 27

1 F 28

GND 11

10

12

13 Y₈

17 Y₁₂

18

19

21

22

23

GND 4

1

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 12 mA at 3.0 V
- MULTIBYTETM flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50 Ω transmission lines @ 85°C
- Integrated 30 Ω termination resistors
- Diode clamps to V_{CC} and GND on all inputs
- Input diodes to accommodate strong drivers

DESCRIPTION

The 74ALVC162835A is an 18-bit universal bus driver. Data flow is controlled by output enable (OE), latch enable (LE) and clock inputs (CP).

When LE is HIGH, the A to Y data flow is transparent. When LE is LOW and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP the A-data is stored in the latch/flip-flop.

The 74ALVC162835A is designed with 30 Ω _series resistors in both HIGH or LOW output stages.

When \overline{OE} is LOW the outputs are active. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the latch/flip -flop.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

QUICK REFERENCE DATA

GND = 0 V. $T_{omb} = 25^{\circ}C$. $t_r = t_f < 2.5 ns$

SYMBOL	PARAMETER	CONDITIO	NS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay An to Yn; LE to Yn; CP to Yn	$V_{CC} = 3.3 \text{ V}, C_{L} = 50 \text{ pF}$	2.9 3.5 3.3	ns	
f _{max}	Maximum clock frequency	V _{CC} = 3.3 V, C _L = 50 pF	240	MHz	
Cl	Input capacitance			4.0	pF
C _{I/O}	Input/Output capacitance				pF
C	Dower dissinction conscitutes per buffer	V = CND to V = 1	transparent mode Output enabled Output disabled	10 3	n F
C _{PD}	Power dissipation capacitance per buffer	$V_I = GND$ to V_{CC}^1	Clocked mode Output enabled Output disabled	21 15	pF

NOTES:

 C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o}) \text{ where: } f_{i} = \text{input frequency in MHz; } C_{L} = \text{output load capacitance in pF;}$

 f_0 = output frequency in MHz; V_{CC} = supply voltage in V; Σ ($C_L \times V_{CC}^2 \times f_0$) = sum of outputs.

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ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74ALVC162835A DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 55	NC	No connection
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	Y_1 to Y_{18}	Data outputs
4, 11, 18, 25, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage
27	ŌĒ	Output enable input (active LOW)
28	LE	Latch enable input (active HIGH)
30	CP	Clock input
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	A_1 to A_{18}	Data inputs

LOGIC SYMBOL



TYPICAL INPUT (DATA OR CONTROL)



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LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

	INPUTS					
OE	LE	СР	Α	Y		
Н	Х	Х	Х	Z		
L	Н	Х	L	L		
L	Н	Х	Н	Н		
L	L	\uparrow	L	L		
L	L	\uparrow	Н	Н		
L	L	Н	Х	Y ₀ 1		
L	L	L	Х	Y ₀ ²		

HIGH voltage level Н =

L = LOW voltage level

Don't care =

X Z ↑ = High impedance "off" state

LOW-to-HIGH level transition =

NOTES:

1. Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.

2. Output level before the indicated steady-state input conditions were established.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	
V _{CC}	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	V
	DC supply voltage (for low-voltage applications)	1	1.2	3.6	1
VI	DC Input voltage range		0	V _{CC}	V
Vo	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _r , t _f	Input rise and fall times	$V_{CC} = 2.3 \text{ to } 3.0 \text{V}$ $V_{CC} = 3.0 \text{ to } 3.6 \text{V}$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	$V_1 \pm 0$	-50	mA
VI	DC input voltage	Note 1	-0.5 to +4.6	V
Ι _{ΟΚ}	DC output diode current	$V_O > V_{CC} \text{ or } V_O \pm 0$	±50	mA
V _O	DC output voltage	Note 1	–0.5 to V _{CC} +0.5	V
Ι _Ο	DC output source or sink current	$V_{O} = 0$ to V_{CC}	±50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		±100	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package –plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

				LIMITS		
SYMBOL	PARAMETER	TEST CONDITIONS		Temp = -40°C to +85°C		
			MIN	TYP ¹	MAX	1
M		V _{CC} = 2.3 to 2.7V	1.7	1.2		V
VIH	HIGH level Input voltage	V _{CC} = 2.7 to 3.6V	2.0	1.5		1 ^v
M		V _{CC} = 2.3 to 2.7V		1.2	0.7	v
VIL	LOW level Input voltage	V _{CC} = 2.7 to 3.6V		1.5	0.8	1 [×]
		V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL} ; I_O = -100 μ A	V _{CC} -0.2	V _{CC}		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL} ; I_O = -4mA	V _{CC} -0.4	V _{CC} -0.11		1
		V_{CC} = 2.3V; V_{I} = V_{IH} or V_{IL} ; I_{O} = -6mA	V _{CC} -0.6	V _{CC} -0.17		1
V _{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL} ; I_O = -4mA	$V_{CC}-0.5$	$V_{CC} - 0.09$		V
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL} ; I_O = -8mA	V _{CC} -0.7	V _{CC} -0.19]
		V_{CC} = 3.0V; V_{I} = V_{IH} or V_{IL} ; I_{O} = -6mA	$V_{CC}-0.6$	V _{CC} -0.13]
		V_{CC} = 3.0V; V_{I} = V_{IH} or $V_{IL;}$ I_{O} = $-12mA$	V _{CC} -1.0	$V_{CC} - 0.27$		
		V_{CC} = 2.3 to 3.6V; $~V_{I}$ = V_{IH} or $V_{IL};~I_{O}$ = 100 μA		GND	0.20	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL} ; I_O = 4mA		0.07	0.40	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL} ; I_O = 6mA		0.11	0.55	
V _{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL} ; I_O = 4mA		0.06	0.40	V
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL} ; I_O = 8mA		0.13	0.60	
		V_{CC} = 3.0V; V_{I} = V_{IH} or $V_{IL;}$ I_{O} = 6mA		0.09	0.55	
		V_{CC} = 3.0V; V_{I} = V_{IH} or $V_{IL;}$ I_{O} = 12mA		0.19	0.80	
l _i	Input leakage current	V_{CC} = 2.3 to 3.6V; V_1 = V_{CC} or GND		0.1	5	μ/
I _{OZ}	3-State output OFF-state current			0.1	10	μA
I _{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; V_{I} = V_{CC} or GND; I_{O} = 0		0.2	40	μ/
ΔI_{CC}	Additional quiescent supply current	$V_{CC} = 2.3V$ to 3.6V; $V_{I} = V_{CC} - 0.6V$; $I_{O} = 0$		150	750	μA

NOTES:

1. All typical values are at $T_{amb} = 25^{\circ}C$.

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AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

 $GND = 0V; \, t_r = t_f \leq 2.0ns; \, C_L = 30pF$

				LIMITS			
SYMBOL	PARAMETER	WAVEFORM	V	UNIT			
		MIN TYP ¹		TYP ¹	MAX	1	
	Propagation delay An to Yn	1, 7	1.0	3.5	5.0		
t _{PHL} /t _{PLH}	Propagation delay LE to Yn	2, 7	1.3	4.1	5.9	ns	
	Propagation delay CP to Yn	4, 7	1.4	4.0	6.3]	
t _{PZH} /t _{PZL}	3-State output enable time OE to Yn	6, 7	1.4	3.8	6.3 ns		
t _{PHZ} /t _{PLZ}	3-State output disable time OE to Yn	6, 7	1.0	2.6	4.9	ns	
	CP pulse width HIGH or LOW	4, 7	3.3	1.0	-		
t _W	LE pulse width HIGH	2, 7	3.3	0.7	-	ns	
	Set-up time An to CP	5, 7	1.0	-	-		
t _{SU}	Set-up time An to LE	3, 7	1.5	-	-	ns	
	Hold time An to CP	5, 7	1.0	0.4	-	20	
t _h	Hold time An to LE	3, 7	0.5	0.1	-	ns	
f _{max}	Maximum clock pulse frequency	4, 7	150	190	-	MHz	

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \le 2.5$ ns; $C_L = 50$ pF

				LIMITS			LIMITS			
SYMBOL	PARAMETER WAVEFOR		V_{CC} = 3.3 \pm 0.3V			V _{CC} = 2.7V				
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX]	
	Propagation delay An to Yn	1, 7	1.0	2.9	4.2	1.0	3.3	5.0		
t _{PHL} /t _{PLH}	Propagation delay LE to Yn	2, 7	1.3	3.4	5.1	1.3	3.8	5.8	ns	
	Propagation delay CP to Yn	4, 7	1.4	3.3	5.4	1.4	3.7	6.1	1	
t _{PZH} /t _{PZL}	3-State output enable time OE to Yn	6, 7	1.1	3.4	5.5	1.1	4.0	6.5	ns	
t _{PHZ} /t _{PLZ}	3-State output disable time OE to Yn	6, 7	1.3	3.0	4.5	1.3	3.2	4.9	ns	
4	CP pulse width HIGH or LOW	4, 7	3.3	0.7	-	3.3	1.2	-		
t _W	LE pulse width HIGH	2, 7	3.3	0.6	-	3.3	0.6	-	ns	
	Set-up time An to CP	5, 7	1.0	-	-	1.0	-	-		
t _{SU}	Set-up time An to LE	3, 7	1.5	-	-	1.5	-	-	ns	
	Hold time An to CP	5, 7	0.9	0.7	-	1.2	0.4	-		
t _h	Hold time An to LE	3, 7	1.0	0.4	-	1.0	0.1	-	ns	
f _{max}	Maximum clock pulse frequency	4, 7	150	240	-	150	190	-	MHz	

NOTES:

1. All typical values are measured $T_{amb} = 25^{\circ}C$. 2. Typical value is measured at $V_{CC} = 3.3V$.

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AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

 $\label{eq:VM} \begin{array}{l} V_M = 1.5 \ V \\ V_X = V_{OL} + 0.3 V \\ V_Y = V_{OH} - 0.3 V \\ V_{OL} \ \text{and} \ V_{OH} \ \text{are the typical output voltage drop that occur with the output load.} \\ V_I = 2.7 V \end{array}$

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

 $V_{M} = 0.5 V_{CC} \\ V_{X} = V_{OL} + 0.15V \\ V_{Y} = V_{OH} - 0.15V \\ \end{cases}$

 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load. $V_{I} = V_{CC}$



Waveform 1. Input (An) to output (Yn) propagation delay



Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays.



Waveform 3. Data set-up and hold times for the An input to the LE input







Waveform 5. Data set-up and hold times for the An input to the clock CP input



Waveform 6. 3-State enable and disable times

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Product specification

TEST CIRCUIT



Waveform 7. Load circuitry for switching times

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Limiting values definition - Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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