DATA SHEET

74AHC1G125; 74AHCT1G125
Bus buffer/line driver; 3-state

Product specification
Supersedes data of 2002 Mar 22

2002 Jun 06

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FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 1000 V.
- Low power dissipation
- Balanced propagation delays
- Very small 5-pin package
- Output capability: standard
- Specified from –40 to +125 °C.

DESCRIPTION

The 74AHC1G/AHCT1G125 is a high-speed Si-gate CMOS device.

The 74AHC1G/AHCT1G125 provides one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input ($\overline{OE}$). A HIGH at $\overline{OE}$ causes the output to assume a high-impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC1G	AHCT1G	
t_{PHL}/t_{PLH}	propagation delay A to Y	C_L = 15 pF; V_{CC} = 5 V	3.4	3.4	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	9	11	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don’t care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGES				
		PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC1G125GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	AM
74AHCT1G125GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	CM
74AHC1G125GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	A25
74AHCT1G125GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	C25

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}$	output enable input
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V_{CC}	supply voltage

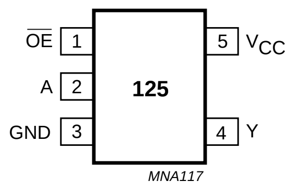


Fig.1 Pin configuration.

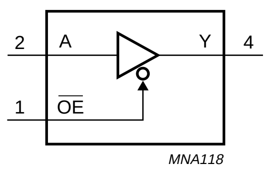


Fig.2 Logic symbol.

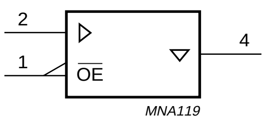


Fig.3 IEC logic symbol.

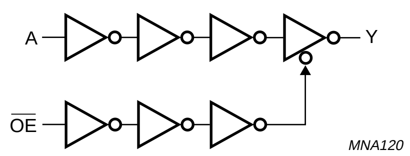


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC1G			74AHCT1G			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 3.3 ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 ±0.5 V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < –0.5 V	–	–20	mA
I_{OK}	output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	output source or sink current	–0.5 V < V_O < V_{CC} + 0.5 V	–	±25	mA
I_{CC}	V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C	–	250	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Family 74AHC1G

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	V
			5.5	3.85	–	–	3.85	–	3.85	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	V
			5.5	–	–	1.65	–	1.65	–	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -50\ \mu A$	2.0	1.9	2.0	–	1.9	–	1.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -50\ \mu A$	3.0	2.9	3.0	–	2.9	–	2.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -50\ \mu A$	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -4.0$ mA	3.0	2.58	–	–	2.48	–	2.40	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 50\ \mu A$	2.0	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 50\ \mu A$	3.0	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 50\ \mu A$	4.5	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	3.0	–	–	0.36	–	0.44	–	0.55	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I_{OZ}	3-state OFF-state current	$V_I = V_{CC}$ or GND	5.5	–	–	0.25	–	2.5	–	10	μA
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	–	2.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	1.0	–	10	–	40	μA
C_I	input capacitance			–	1.5	10	–	10	–	10	pF

Family 74AHCT1G

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -50\ \mu A$	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 50\ \mu A$	4.5	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I_{OZ}	3-state OFF-state current	$V_I = V_{CC}$ or GND	5.5	–	–	0.25	–	2.5	–	10	μA
I_{LI}	input leakage current	$V_I = V_{IH}$ or V_{IL}	5.5	–	–	0.1	–	1.0	–	2.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	1.0	–	10	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = 3.4$ V; other inputs at V_{CC} or GND; $I_O = 0$	5.5	–	–	1.35	–	1.5	–	1.5	mA
C_I	input capacitance			–	1.5	10	–	10	–	10	pF

AC CHARACTERISTICS

Type 74AHC1G125

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L (pF)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 3.0 to 3.6 V; note 1											
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 7	15	–	4.7	8.0	1.0	9.5	1.0	11.5	ns
t_{PZH}/t_{PZL}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	15	–	5.0	8.0	1.0	9.5	1.0	11.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	15	–	6.0	9.7	1.0	11.5	1.0	12.5	ns
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 7	50	–	6.6	11.5	1.0	13.0	1.0	14.5	ns
t_{PZH}/t_{PZL}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	50	–	6.9	11.5	1.0	13.0	1.0	14.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	50	–	8.3	13.2	1.0	15.0	1.0	16.5	ns
V_{CC} = 4.5 to 5.5 V; note 2											
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 7	15	–	3.4	5.5	1.0	6.5	1.0	7.0	ns
t_{PZH}/t_{PZL}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	15	–	3.6	5.1	1.0	6.0	1.0	6.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	15	–	4.1	6.8	1.0	8.0	1.0	8.5	ns
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 7	50	–	4.8	7.5	1.0	8.5	1.0	9.5	ns
t_{PZH}/t_{PZL}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	50	–	4.9	7.5	1.0	8.5	1.0	9.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	50	–	5.7	8.8	1.0	10.0	1.0	11.0	ns

Notes

1. All typical values are measured at V_{CC} = 3.3 V.
2. All typical values are measured at V_{CC} = 5.0 V.

Type 74AHCT1G125

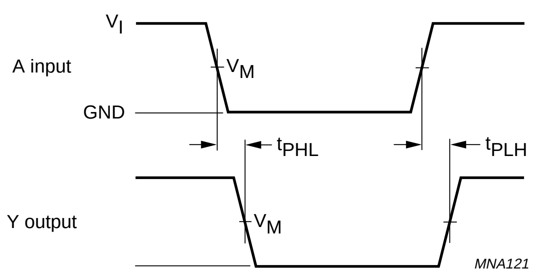
GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L (pF)	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 4.5 to 5.5 V; note 1											
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 7	15	–	3.4	5.5	1.0	6.5	1.0	7.0	ns
t_{PZH}/t_{PZL}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	15	–	3.9	5.1	1.0	6.0	1.0	6.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	15	–	4.5	6.8	1.0	8.0	1.0	8.5	ns
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 7	50	–	4.8	7.5	1.0	8.5	1.0	9.5	ns
t_{PZH}/t_{PZL}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	50	–	5.1	7.5	1.0	8.5	1.0	9.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $\overline{OE}$ to Y	see Figs 6 and 7	50	–	6.1	8.8	1.0	10.0	1.0	11.0	ns

Note

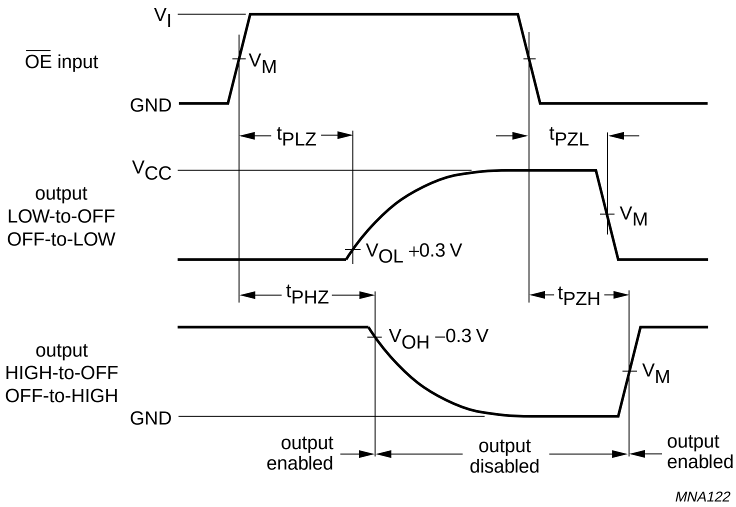
1. All typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS



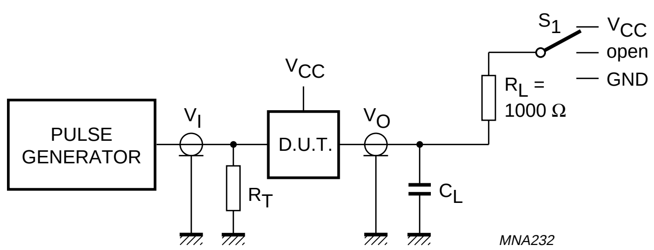
FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC1G	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT1G	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.5 The input (A) to output (Y) propagation delays.



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC1G	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT1G	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.6 The 3-state enable and disable times.



TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance (see Chapter “AC characteristics”).

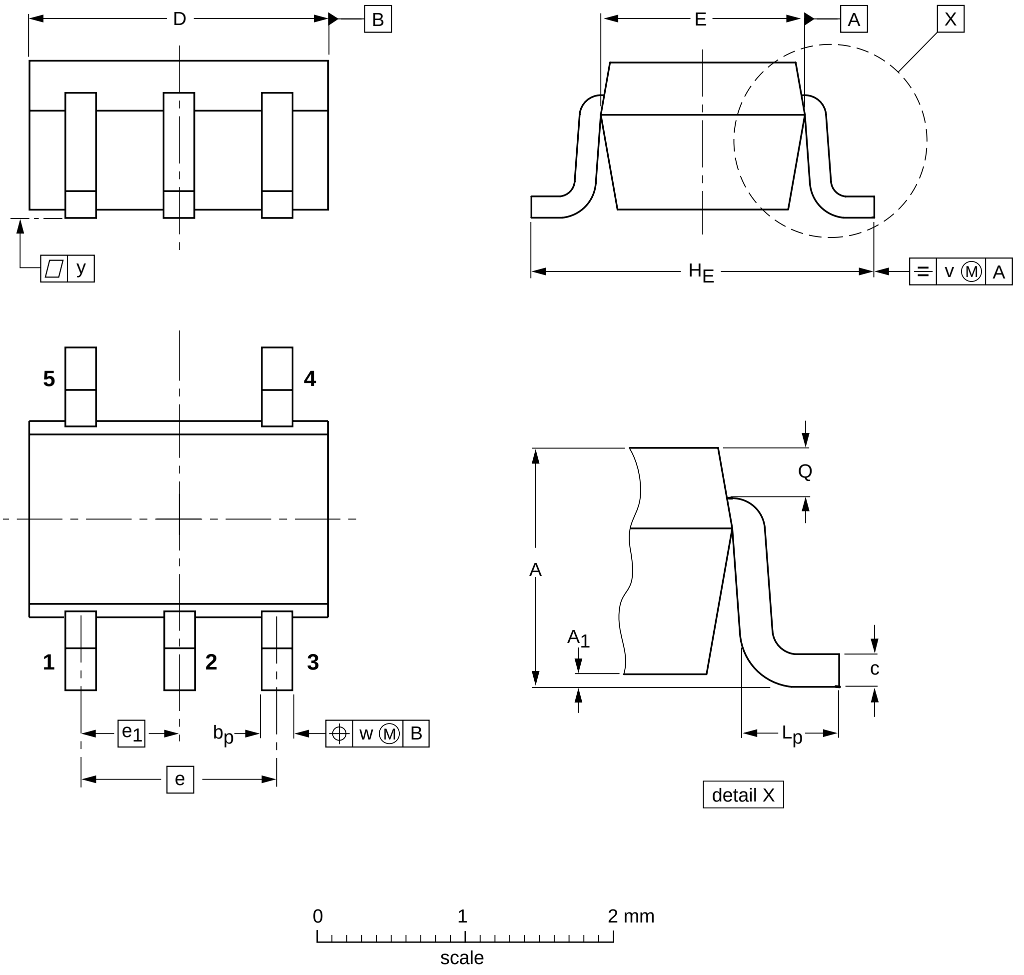
R_L = load resistance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads **SOT353**

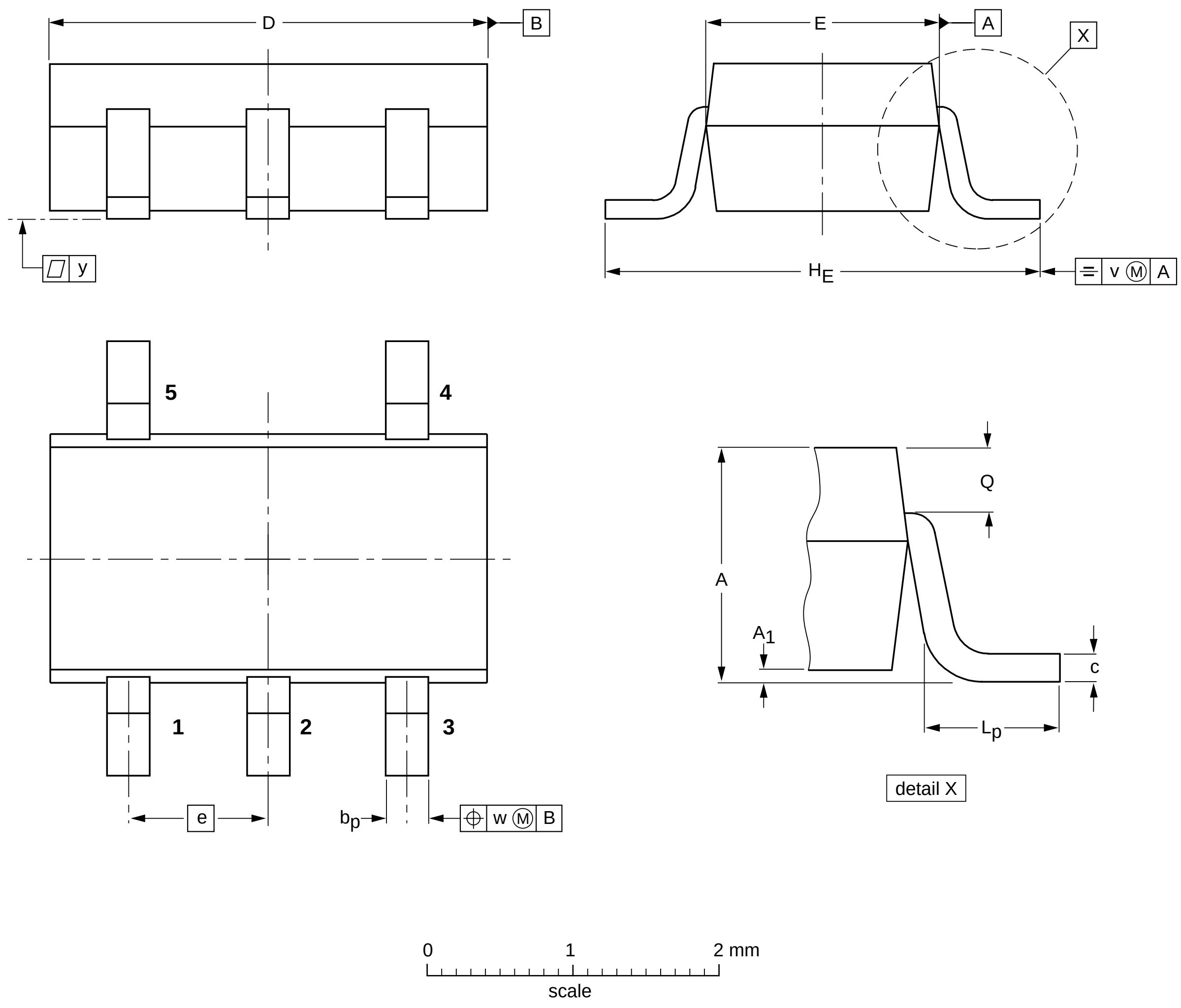


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Plastic surface mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *“(LF)BGA Application Note*” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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