

# DATA SHEET

**74ABT16501A**

**74ABTH16501A**

**18-bit universal bus transceiver (3-State)**

Product specification  
Supersedes data of 1997 Jun 12  
IC23 Data Handbook

1998 Feb 27

# 18-bit universal bus transceiver (3-State)

**74ABT16501A**  
**74ABTH16501A**

## FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- 74ABTH16501A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Positive edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Flexible operation permits 18 embedded D-type latches or flip-flops to operate in clocked, transparent, and latched modes.

## DESCRIPTION

The 74ABT16501A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and OEBA), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses  $\overline{\text{OEBA}}$ , LEBA and CPBA. The output enables are complimentary (OEAB is active High, and  $\overline{\text{OEBA}}$  is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Two options are available, 74ABT16501A which does not have the bus-hold feature and 74ABTH16501A which incorporates the bus-hold feature.

## QUICK REFERENCE DATA

| SYMBOL                               | PARAMETER                                 | CONDITIONS<br>$T_{\text{amb}} = 25^{\circ}\text{C}$ ; GND = 0V    | TYPICAL    | UNIT          |
|--------------------------------------|-------------------------------------------|-------------------------------------------------------------------|------------|---------------|
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation delay<br>An to Bn or Bn to An | $C_L = 50\text{pF}$ ;<br>$V_{\text{CC}} = 5\text{V}$              | 2.2<br>1.8 | ns            |
| $C_{\text{IN}}$                      | Input capacitance (Control pins)          | $V_I = 0\text{V}$ or $V_{\text{CC}}$                              | 3          | pF            |
| $C_{\text{I/O}}$                     | I/O pin capacitance                       | Outputs disabled; $V_{\text{I/O}} = 0\text{V}$ or $V_{\text{CC}}$ | 7          | pF            |
| $I_{\text{CCZ}}$                     | Quiescent supply current                  | Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$                   | 500        | $\mu\text{A}$ |
| $I_{\text{CCL}}$                     |                                           | Outputs low; $V_{\text{CC}} = 5.5\text{V}$                        | 9          | mA            |

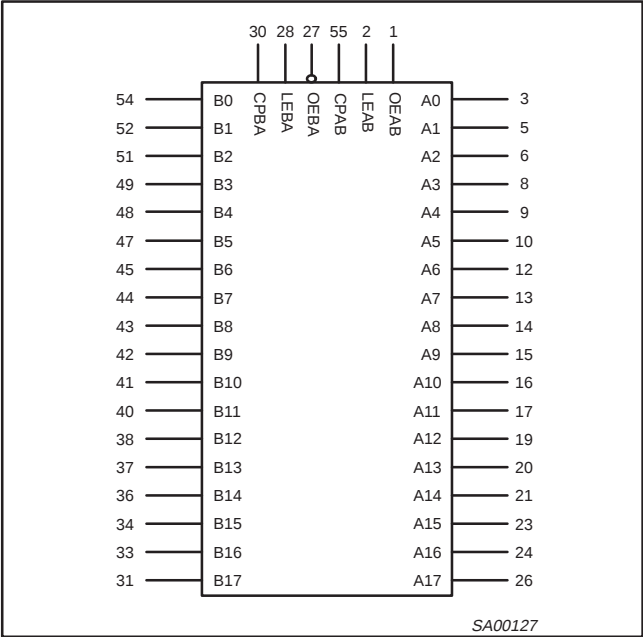
## ORDERING INFORMATION

| PACKAGES                     | TEMPERATURE RANGE                              | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|------------------------------------------------|-----------------------|---------------|------------|
| 56-Pin Plastic SSOP Type III | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 74ABT16501A DL        | BT16501A DL   | SOT371-1   |
| 56-Pin Plastic TSSOP Type II | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 74ABT16501A DGG       | BT16501A DGG  | SOT364-1   |
| 56-Pin Plastic SSOP Type III | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 74ABTH16501A DL       | BH16501A DL   | SOT371-1   |
| 56-Pin Plastic TSSOP Type II | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 74ABTH16501A DGG      | BH16501A DGG  | SOT364-1   |

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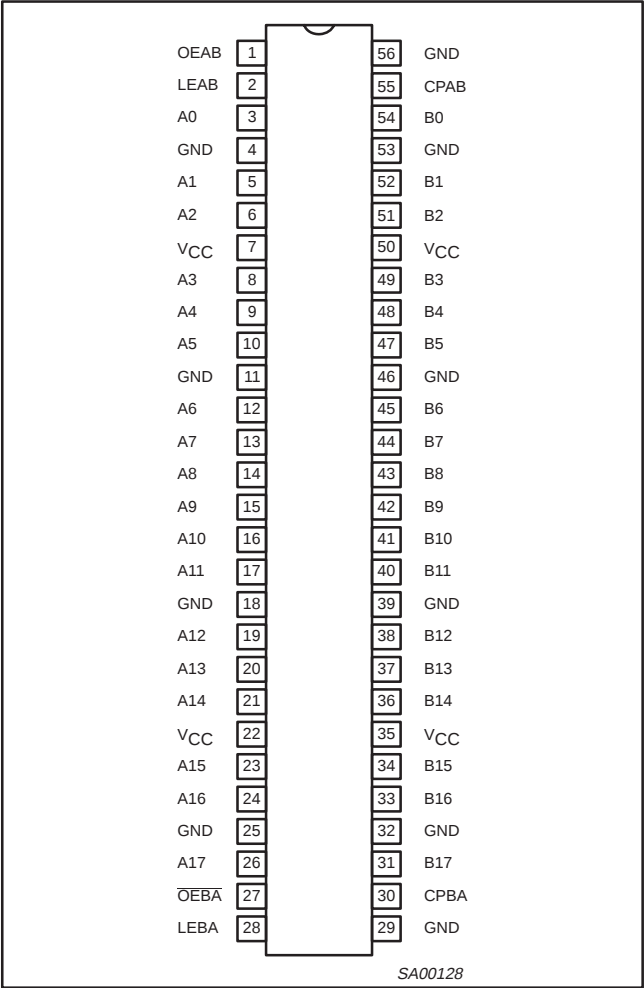
LOGIC SYMBOL



PIN DESCRIPTION

| PIN NUMBER                                                             | SYMBOL                   | NAME AND FUNCTION                              |
|------------------------------------------------------------------------|--------------------------|------------------------------------------------|
| 1                                                                      | OEAB                     | A-to-B Output enable input                     |
| 27                                                                     | $\overline{\text{OEBA}}$ | B-to-A Output enable input (active low)        |
| 2, 28                                                                  | LEAB/LEBA                | A-to-B/B-to-A Latch enable input               |
| 55,30                                                                  | CPAB/CPBA                | A-to-B/B-to-A Clock input (active rising edge) |
| 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26      | A0-A17                   | Data inputs/outputs (A side)                   |
| 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31 | B0-B17                   | Data inputs/outputs (B side)                   |
| 4, 11, 18, 25, 32, 39, 46, 53                                          | GND                      | Ground (0V)                                    |
| 7, 22, 35, 50                                                          | V <sub>CC</sub>          | Positive supply voltage                        |

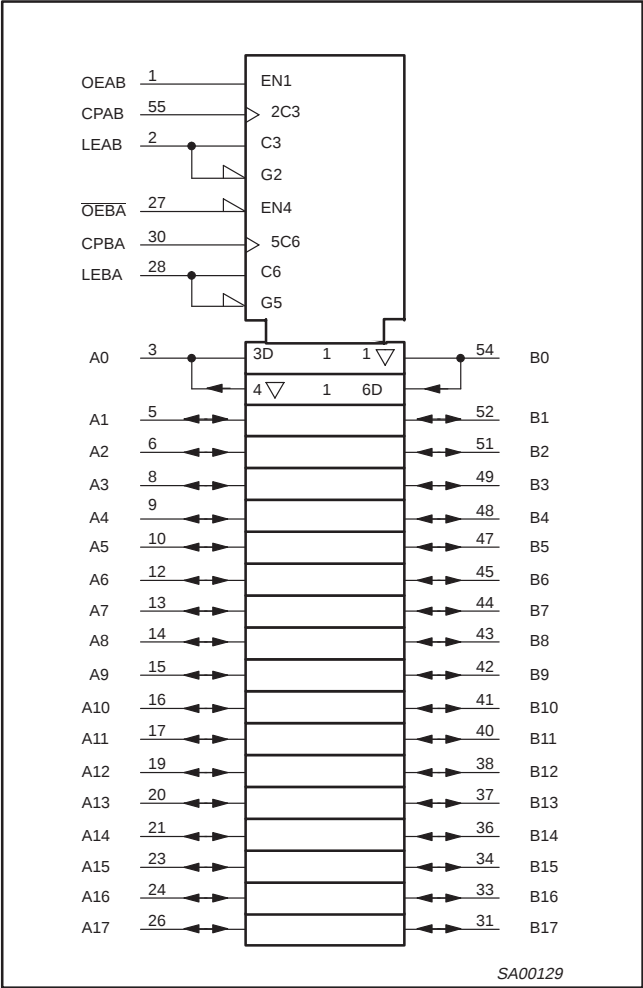
PIN CONFIGURATION



18-bit universal bus transceiver (3-State)

74ABT16501A  
74ABTH16501A

LOGIC SYMBOL (IEEE/IEC)



## 18-bit universal bus transceiver (3-State)

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## FUNCTION TABLE

| INPUTS |      |        |    | Internal Registers | OUTPUTS | OPERATING MODE       |
|--------|------|--------|----|--------------------|---------|----------------------|
| OEAB   | LEAB | CPAB   | An |                    | Bn      |                      |
| L      | H    | X      | X  | X                  | Z       | Disabled             |
| L      | ↓    | X      | h  | H                  | Z       | Disabled, Latch data |
| L      | ↓    | X      | l  | L                  | Z       |                      |
| L      | L    | H or L | X  | NC                 | Z       | Disabled, Hold data  |
| L      | L    | ↑      | h  | H                  | Z       | Disabled, Clock data |
| L      | L    | ↑      | l  | L                  | Z       |                      |
| H      | H    | X      | H  | H                  | H       | Transparent          |
| H      | H    | X      | L  | L                  | L       |                      |
| H      | ↓    | X      | h  | H                  | H       | Latch data & display |
| H      | ↓    | X      | l  | L                  | L       |                      |
| H      | L    | ↑      | h  | H                  | H       | Clock data & display |
| H      | L    | ↑      | l  | L                  | L       |                      |
| H      | L    | H or L | X  | H                  | H       | Hold data & display  |
| H      | L    | H or L | X  | L                  | L       |                      |

**NOTE:** A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{\text{OEBA}}$ , LEBA, and CPBA.

H = High voltage level

h = High voltage level one set-up time prior to the Enable or Clock transition

L = Low voltage level

l = Low voltage level one set-up time prior to the Enable or Clock transition

NC= No Change

X = Don't care

Z = High Impedance "off" state

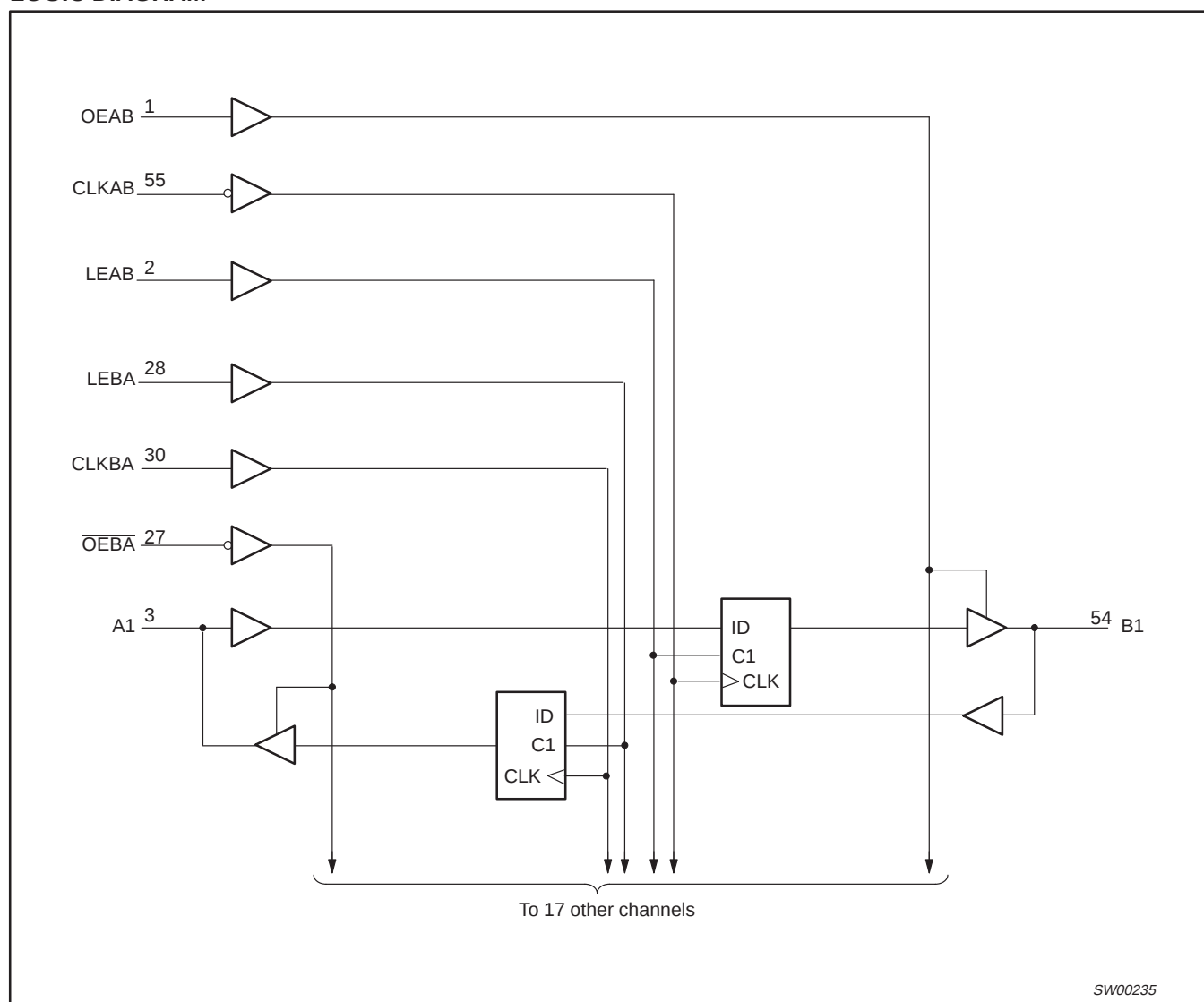
↓ = High-to-Low Enable or Clock transition

↑ = Low-to-High Clock transition

## 18-bit universal bus transceiver (3-State)

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## LOGIC DIAGRAM



## 18-bit universal bus transceiver (3-State)

74ABT16501A  
74ABTH16501AABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

| SYMBOL    | PARAMETER                      | CONDITIONS                  | RATING       | UNIT |
|-----------|--------------------------------|-----------------------------|--------------|------|
| $V_{CC}$  | DC supply voltage              |                             | −0.5 to +7.0 | V    |
| $I_{IK}$  | DC input diode current         | $V_I < 0$                   | −18          | mA   |
| $V_I$     | DC input voltage <sup>3</sup>  |                             | −1.2 to +7.0 | V    |
| $I_{OK}$  | DC output diode current        | $V_O < 0$                   | −50          | mA   |
| $V_{OUT}$ | DC output voltage <sup>3</sup> | Output in Off or High state | −0.5 to +5.5 | V    |
| $I_{OUT}$ | DC output current              | Output in Low state         | 128          | mA   |
|           |                                | Output in High state        | −64          |      |
| $T_{stg}$ | Storage temperature range      |                             | −65 to +150  | °C   |

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL              | PARAMETER                                           | LIMITS |          | UNIT |
|---------------------|-----------------------------------------------------|--------|----------|------|
|                     |                                                     | MIN    | MAX      |      |
| $V_{CC}$            | DC supply voltage                                   | 4.5    | 5.5      | V    |
| $V_I$               | Input voltage                                       | 0      | $V_{CC}$ | V    |
| $V_{IH}$            | High-level input voltage                            | 2.0    |          | V    |
| $V_{IL}$            | Input voltage                                       |        | 0.8      | V    |
| $I_{OH}$            | High-level output current                           |        | −32      | mA   |
| $I_{OL}$            | Low-level output current                            |        | 64       | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate; Outputs enabled |        | 10       | ns/V |
| $T_{amb}$           | Operating free-air temperature range                | −40    | +85      | °C   |

## 18-bit universal bus transceiver (3-State)

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74ABTH16501A

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL                             | PARAMETER                                                         | TEST CONDITIONS                                                                                                                           |              | LIMITS                   |       |      |                                   |      | UNIT |
|------------------------------------|-------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------------------|-------|------|-----------------------------------|------|------|
|                                    |                                                                   |                                                                                                                                           |              | T <sub>amb</sub> = +25°C |       |      | T <sub>amb</sub> = -40°C to +85°C |      |      |
|                                    |                                                                   |                                                                                                                                           |              | MIN                      | TYP   | MAX  | MIN                               | MAX  |      |
| V <sub>IK</sub>                    | Input clamp voltage                                               | V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA                                                                                           |              |                          | -0.8  | -1.2 |                                   | -1.2 | V    |
| V <sub>OH</sub>                    | High-level output voltage                                         | V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                                       |              | 2.5                      | 2.9   |      | 2.5                               |      | V    |
|                                    |                                                                   | V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                                       |              | 3.0                      | 4.0   |      | 3.0                               |      | V    |
|                                    |                                                                   | V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                                      |              | 2.0                      | 2.4   |      | 2.0                               |      | V    |
| V <sub>OL</sub>                    | Low-level output voltage                                          | V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                                       |              |                          | 0.35  | 0.55 |                                   | 0.55 | V    |
| V <sub>RST</sub>                   | Power-up output voltage <sup>3</sup>                              | V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>                                                     |              |                          | 0.13  | 0.55 |                                   | 0.55 | V    |
| I <sub>I</sub>                     | Input leakage current                                             | V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V                                                                                      | Control pins |                          | ±0.01 | ±1.0 |                                   | ±1.0 | μA   |
| I <sub>HOLD</sub>                  | Bus Hold current A and B ports <sup>5</sup> 74ABTH16501A          | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0.8V                                                                                             |              | 35                       |       |      | 35                                |      | μA   |
|                                    |                                                                   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 2.0V                                                                                             |              | -75                      |       |      | -75                               |      |      |
|                                    |                                                                   | V <sub>CC</sub> = 5.5V; V <sub>I</sub> = 0 to 5.5V                                                                                        |              | ±800                     |       |      |                                   |      |      |
| I <sub>OFF</sub>                   | Power-off leakage current                                         | V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V                                                                           |              |                          | ±2    | ±100 |                                   | ±100 | μA   |
| I <sub>PU/PD</sub>                 | Power-up/down 3-State output current <sup>4</sup>                 | V <sub>CC</sub> = 2.1V; V <sub>O</sub> = 0.0V or V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = Don't care |              |                          | ±2    | ±50  |                                   | ±50  | μA   |
| I <sub>IH</sub> + I <sub>OZH</sub> | 3-State output High current                                       | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                                        |              |                          | 1.0   | 10   |                                   | 10   | μA   |
| I <sub>IL</sub> + I <sub>OZL</sub> | 3-State output Low current                                        | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.0V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                                        |              |                          | -1.0  | -10  |                                   | -10  | μA   |
| I <sub>CEX</sub>                   | Output High leakage current                                       | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>                                                    |              |                          | 2.0   | 50   |                                   | 50   | μA   |
| I <sub>O</sub>                     | Output current <sup>1</sup>                                       | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V                                                                                             |              | -50                      | -80   | -180 | -50                               | -180 | mA   |
| I <sub>CCH</sub>                   | Quiescent supply current                                          | V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>                                                             |              |                          | 0.5   | 2    |                                   | 2    | mA   |
| I <sub>CCL</sub>                   |                                                                   | V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>                                                              |              |                          | 9     | 19   |                                   | 19   | mA   |
| I <sub>CCZ</sub>                   |                                                                   | V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>                                                          |              |                          | 0.5   | 2    |                                   | 2    | mA   |
| ΔI <sub>CC</sub>                   | Additional supply current per input pin <sup>2</sup> 74ABT16501A  | V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND                                                         |              |                          | 5.0   | 50   |                                   | 50   | μA   |
| ΔI <sub>CC</sub>                   | Additional supply current per input pin <sup>2</sup> 74ABTH16501A | V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND                                                         |              |                          | 200   | 500  |                                   | 500  | μA   |

## NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V<sub>CC</sub> between 0V and 2.1V, with a transition time of up to 10msec. From V<sub>CC</sub> = 2.1V to V<sub>CC</sub> = 5V ± 10% a transition time of up to 100μsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

## 18-bit universal bus transceiver (3-State)

74ABT16501A  
74ABTH16501A

## AC CHARACTERISTICS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

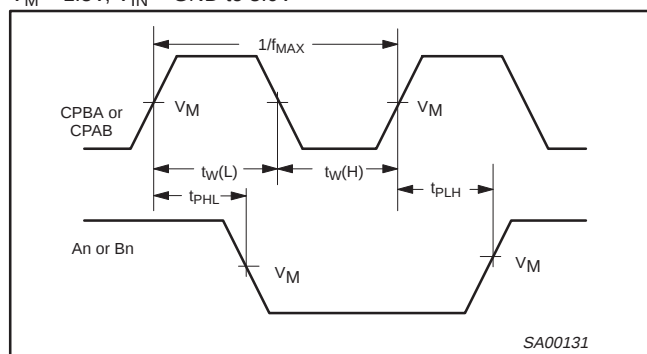
| SYMBOL                               | PARAMETER                                      | WAVEFORM | LIMITS                                              |            |            |                                                                  |            | UNIT |
|--------------------------------------|------------------------------------------------|----------|-----------------------------------------------------|------------|------------|------------------------------------------------------------------|------------|------|
|                                      |                                                |          | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V |            |            | T <sub>amb</sub> = −40 to +85°C<br>V <sub>CC</sub> = +5.0V ±0.5V |            |      |
|                                      |                                                |          | MIN                                                 | TYP        | MAX        | MIN                                                              | MAX        |      |
| f <sub>max</sub>                     | Maximum clock frequency                        | 1        | 150                                                 | 225        |            | 150                                                              |            | MHz  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>An to Bn or Bn to An      | 2        | 1.0<br>1.0                                          | 2.2<br>1.8 | 3.0<br>2.5 | 1.0<br>1.0                                                       | 3.5<br>3.0 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>LEAB to Bn or LEBA to An  | 3        | 1.5<br>1.4                                          | 3.2<br>2.9 | 4.3<br>3.8 | 1.5<br>1.4                                                       | 5.0<br>4.2 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CPAB to Bn or CPBA to An  | 1        | 1.6<br>1.4                                          | 3.5<br>2.9 | 4.5<br>3.8 | 1.6<br>1.4                                                       | 5.0<br>4.2 | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output enable time<br>to HIGH and LOW level    | 5<br>6   | 1.1<br>1.0                                          | 3.0<br>2.4 | 4.0<br>3.4 | 1.1<br>1.0                                                       | 4.7<br>3.9 | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output disable time<br>from HIGH and LOW level | 5<br>6   | 1.3<br>1.0                                          | 3.3<br>2.4 | 4.3<br>3.4 | 1.3<br>1.0                                                       | 5.3<br>3.9 | ns   |

## AC SETUP REQUIREMENTS

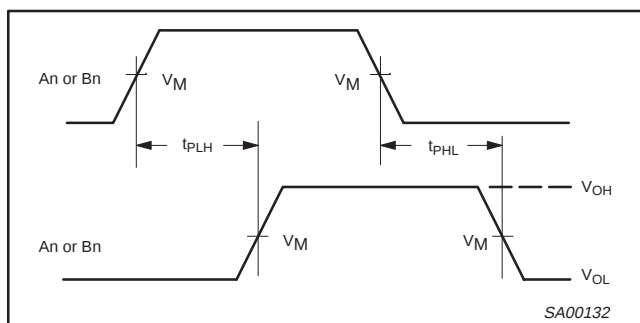
GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

| SYMBOL                             | PARAMETER                                           | WAVEFORM | LIMITS                                                                 |              |                                                                                                        | UNIT |
|------------------------------------|-----------------------------------------------------|----------|------------------------------------------------------------------------|--------------|--------------------------------------------------------------------------------------------------------|------|
|                                    |                                                     |          | $T_{\text{amb}} = +25^\circ\text{C}$<br>$V_{\text{CC}} = +5.0\text{V}$ |              | $T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$<br>$V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$ |      |
|                                    |                                                     |          | MIN                                                                    | TYP          | MIN                                                                                                    |      |
| $t_s(\text{H})$<br>$t_s(\text{L})$ | Setup time, HIGH or LOW<br>An to CPAB or Bn to CPBA | 4        | 2.0<br>2.0                                                             | 0.5<br>0.5   | 2.0<br>2.0                                                                                             | ns   |
| $t_h(\text{H})$<br>$t_h(\text{L})$ | Hold time, HIGH or LOW<br>An to CPAB or Bn to CPBA  | 4        | 0.7<br>0.7                                                             | -0.5<br>-0.5 | 0.7<br>0.7                                                                                             | ns   |
| $t_s(\text{H})$<br>$t_s(\text{L})$ | Setup time, HIGH or LOW<br>An to LEAB or Bn to LEBA | 4        | 2.0<br>2.0                                                             | 0.5<br>0.4   | 2.0<br>2.0                                                                                             | ns   |
| $t_h(\text{H})$<br>$t_h(\text{L})$ | Hold time HIGH or LOW<br>An to LEAB or Bn to LEBA   | 4        | 0.7<br>0.7                                                             | -0.4<br>-0.5 | 0.7<br>0.7                                                                                             | ns   |
| $t_w$                              | Pulse width, HIGH or LOW<br>CPAB or CPBA            | 1        | 3                                                                      | 1.9          | 3                                                                                                      | ns   |
| $t_w(\text{H})$                    | Pulse width, HIGH<br>LEAB or LEBA                   | 3        | 3                                                                      | 1.2          | 3                                                                                                      | ns   |

## AC WAVEFORMS

 $V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND to } 3.0\text{V}$ 

Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



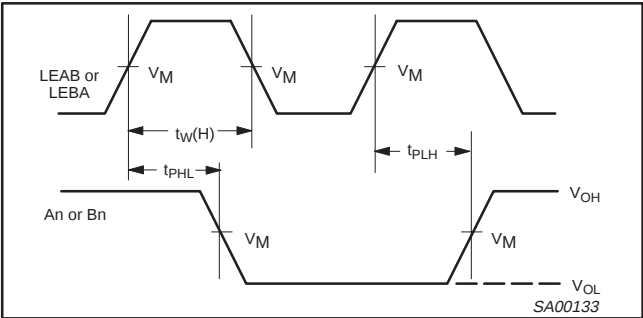
Waveform 2. Propagation Delay, Transparent Mode

18-bit universal bus transceiver (3-State)

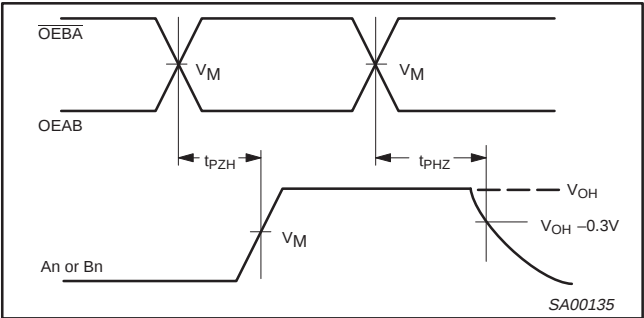
74ABT16501A  
74ABTH16501A

AC WAVEFORMS (Continued)

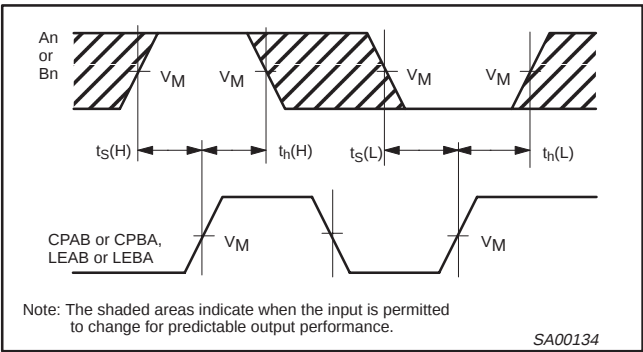
$V_M = 1.5V$ ,  $V_{IN} = GND$  to  $3.0V$



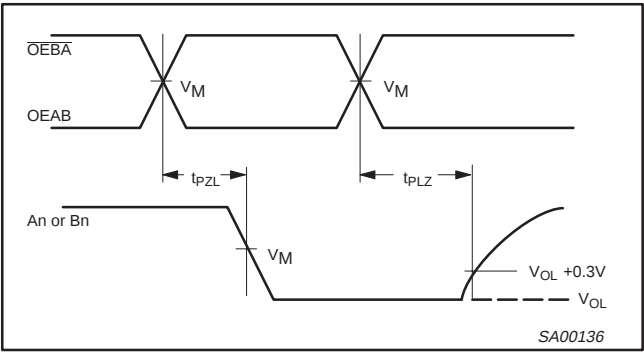
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. Data Setup and Hold Times



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

**SWITCH POSITION**

| TEST      | SWITCH |
|-----------|--------|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open   |

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

Input Pulse Definition

$V_M = 1.5V$

| FAMILY    | INPUT PULSE REQUIREMENTS |           |       |       |       |
|-----------|--------------------------|-----------|-------|-------|-------|
|           | Amplitude                | Rep. Rate | $t_W$ | $t_R$ | $t_F$ |
| 74ABT/H16 | 3.0V                     | 1MHz      | 500ns | 2.5ns | 2.5ns |

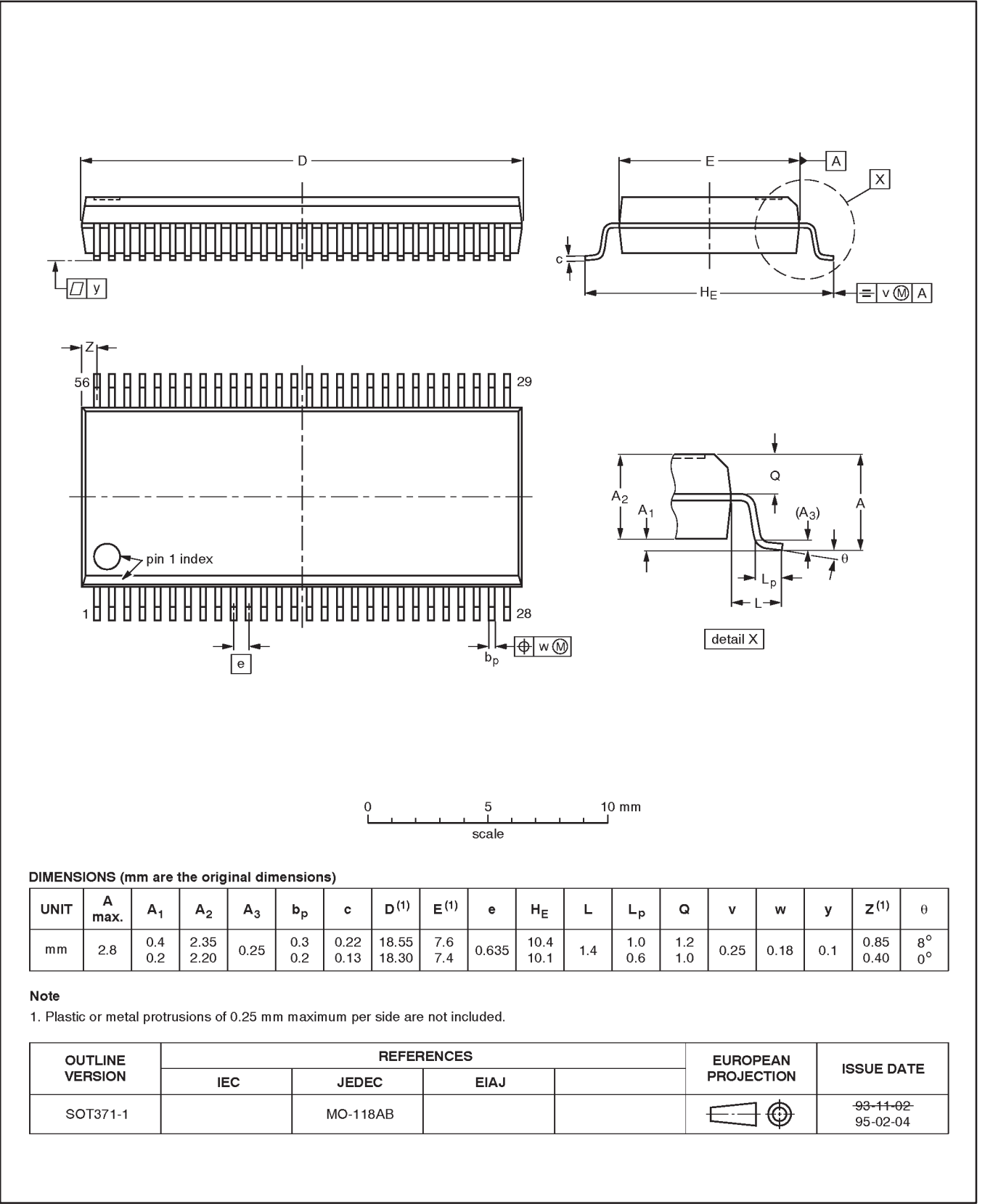
SA00018

18-bit universal bus transceiver (3-State)

74ABT16501A  
74ABTH16501A

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

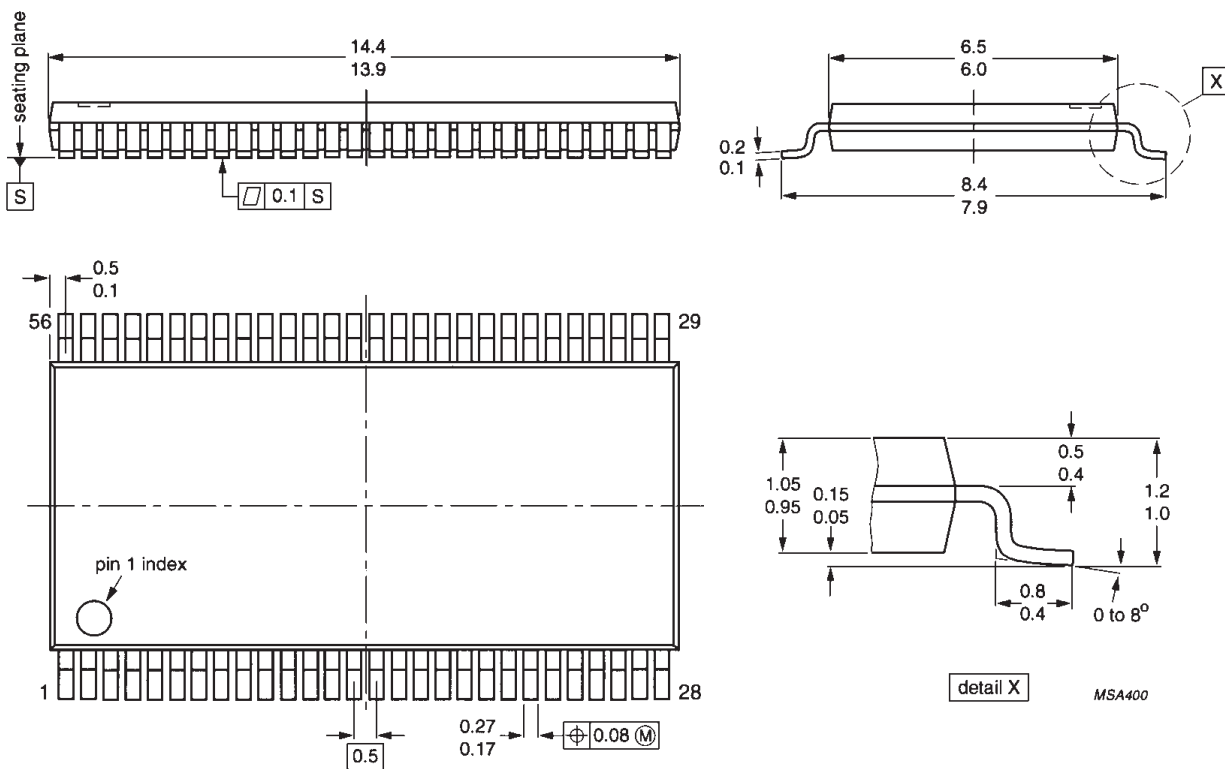


## 18-bit universal bus transceiver (3-State)

74ABT16501A  
74ABTH16501A

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



74ABT16501A  
74ABTH16501A

### Data sheet status

| Data sheet status         | Product status | Definition [1]                                                                                                                                                                                                                                             |
|---------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.                                                                                                          |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                       |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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