# CAT64LC10/20/40
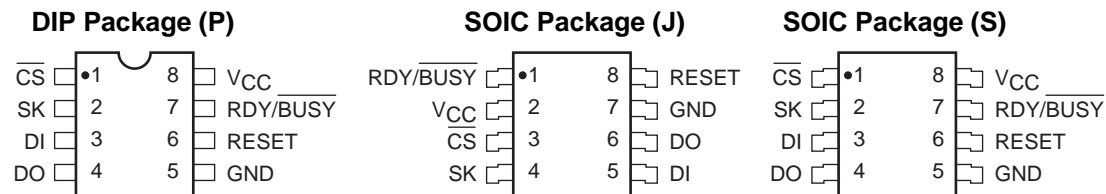
## 1K/2K/4K-Bit Serial E²PROM

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## FEATURES

- **SPI Bus Compatible**
- **Low Power CMOS Technology**
- **2.5V to 6.0V Operation**
- **Self-Timed Write Cycle with Auto-Clear**
- **Hardware Reset Pin**
- **Hardware and Software Write Protection**

- **Commercial and Industrial Temperature Ranges**
- **Power-Up Inadvertant Write Protection**
- **$\overline{RDY/BUSY}$ Pin for End-of-Write Indication**
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**

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## DESCRIPTION

The CAT64LC10/20/40 is a 1K/2K/4K-bit Serial E²PROM which is configured as 64/128/256 registers by 16 bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT64LC10/20/40 is manufactured using Catalyst's advanced CMOS E²PROM float-ing gate technology. It is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin DIP or SOIC packages.

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## PIN CONFIGURATION

**DIP Package (P)**

| | | |
|---|---|---|
| $\overline{CS}$ | 1 | 8 $V_{CC}$ |
| SK | 2 | 7 RDY/$\overline{BUSY}$ |
| DI | 3 | 6 RESET |
| DO | 4 | 5 GND |

**SOIC Package (J)**

| | | |
|---|---|---|
| RDY/$\overline{BUSY}$ | 1 | 8 RESET |
| $V_{CC}$ | 2 | 7 GND |
| $\overline{CS}$ | 3 | 6 DO |
| SK | 4 | 5 DI |

**SOIC Package (S)**

| | | |
|---|---|---|
| $\overline{CS}$ | 1 | 8 $V_{CC}$ |
| SK | 2 | 7 RDY/$\overline{BUSY}$ |
| DI | 3 | 6 RESET |
| DO | 4 | 5 GND |

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## PIN FUNCTIONS

| Pin Name | Function |
|---|---|
| $\overline{CS}$ | Chip Select |
| SK | Clock Input |
| DI | Serial Data Input |
| DO | Serial Data Output |
| $V_{CC}$ | +2.5V to +6.0V Power Supply |
| GND | Ground |
| RESET | Reset |
| RDY/$\overline{BUSY}$ | Ready/$\overline{BUSY}$ Status |

## BLOCK DIAGRAM
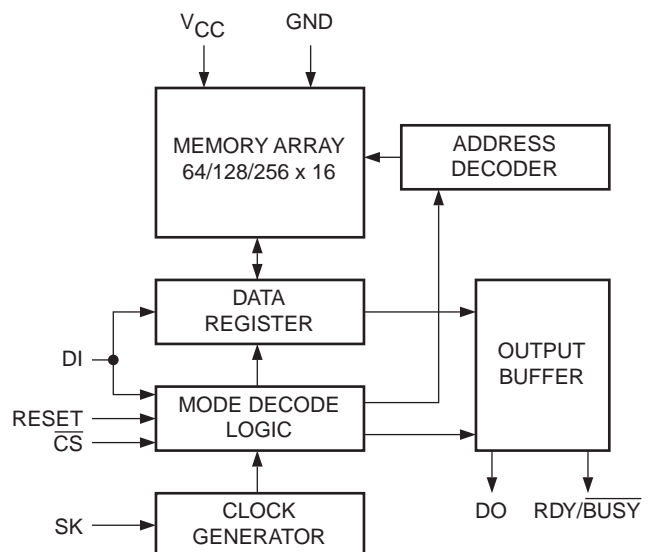


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## ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ................. −55°C to +125°C

Storage Temperature ...................... −65°C to +150°C

Voltage on any Pin with
  Respect to Ground[1] ........... −2.0V to +$V_{CC}$ +2.0V

$V_{CC}$ with Respect to Ground ............... −2.0V to +7.0V

Package Power Dissipation
  Capability (Ta = 25°C).................................. 1.0W

Lead Soldering Temperature (10 secs) ............ 300°C

Output Short Circuit Current[2] ........................ 100 mA

## *COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

### RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Min. | Max. | Units | Reference Test Method |
|--------|-----------|------|------|-------|----------------------|
| $N_{END}$[3] | Endurance | 1,000,000 | | Cycles/Byte | MIL-STD-883, Test Method 1033 |
| $T_{DR}$[3] | Data Retention | 100 | | Years | MIL-STD-883, Test Method 1008 |
| $V_{ZAP}$[3] | ESD Susceptibility | 2000 | | Volts | MIL-STD-883, Test Method 3015 |
| $I_{LTH}$[3][4] | Latch-Up | 100 | | mA | JEDEC Standard 17 |

### CAPACITANCE ($T_A$ = 25°C, f= 1.0 MHz, $V_{CC}$ =6.0V)

| Symbol | Test | Max. | Units | Conditions |
|--------|------|------|-------|-----------|
| $C_{I/O}$[3] | Input/Output Capacitance (DO, RDY/$\overline{BUSY}$) | 8 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$[3] | Input Capacitance ($\overline{CS}$, SK, DI, RESET) | 6 | pF | $V_{IN}$ = 0V |

Note:
(1) The minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is $V_{CC}$ +0.5V, which may overshoot to $V_{CC}$ +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1V to $V_{CC}$ +1V.

## D.C. OPERATING CHARACTERISTICS

$V_{CC}$ = +2.5V to +6.0V, unless otherwise specified.

| Sym. | Parameter | | Min. | Typ. | Max. | Units | Test Conditions |
|------|-----------|--|------|------|------|-------|-----------------|
| | | | **Limits** | | | | |
| $I_{CC}$ | Operating Current | 2.5V | | | 0.4 | mA | $f_{SK}$ = 250 kHz |
| | EWEN, EWDS, READ | 6.0V | | | 1 | mA | $f_{SK}$ = 1 MHz |
| $I_{CCP}$ | Program Current | 2.5V | | | 2 | mA | |
| | | 6.0V | | | 3 | mA | |
| $I_{SB}$[1] | Standby Current | | | | 0 | µA | $V_{IN}$ = GND or $V_{CC}$ $\overline{CS}$ = $V_{CC}$ |
| $I_{LI}$ | Input Leakage Current | | | | 2 | µA | $V_{IN}$ = GND to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | | | 10 | µA | $V_{OUT}$ = GND to $V_{CC}$ |
| $V_{IL}$ | Low Level Input Voltage, DI | | −0.1 | | $V_{CC}$ x 0.3 | V | |
| $V_{IH}$ | High Level Input Voltage, DI | | $V_{CC}$ x 0.7 | | $V_{CC}$ + 0.5 | V | |
| $V_{IL}$ | Low Level Input Voltage, $\overline{CS}$, SK, RESET | | −0.1 | | $V_{CC}$ x 0.2 | V | |
| $V_{IH}$ | High Level Input Voltage, $\overline{CS}$, SK, RESET | | $V_{CC}$ x 0.8 | | $V_{CC}$ + 0.5 | V | |
| $V_{OH}$[2] | High Level Output Voltage | 2.5V | $V_{CC}$ − 0.3 | | | V | $I_{OH}$ = −10µA |
| | | 6.0V | $V_{CC}$ − 0.3 | | | | $I_{OH}$ = −10µA |
| | | | 2.4 | | | | $I_{OH}$ = −400µA |
| $V_{OL}$[2] | Low Level Output Voltage | 2.5V | | | 0.4 | V | $I_{OL}$ = 10µA |
| | | 6.0V | | | 0.4 | V | $I_{OL}$ = 2.1mA |

Note:
(1) Standby Current ($I_{SB}$) = 0µA (<900nA) ____
(2) $V_{OH}$ and $V_{OL}$ spec applies to READY/BUSY pin also

## A.C. OPERATING CHARACTERISTICS

$V_{CC}$ = +2.5V to +6.0V, unless otherwise specified.

| Symbol | Parameter | | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{CSS}$ | $\overline{CS}$ Setup Time | | 100 | | | ns |
| $t_{CSH}$ | $\overline{CS}$ Hold Time | | 100 | | | ns |
| $t_{DIS}$ | DI Setup Time | | 200 | | | ns |
| $t_{DIH}$ | DI Hold Time | | 200 | | | ns |
| $t_{PD1}$ | Output Delay to 1 | | | | 300 | ns |
| $t_{PD0}$ | Output Delay to 0 | | | | 300 | ns |
| $t_{HZ}$[2] | Output Delay to High Impendance | | | | 500 | ns |
| $t_{CSMIN}$ | Minimum $\overline{CS}$ High Time | | 250 | | | ns |
| $t_{SKHI}$ | Minimum SK High Time | 2.5V | 1000 | | | ns |
| | | 4.5V–6.0V | 400 | | | |
| $t_{SKLOW}$ | Minimum SK Low Time | 2.5V | 1000 | | | ns |
| | | 4.5V–6.0V | 400 | | | |
| $t_{SV}$ | Output Delay to Status Valid | | | | 500 | ns |
| $f_{SK}$ | Maximum Clock Frequency | 2.5V | 250 | | | kHz |
| | | 4.5V–6.0V | 1000 | | | |
| $t_{RESS}$ | Reset to $\overline{CS}$ Setup Time | | 0 | | | ns |
| $t_{RESMIN}$ | Minimum RESET High Time | | 250 | | | ns |
| $t_{RESH}$ | RESET to READY Hold Time | | 0 | | | ns |
| $t_{RC}$ | Write Recovery | | 100 | | | ns |

## POWER-UP TIMING[1][3]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{PUR}$ | Power-Up to Read Operation | | 10 | μs |
| $t_{PUW}$ | Power-Up to Program Operation | | 1 | ms |

## WRITE CYCLE LIMIITS

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{WR}$ | Program Cycle Time | 2.5V | | 10 | ms |
| | | 4.5V–6.0V | | 5 | |

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
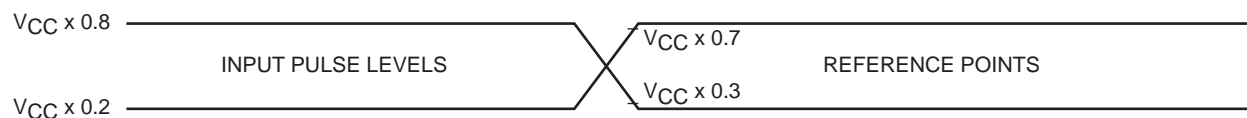(2) This parameter is sampled but not 100% tested.
(3) $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the specified operation can be initiated.

## INSTRUCTION SET

| Instruction | | Opcode | Address | Data |
|---|---|---|---|---|
| Read | 64LC10 | 10101000 | A5 A4 A3 A2 A1 A0 0 0 | D15 - D0 |
| | 64LC20 | 10101000 | A6 A5 A4 A3 A2 A1 A0 0 | D15 - D0 |
| | 64LC40 | 10101000 | A7 A6 A5 A4 A3 A2 A1 A0 | D15 - D0 |
| Write | 64LC10 | 10100100 | A5 A4 A3 A2 A1 A0 0 0 | D15 - D0 |
| | 64LC20 | 10100100 | A6 A5 A4 A3 A2 A1 A0 0 | D15 - D0 |
| | 64LC40 | 10100100 | A7 A6 A5 A4 A3 A2 A1 A0 | D15 - D0 |
| Write Enable | | 10100011 | X X X X X X X X | |
| Write Disable | | 10100000 | X X X X X X X X | |
| [Write All Locations][1] | | 10100001 | X X X X X X X X | D15–D0 |

## Figure 1. A.C. Testing Input/Output Waveform [2][3][4] ($C_L$ = 100 pF)



$V_{CC}$ x 0.8

$V_{CC}$ x 0.2

INPUT PULSE LEVELS

$V_{CC}$ x 0.7

$V_{CC}$ x 0.3

REFERENCE POINTS

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Note:
(1)  (Write All Locations) is a test mode operation and is therefore not included in the A.C./D.C. Operations specifications.
(2)  Input Rise and Fall Times (10% to 90%) < 10 ns.
(3)  Input Pulse Levels = $V_{CC}$ x 0.2 and $V_{CC}$ x 0.8.
(4)  Input and Output Timing Reference = $V_{CC}$ x 0.3 and $V_{CC}$ x 0.7.

## DEVICE OPERATION

The CAT64LC10/20/40 is a 1K/2K/4K-bit nonvolatile memory intended for use with all standard controllers. The CAT64LC10/20/40 is organized in a 64/128/256 x 16 format. All instructions are based on an 8-bit format. There are four 16-bit instructions: READ, WRITE, EWEN, and EWDS. The CAT64LC10/20/40 operates on a single power supply ranging from 2.5V to 6.0V and it has an on-chip voltage generator to provide the high voltage needed during a programming operation. Instructions, addresses and data to be written are clocked into the DI pin on the rising edge of the SK clock. The DO pin is normally in a high impedance state except when outputting data in a READ operation or outputting RDY/$\overline{BUSY}$ status when polled during a WRITE operation.

The format for all instructions sent to this device includes a 4-bit start sequence, 1010, a 4-bit op code and an 8-bit address field or dummy bits. For a WRITE operation,

### Figure 2. Sychronous Data Timing
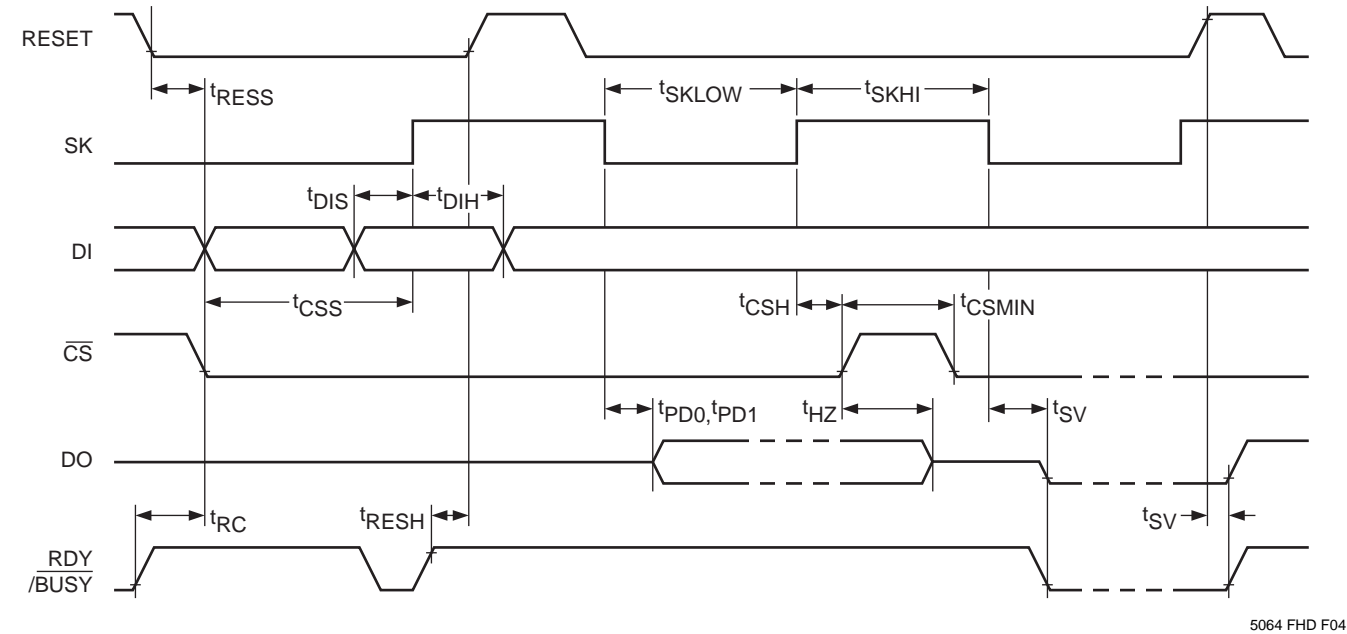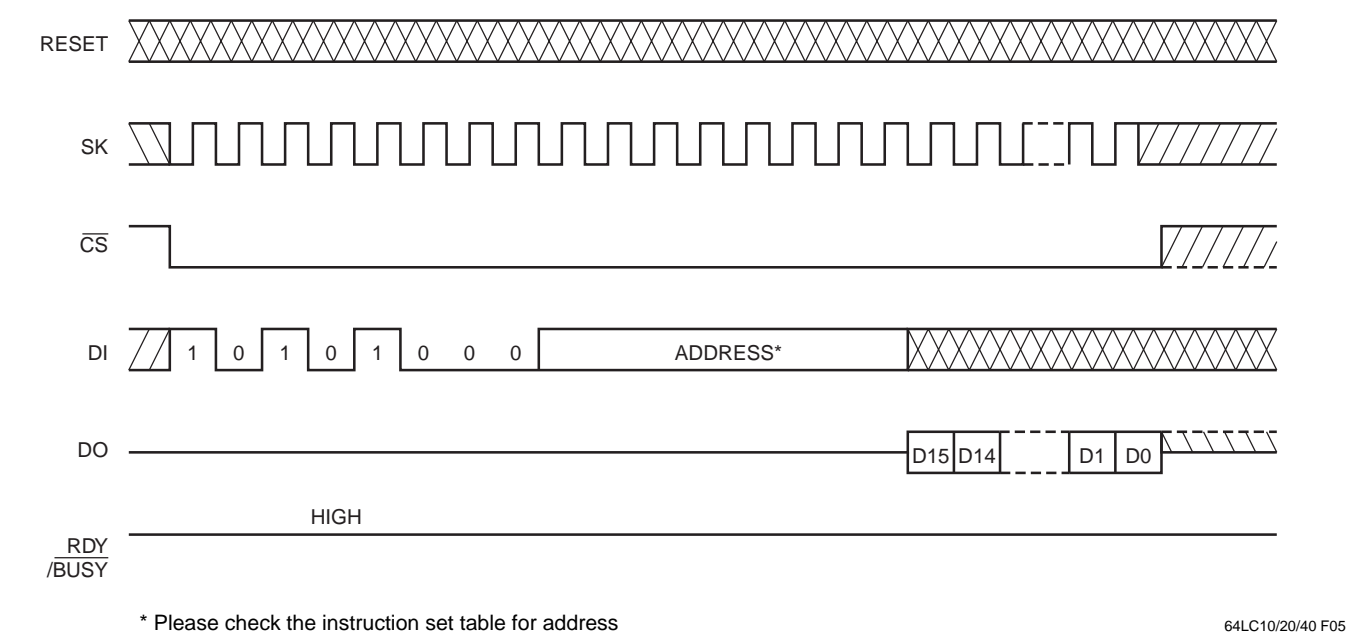


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### Figure 3. Read Instruction Timing



* Please check the instruction set table for address

a 16-bit data field is also required following the 8-bit address field.

The CAT64LC10/20/40 requires an active LOW $\overline{CS}$ in order to be selected. Each instruction must be preceded by a HIGH-to-LOW transition of $\overline{CS}$ before the input of the 4-bit start sequence. Prior to the 4-bit start sequence (1010), the device will ignore inputs of all other logical sequence.

**Read**

Upon receiving a READ command and address (clocked into the DI pin), the DO pin will output data one $t_{PD}$ after the falling edge of the 16th clock (the last bit of the address field). The READ operation is not affected by the RESET input.

**Write**

After receiving a WRITE op code, address and data, the device goes into the AUTO-Clear cycle and then the
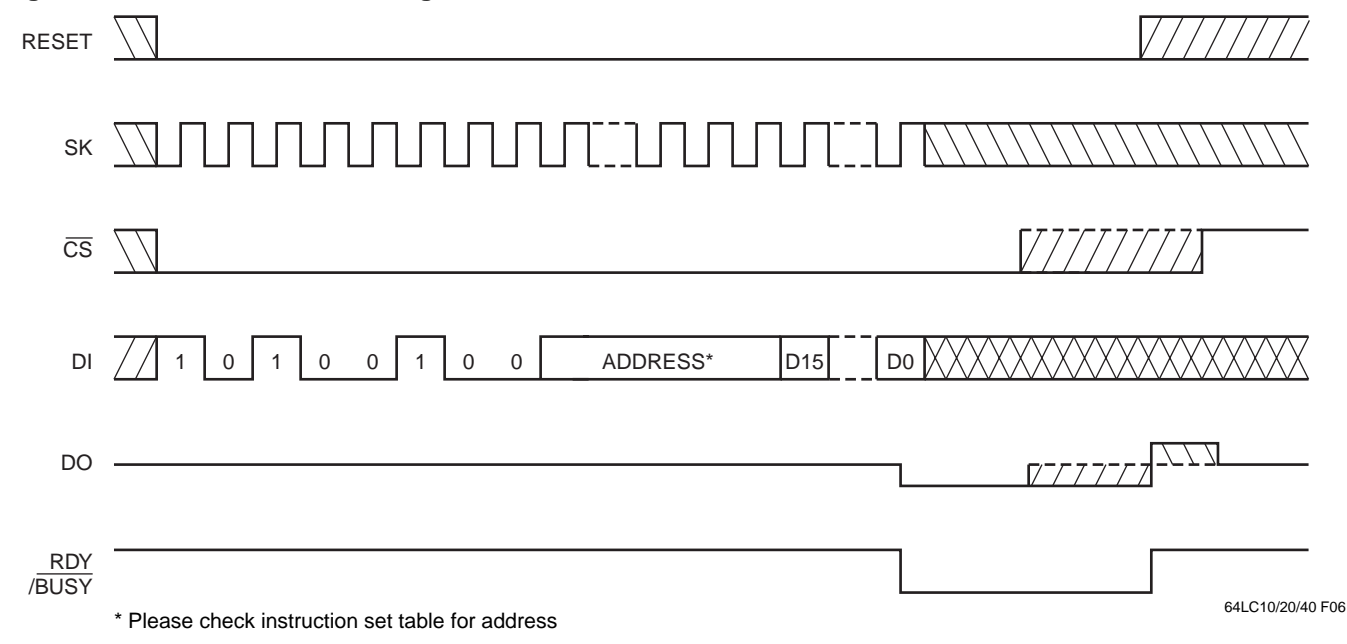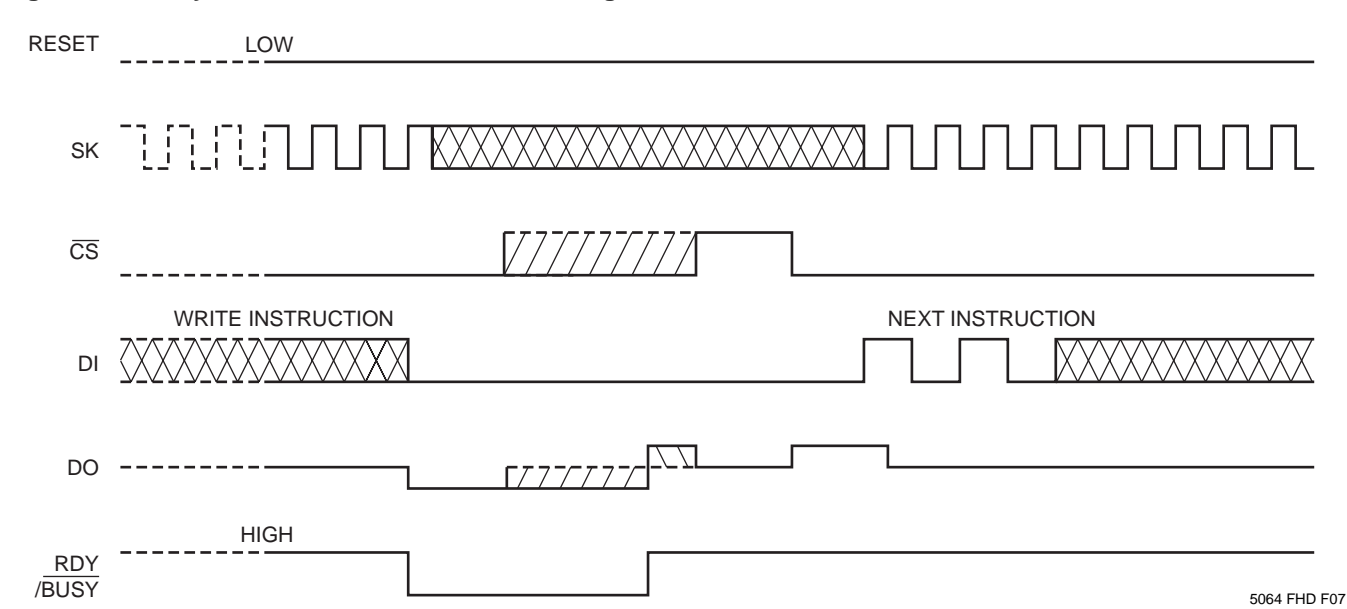
**Figure 4.  Write Instruction Timing**



* Please check instruction set table for address

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**Figure 5.  Ready/BUSY Status Instruction Timing**



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WRITE cycle. The RDY/$\overline{\text{BUSY}}$ pin will output the $\overline{\text{BUSY}}$ status (LOW) one $t_{SV}$ after the rising edge of the 32nd clock (the last data bit) and will stay LOW until the write cycle is complete. Then it will output a logical "1" until the next WRITE cycle. The RDY/$\overline{\text{BUSY}}$ output is not affected by the input of $\overline{\text{CS}}$.

An alternative to get RDY/$\overline{\text{BUSY}}$ status is from the DO pin. During a write cycle, asserting a LOW input to the $\overline{\text{CS}}$ pin will cause the DO pin to output the RDY/$\overline{\text{BUSY}}$ status. Bringing $\overline{\text{CS}}$ HIGH will bring the DO pin back to a high impedance state again. After the device has completed a WRITE cycle, the DO pin will output a

logical "1" when the device is deselected. The rising edge of the first "1" input on the DI pin will reset DO back to the high impedance state again.

The WRITE operation can be halted anywhere in the operation by the RESET input. If a RESET pulse occurs during a WRITE operation, the device will abort the operation and output a READY status.

NOTE: Data may be corrupted if a RESET occurs while the device is $\overline{\text{BUSY}}$. If the reset occurs before the $\overline{\text{BUSY}}$ period, no writing will be initiated. However, if RESET occurs after the $\overline{\text{BUSY}}$ period, new data will have been written over the old data.

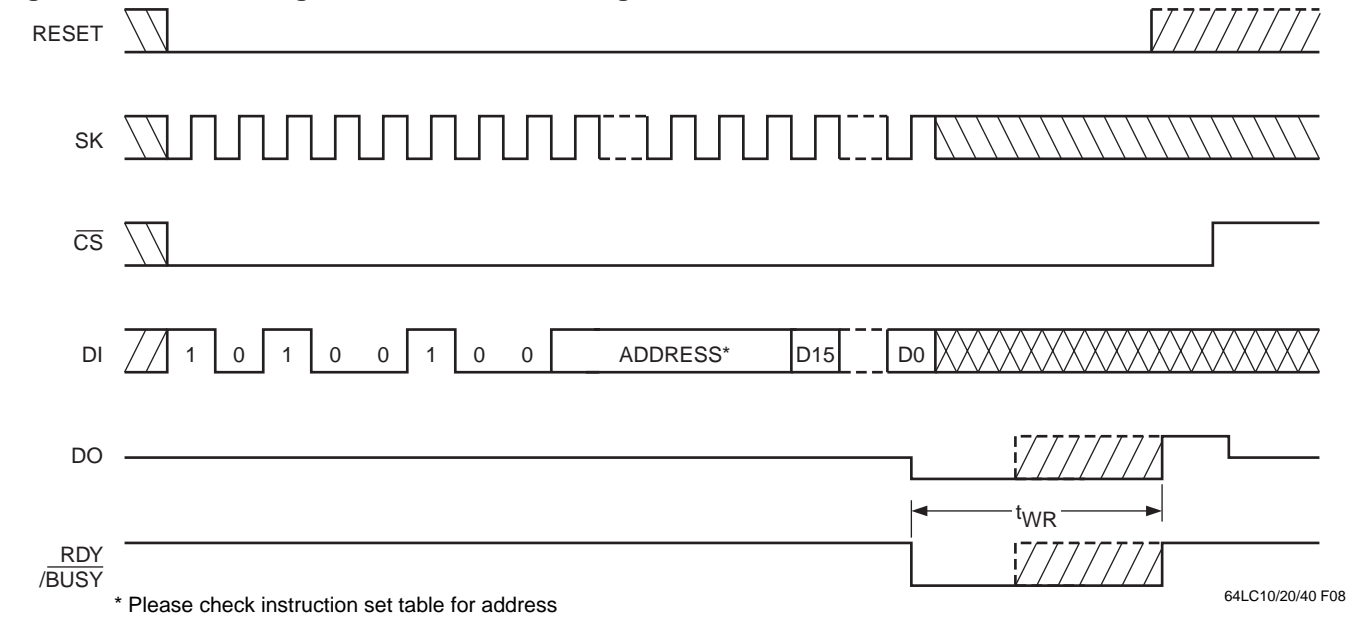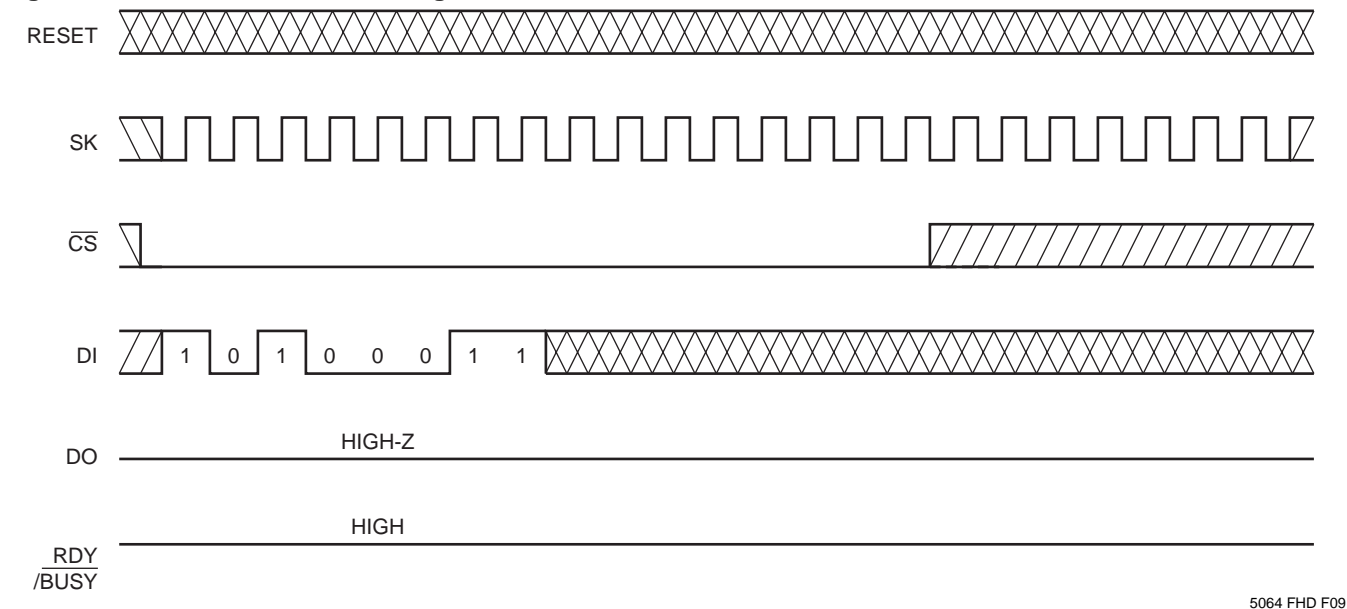**Figure 6.  RESET During $\overline{\text{BUSY}}$ Instruction Timing**



* Please check instruction set table for address

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**Figure 7.  EWEN Instruction Timing**



5064 FHD F09

## RESET

The RESET pin, when set to HIGH, will reset or abort a WRITE operation. When RESET is set to HIGH while the WRITE instruction is being entered, the device will not execute the WRITE instruction and will keep DO in High-Z condition.

When RESET is set to HIGH, while the device is in a clear/write cycle, the device will abort the operation and will display READY status on the RDY/$\overline{BUSY}$ pin and on the DO pin if $\overline{CS}$ is low.
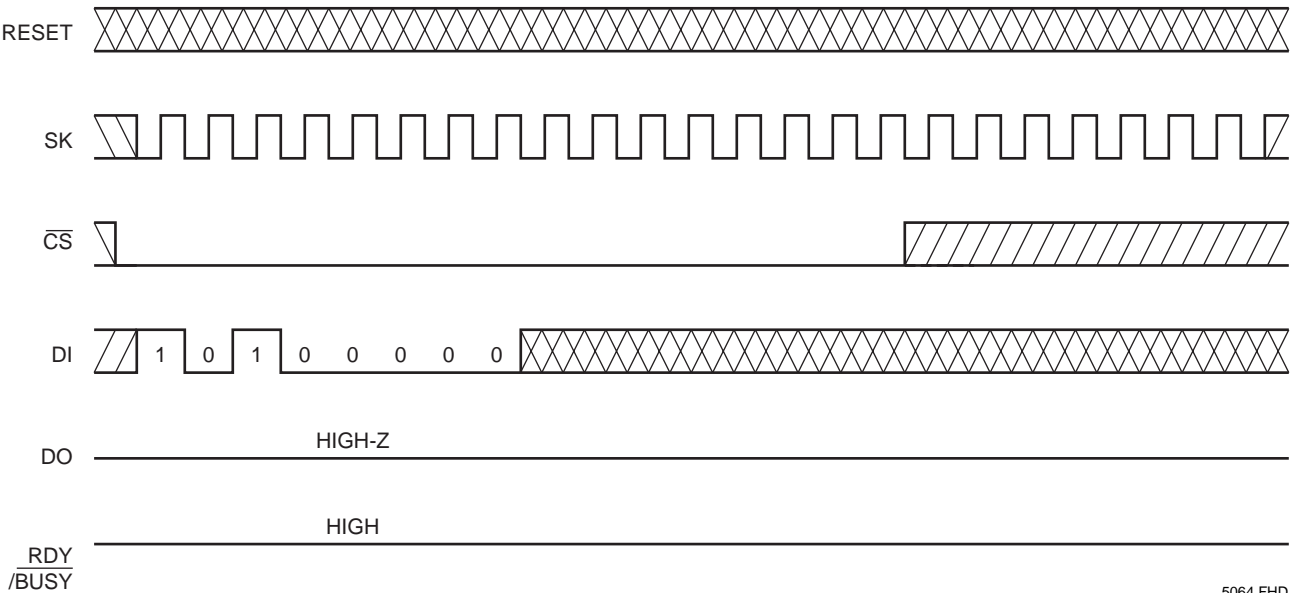
The RESET input affects only the WRITE and WRITE ALL operations. It does not reset any other operations such as READ, EWEN and EWDS.
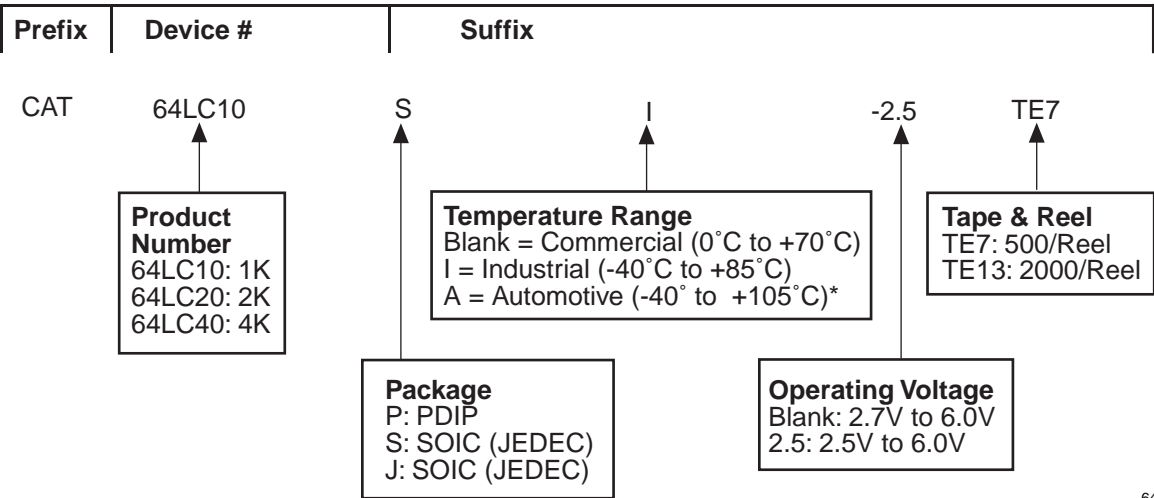
## ERASE/WRITE ENABLE and DISABLE

The CAT64LC10/20/40 powers up in the erase/write disabled state. After power-up or while the device is in an erase/write disabled state, any write operation must be preceded by an execution of the EWEN instruction. Once enabled, the device will stay enabled until an EWDS has been executed or a power-down has occured. The EWDS is used to prevent any inadvertent over-writing of the data. The EWEN and EWDS instructions have no affect on the READ operation and are not affected by the RESET input.

**Figure 8. EWDS Instruction Timing**



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## ORDERING INFORMATION



| Prefix | Device # | | Suffix | | | |
|---|---|---|---|---|---|---|
| CAT | 64LC10 | S | I | -2.5 | TE7 | |

**Product Number**
64LC10: 1K
64LC20: 2K
64LC40: 4K

**Package**
P: PDIP
S: SOIC (JEDEC)
J: SOIC (JEDEC)

**Temperature Range**
Blank = Commercial (0˚C to +70˚C)
I = Industrial (-40˚C to +85˚C)
A = Automotive (-40˚ to +105˚C)*

**Operating Voltage**
Blank: 2.7V to 6.0V
2.5: 2.5V to 6.0V

**Tape & Reel**
TE7: 500/Reel
TE13: 2000/Reel

\* -40˚C to +125˚C is available upon request

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Notes:
(1) The device used in the above example is a 64LC10SI-2.5TE7 (SOIC, Industrial Temperature, 2.5 Volt to 6 Volt Operating Voltage, Tape & Reel)

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