# MC74HC4024

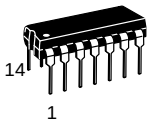
# 7-Stage Binary Ripple Counter
## High–Performance Silicon–Gate CMOS

The MC74HC4024 is identical in pinout to the standard CMOS MC14024. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

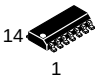
This device consists of 7 master–slave flip–flops. The output of each flip–flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative going edge of the Clock input. Reset is asynchronous and active–high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4024 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 206 FETs or 51.5 Equivalent Gates




**N SUFFIX**
PLASTIC PACKAGE
CASE 646–06

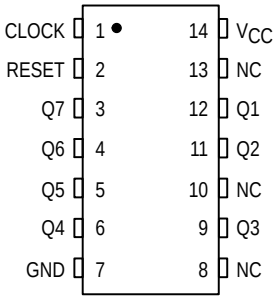



**D SUFFIX**
SOIC PACKAGE
CASE 751A–03

**ORDERING INFORMATION**

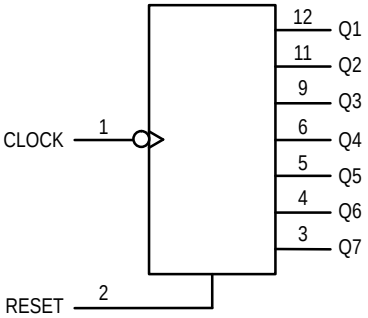
| | |
|---|---|
| MC74HCXXXXN | Plastic |
| MC74HCXXXXD | SOIC |

**PIN ASSIGNMENT**




NC = NO CONNECTION

**LOGIC DIAGRAM**




PIN 14 = $V_{CC}$
PIN 7 = GND
PINS 8, 10 AND 13 = NO CONNECTION

**FUNCTION TABLE**

| Clock | Reset | Output State |
|---|---|---|
| ↗ | L | No Change |
| ↘ | L | Advance to Next State |
| X | H | All Outputs are Low |







MOTOROLA

**MAXIMUM RATINGS***

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | – 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | – 1.5 to $V_{CC}$ + 1.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air Plastic DIP† | 750 | mW |
| | SOIC Package† | 500 | |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | – 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time $V_{CC}$ = 2.0 V | 0 | 1000 | ns |
| | (Figure 1) $V_{CC}$ = 4.5 V | 0 | 500 | |
| | $V_{CC}$ = 6.0 V | 0 | 400 | |

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = $V_{CC}$ – 0.1 V, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 0.3 | 0.3 | 0.3 | V |
| | | | 4.5 | 0.9 | 0.9 | 0.9 | |
| | | | 6.0 | 1.2 | 1.2 | 1.2 | |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\|$ ≤ 4.0 mA | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | $\|I_{out}\|$ ≤ 5.2 mA | 6.0 | 5.48 | 5.34 | 5.20 | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\|$ ≤ 4.0 mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | $\|I_{out}\|$ ≤ 5.2 mA | 6.0 | 0.26 | 0.33 | 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND, $I_{out}$ = 0 μA | 6.0 | 8 | 80 | 160 | μA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $f_{max}$ | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 2.0<br>4.5<br>6.0 | 5.4<br>27<br>32 | 4.4<br>22<br>26 | 3.6<br>18<br>21 | MHz |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4) | 2.0<br>4.5<br>6.0 | 210<br>42<br>36 | 265<br>53<br>45 | 315<br>63<br>54 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4) | 2.0<br>4.5<br>6.0 | 210<br>42<br>36 | 265<br>53<br>45 | 315<br>63<br>54 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, QN to QN + 1 (Figures 3 and 4) | 2.0<br>4.5<br>6.0 | 125<br>25<br>21 | 155<br>31<br>26 | 190<br>38<br>32 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0<br>4.5<br>6.0 | 75<br>15<br>13 | 95<br>19<br>16 | 110<br>22<br>19 | ns |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

* For $T_A$ = 25°C and $C_L$ = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:
$V_{CC}$ = 2.0 V: $t_P$ = [205 + 100(N – 1)] ns
$V_{CC}$ = 4.5 V: $t_P$ = [41 + 20(N – 1)] ns
$V_{CC}$ = 6.0 V: $t_P$ = [35 + 17(N – 1)] ns

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Package)* | 30 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** (Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{rec}$ | Minimum Recovery Time, Reset Inactive to Clock (Figure 2) | 2.0<br>4.5<br>6.0 | 100<br>20<br>17 | 125<br>25<br>21 | 150<br>30<br>26 | ns |
| $t_w$ | Minimum Pulse Width, Clock (Figure 1) | 2.0<br>4.5<br>6.0 | 80<br>16<br>14 | 100<br>20<br>17 | 120<br>24<br>20 | ns |
| $t_w$ | Minimum Pulse Width, Reset (Figure 2) | 2.0<br>4.5<br>6.0 | 80<br>16<br>14 | 100<br>20<br>17 | 120<br>24<br>20 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times (Figure 1) | 2.0<br>4.5<br>6.0 | 1000<br>500<br>400 | 1000<br>500<br>400 | 1000<br>500<br>400 | ns |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

## PIN DESCRIPTIONS

### INPUTS

**Clock (Pin 1)**

Negative edge triggering clock input. A High to low transition of this input advances the state of the counter.

**Reset (Pin 2)**

Active high asynchronous reset. A high level applied to this input resets the counter to its zero state, thus forcing all Q outputs low.

### OUTPUTS

**Q1 – Q7 (Pins 12, 11, 9, 6, 5, 4, 3)**

Active–high outputs. Each QN output divides the Clock input frequency by $2^N$.

## SWITCHING WAVEFORMS

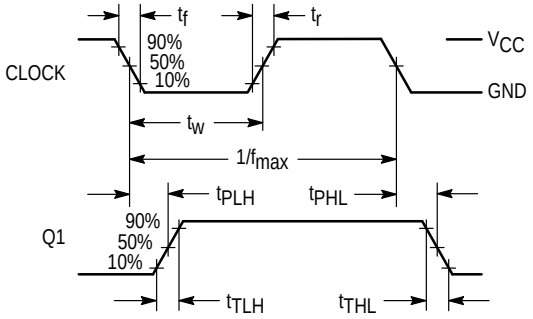



**Figure 1.**

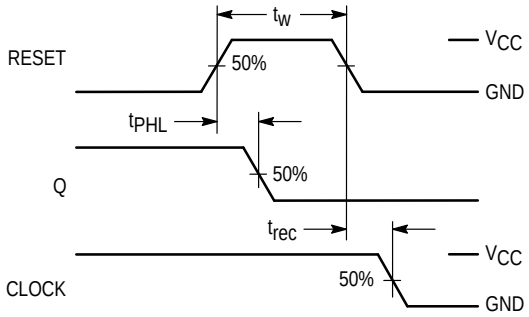



**Figure 2.**

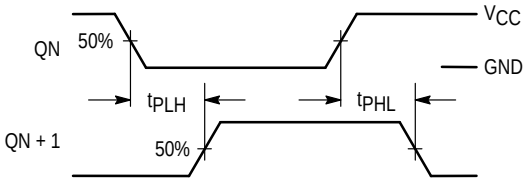
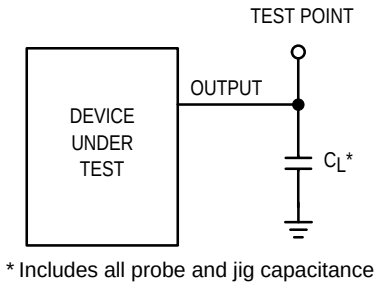


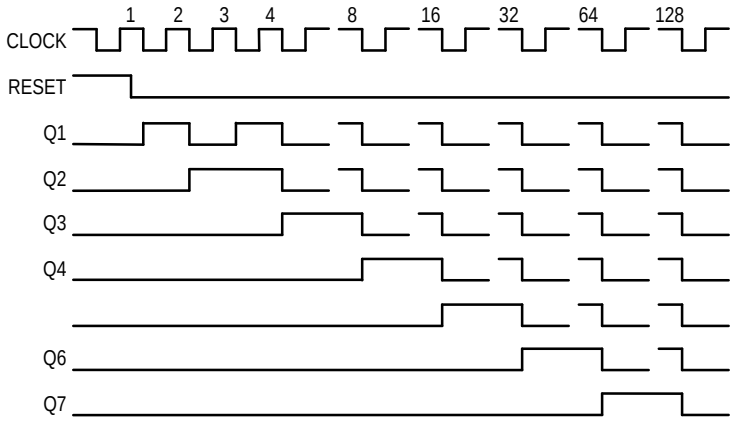

**Figure 3.**



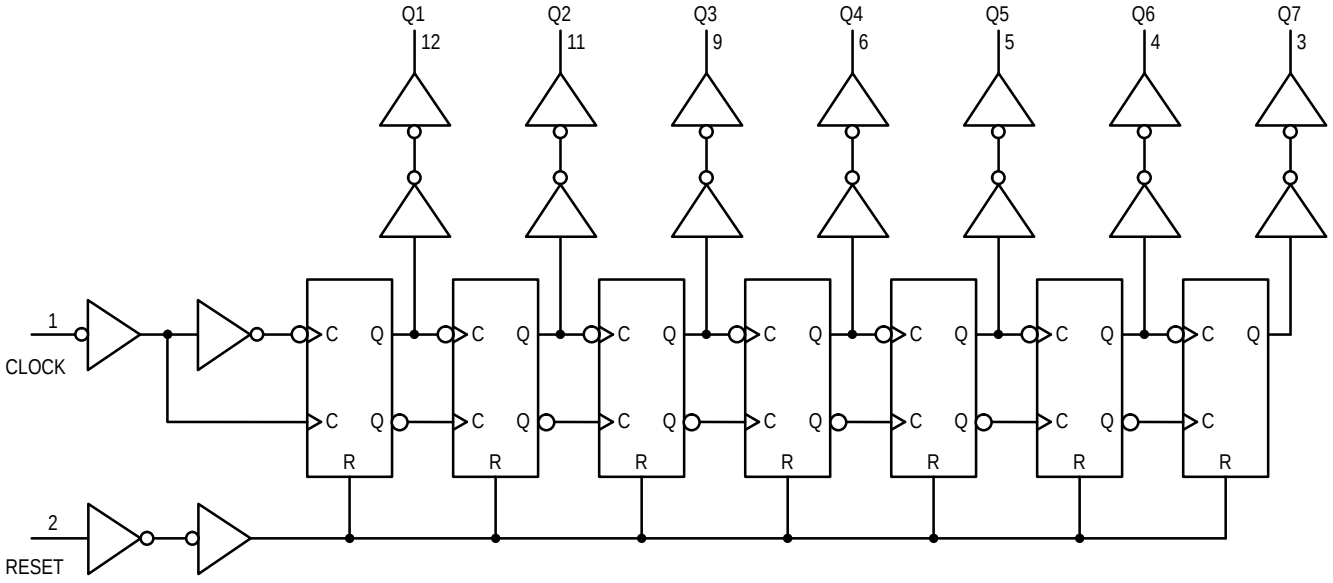

* Includes all probe and jig capacitance

**Figure 4. Test Circuit**

**TIMING DIAGRAM**

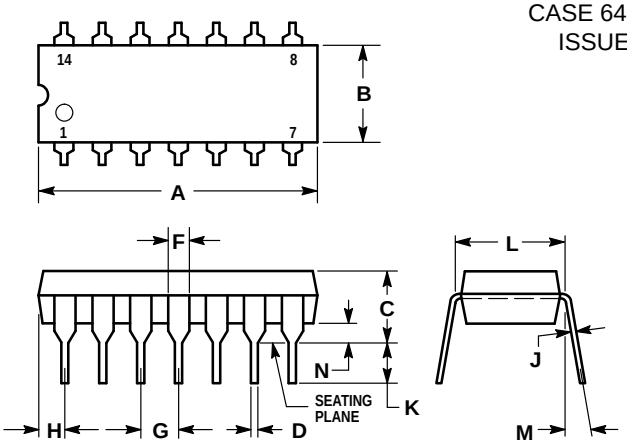



**EXPANDED LOGIC DIAGRAM**



## OUTLINE DIMENSIONS

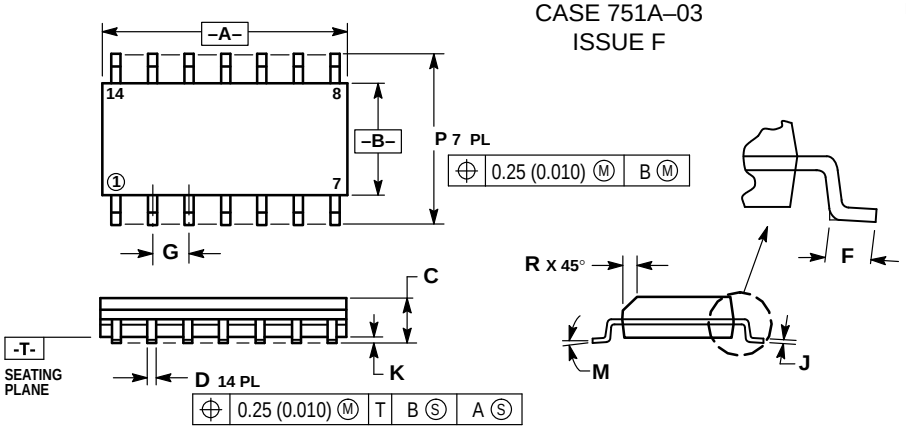
### N SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L




NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.015 | 0.039 | 0.39 | 1.01 |

### D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |



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